Asynchronous Sequential Logic

LECTURE 3

- **Introduction**
- **Analysis Procedure**

Dronacharya Group of Institutions

Introduction

- **Synchronous Sequential Circuits**

The change of internal state occurs in response to the synchronized clock pulse.

Memory elements are clocked flip-flops.

- **Asynchronous Sequential Circuits**

The change of internal state occurs when there is a change in the input variables.

Memory elements are unclocked flip-flops or time-delay elements.

Introduction

- **Synchronous Sequential Circuits**

Timing problems are eliminated by triggering all flip-flops with pulse edge.

Higher speed
More economical

- **Asynchronous Sequential Circuits**

Care must be taken to ensure that each new state is stable even though a feedback path exists.

Introduction

- **Asynchronous Sequential Circuits**

When an input variable changes in value, the *y* secondary variables do not change instantaneously.

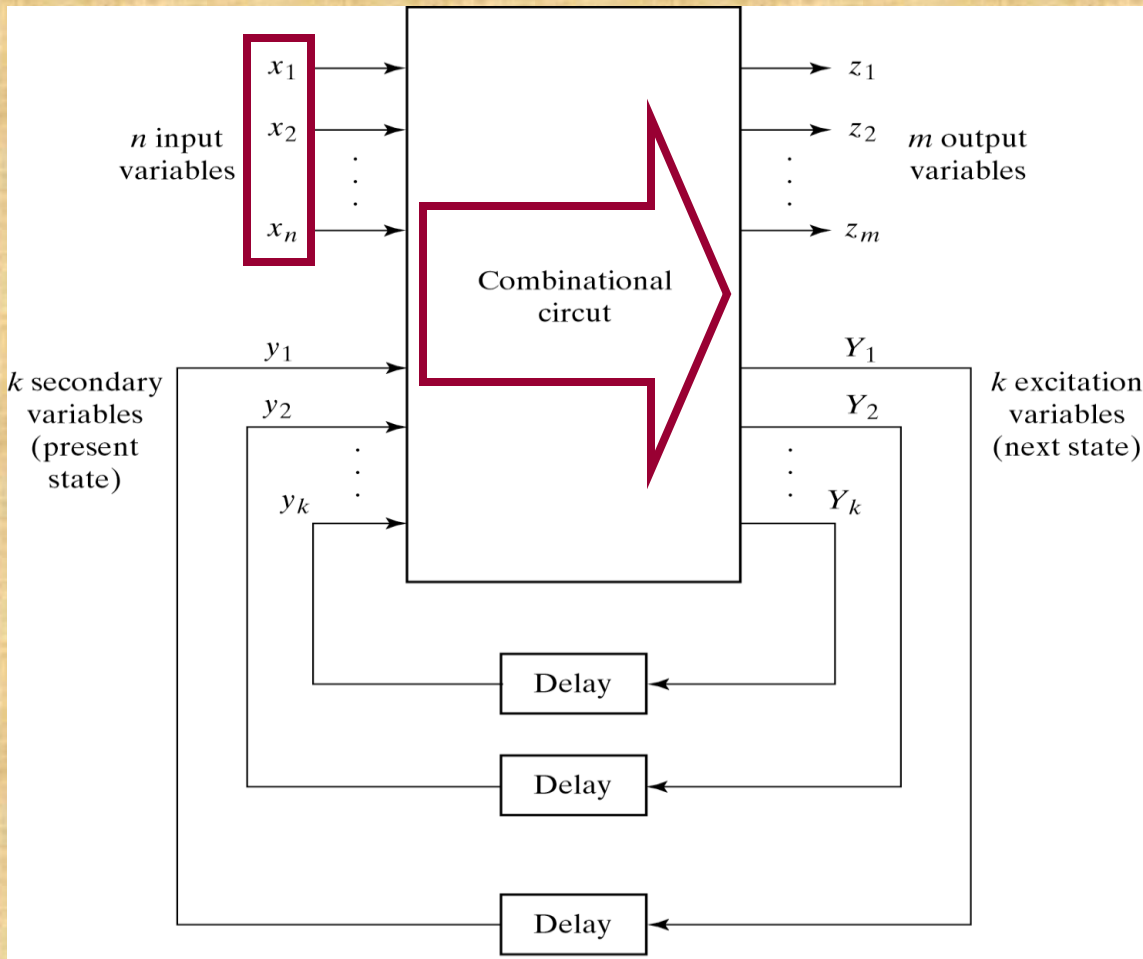


Fig. 9-1 Block Diagram of an Asynchronous Sequential Circuit

Introduction

- **Asynchronous Sequential Circuits**

In steady-state condition, the *y*'s and the *Y*'s are the same, but during transition they are not.

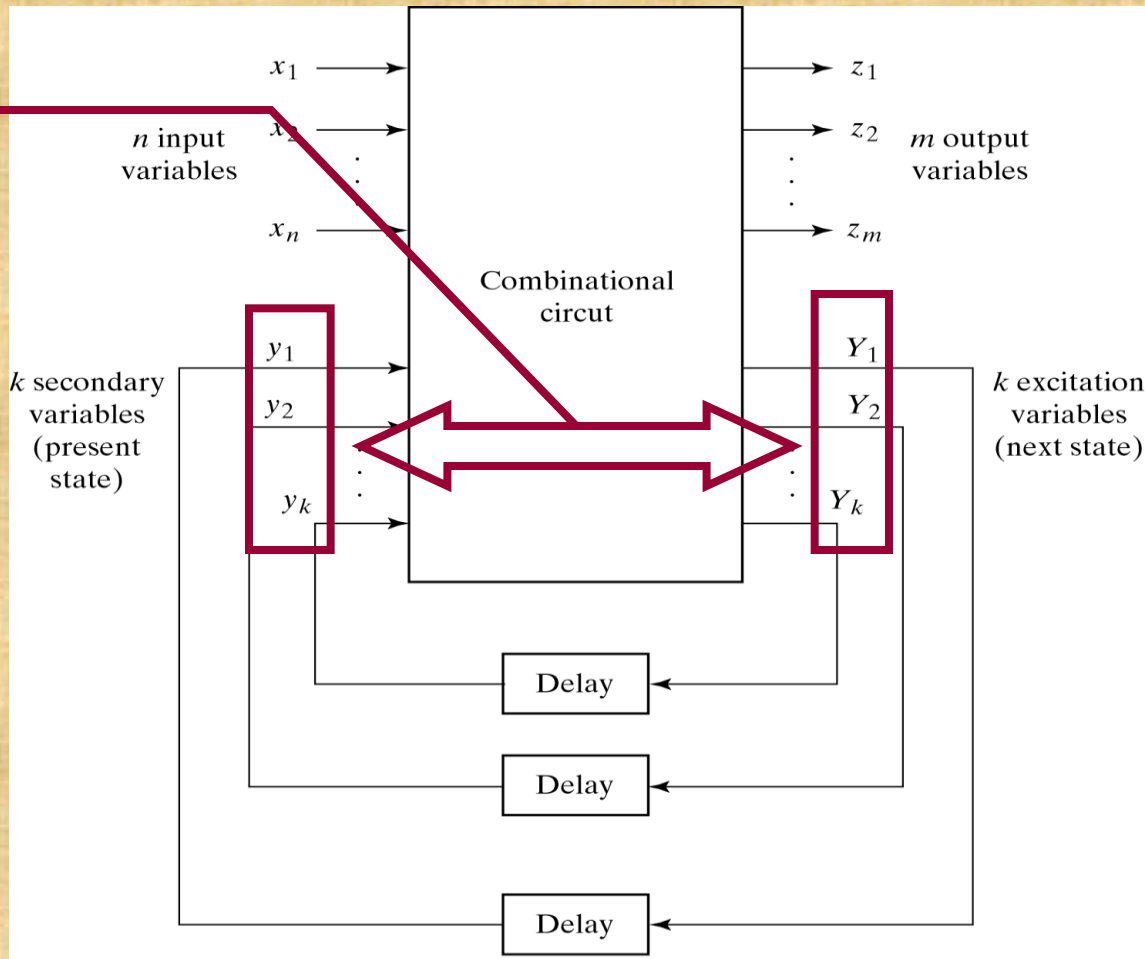


Fig. 9-1 Block Diagram of an Asynchronous Sequential Circuit

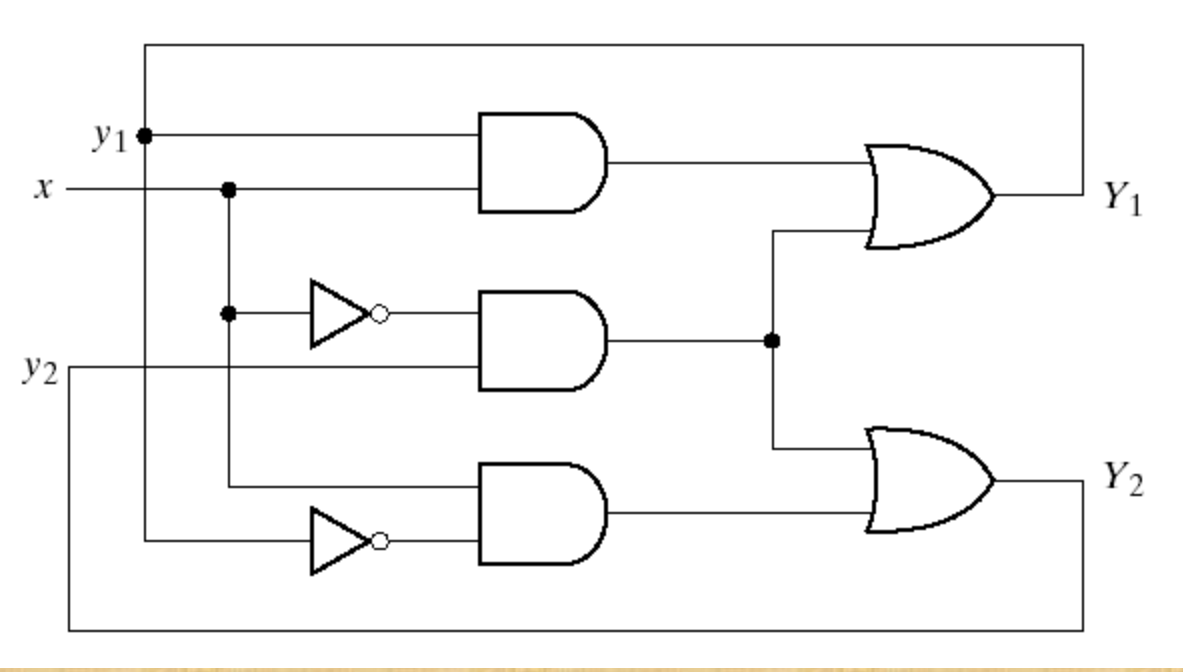
Introduction

- **Fundamental mode**

Fundamental mode :Only one input variable can change at any one time and the time between two input changes must be longer than the time it takes the circuit to reach a stable state.

Analysis Procedure

Transition Table



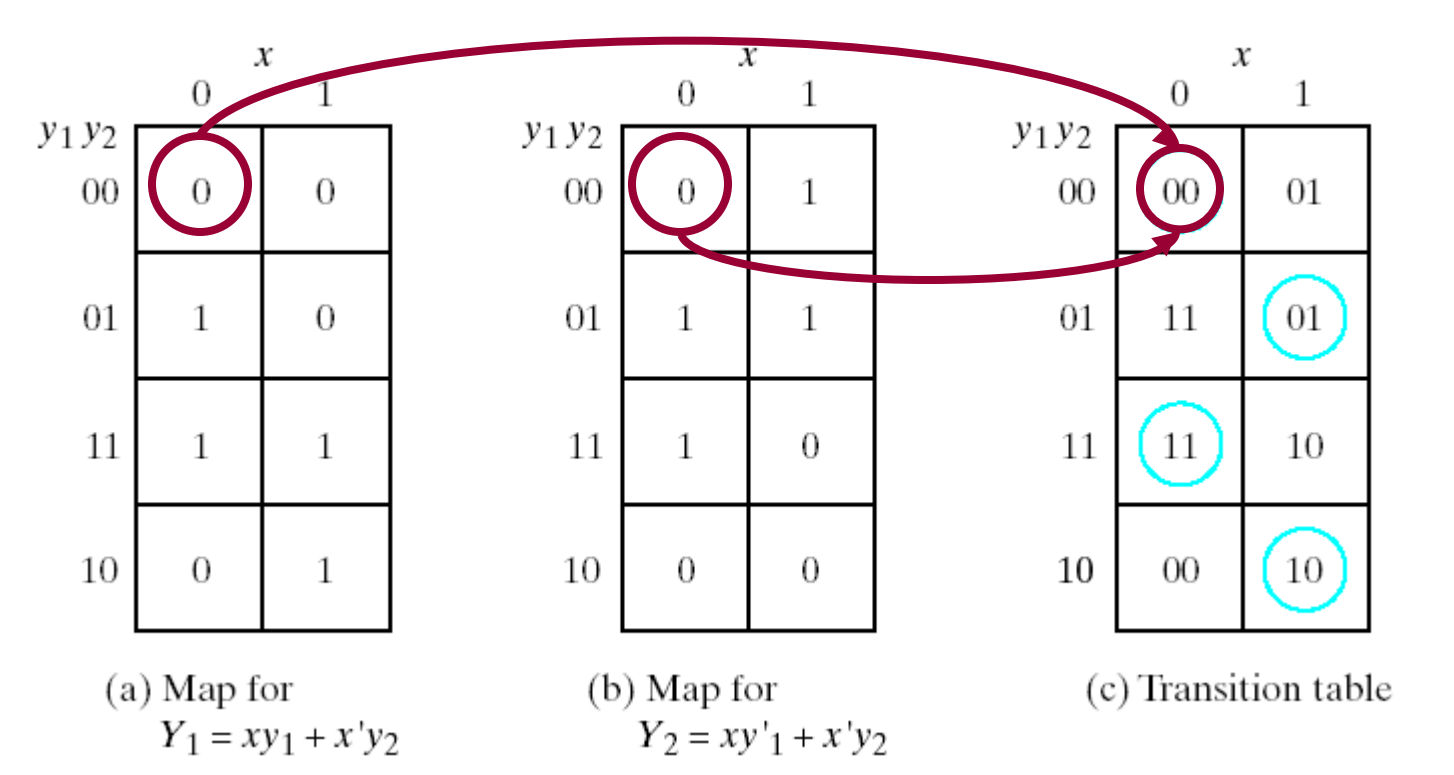
$$Y_1 = xy_1 + x'y_2$$

$$Y_2 = xy'_1 + x'y_2$$

Analysis Procedure

Transition Table

$Y_1 = xy_1 + x'y_2$ $Y_2 = xy'_1 + x'y_2$



$y_1 y_2$	$x=0$	$x=1$
00	0	0
01	1	0
11	1	1
10	0	1

(a) Map for $Y_1 = xy_1 + x'y_2$

$y_1 y_2$	$x=0$	$x=1$
00	0	1
01	1	1
11	1	0
10	0	0

(b) Map for $Y_2 = xy'_1 + x'y_2$

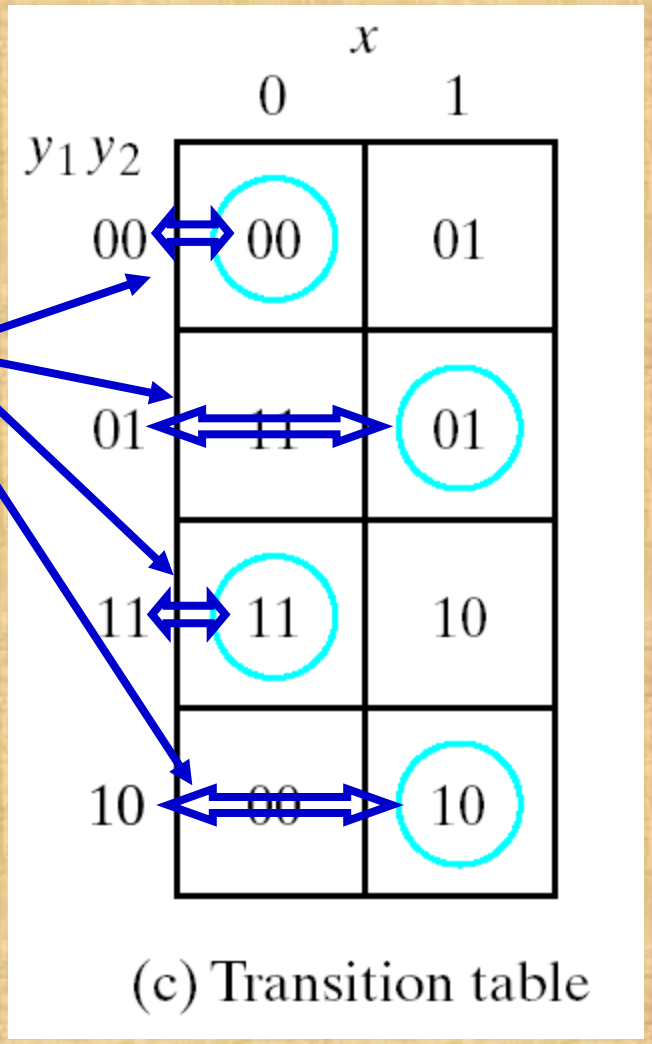
$y_1 y_2$	$x=0$	$x=1$
00	00	01
01	11	01
11	11	10
10	00	10

(c) Transition table

Analysis Procedure

Transition Table

For a state to be stable, the value of Y must be the same as that of $y = y_1 y_2$

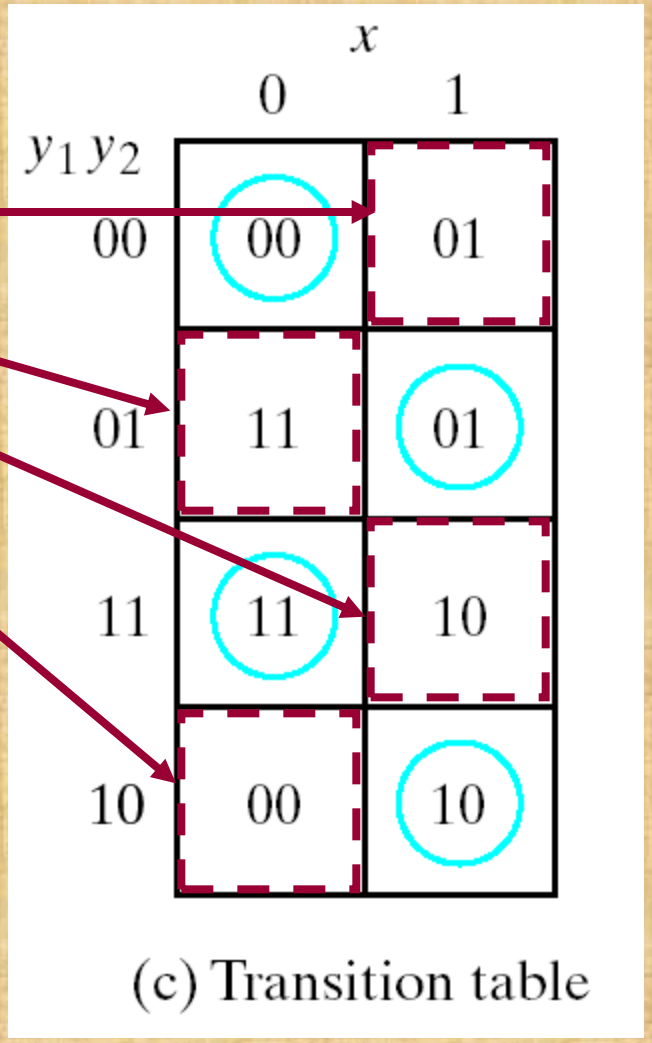


(c) Transition table

Analysis Procedure

Transition Table

The Unstable states,
$Y \neq y$



(c) Transition table

Analysis Procedure

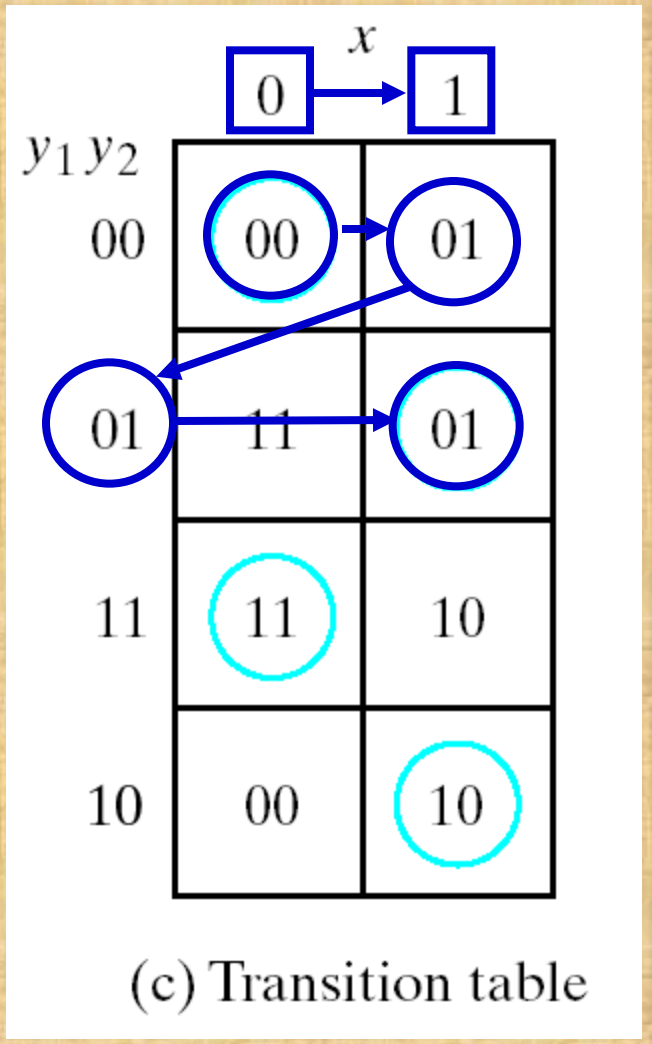
Transition Table

Consider the square for $x = 0$ and $y = 00$. It is stable.

x changes from 0 to 1.

The circuit changes the value of Y to 01. The state is unstable.

The feedback causes a change in y to 01. The circuit reaches stable.

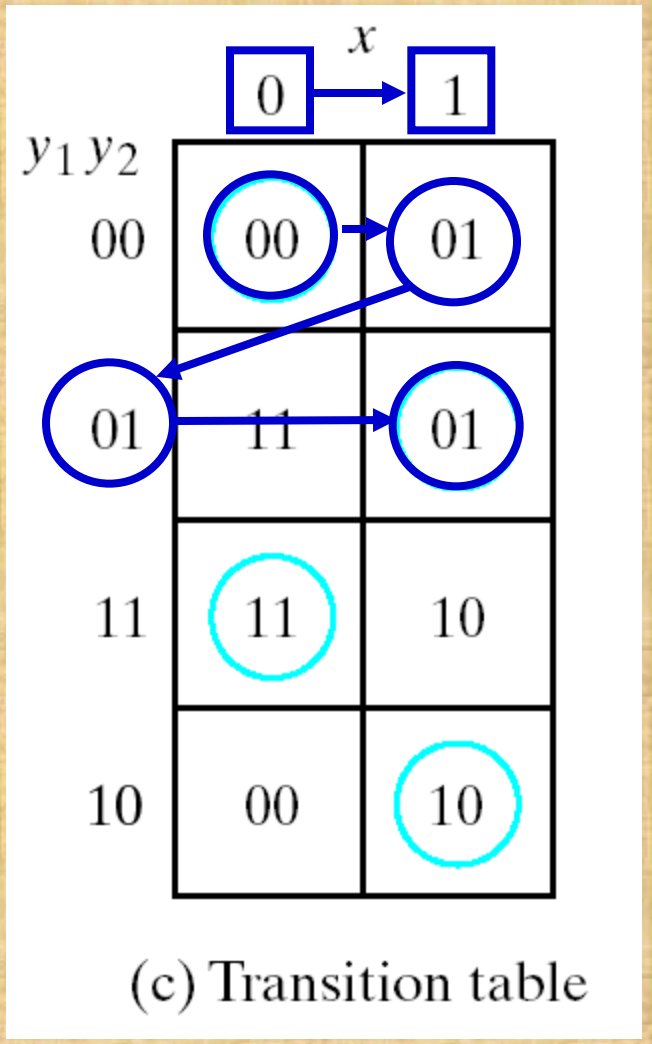


(c) Transition table

Analysis Procedure

Transition Table

In general, if a change in the input takes the circuit to an unstable state, *y* will change until it reaches a stable state.



(c) Transition table

Analysis Procedure

Flow Table

Flow Table

Transition table whose s
are named by letter sym
instead of binary values

	x = 0	x = 1
a	(a)	b
b	c	(b)
c	(c)	d
d	a	(d)

$y_1 y_2$	x = 0	x = 1
00	(00)	01
01	11	(01)
11	(11)	10
10	00	(10)

(c) Transition table

Analysis Procedure

Flow Table

It is called primitive flow table because it has only one stable state in each row.

	x = 0	x = 1
a	(a)	b
b	c	(b)
c	(c)	d
d	a	(d)

	x_1x_2 = 00	01	11	10
a	(a), 0	(a), 0	(a), 0	b, 0
b	a, 0	a, 0	(b), 1	(b), 0

(b) Two states with two inputs and one output

It is a flow table with more than one stable state in the same row.

Analysis Procedure

Flow Table

$y_1 y_2$	x = 0	x = 1
00	(00)	01
01	11	(01)
11	(11)	10
10	00	(10)

(c) Transition table

y	$x_1 x_2$ = 00	01	11	10
0	(0)	(0)	(0)	1
1	0	0	(1)	(1)

(a) Transition table

$Y = x_1 x'_2 + x_1 y$

y	$x_1 x_2$ = 00	01	11	10
0	0	0	0	0
1	0	0	1	0

(b) Map for output

$z = x_1 x_2 y$

Analysis Procedure

y \ x_1x_2	00	01	11	10
0	0	0	0	1
1	0	0	1	1

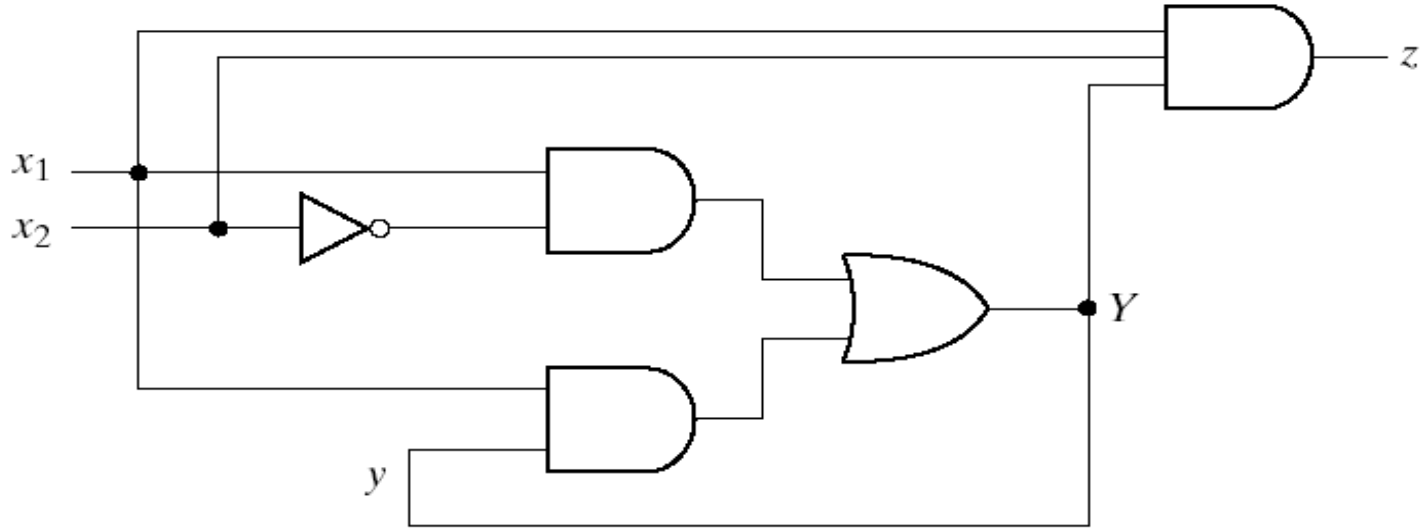
(a) Transition table

$Y = x_1x'_2 + x_1y$

y \ x_1x_2	00	01	11	10
0	0	0	0	0
1	0	0	1	0

(b) Map for output

$z = x_1x_2y$



Analysis Procedure

Two or more binary state variables change value in response to a change in an input variable

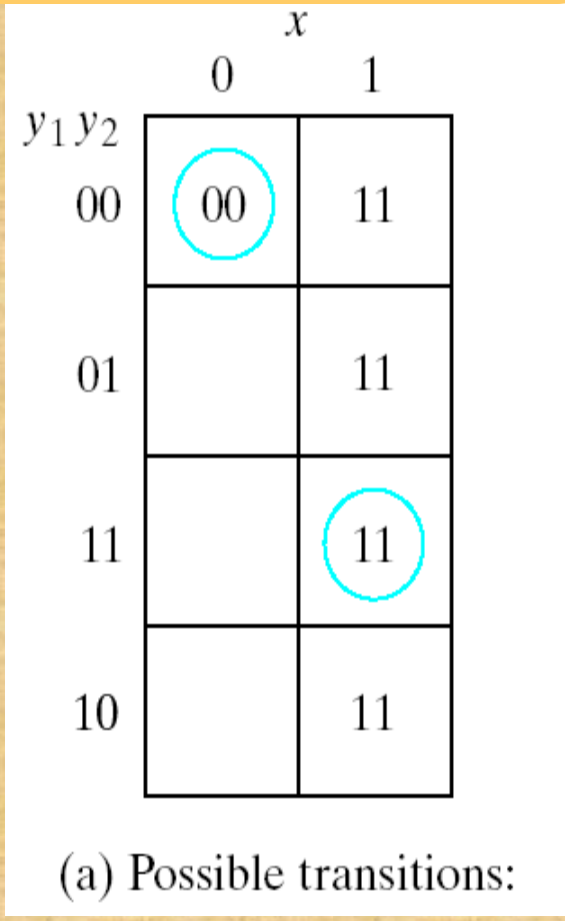
Race Conditions

Noncritical Race:

State variables change from 00 to 11. The possible transition could be

00	11	
00	01	11
00	10	11

It is a noncritical race. The final stable state that the circuit reaches does not depend on the order in which the state variables change.



(a) Possible transitions:

Analysis Procedure

Race Conditions

Critical Race:

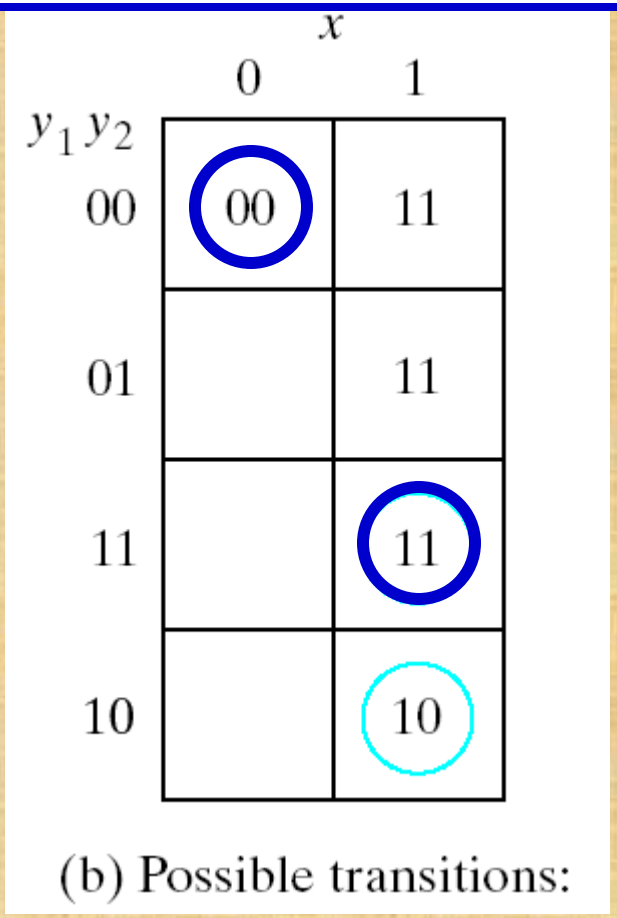
State variables change from 00 to 11. The possible transition could be

00 11

00 01 11

00 10

It is a critical race. The final stable state depends on the order in which the state variables change.



(b) Possible transitions:

Analysis Procedure

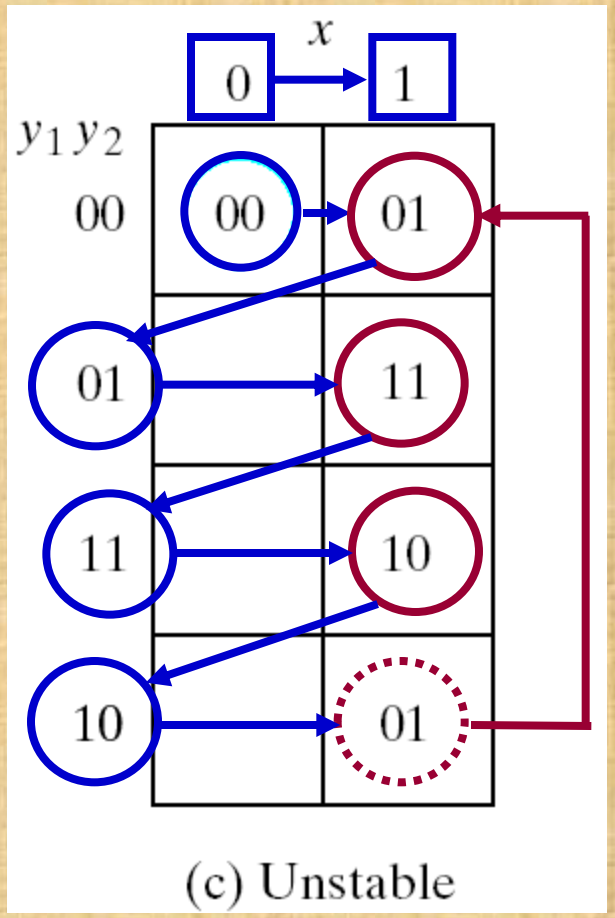
Race Conditions

Cycle

When a circuit goes through a unique sequence of unstable states, it is said to have a *cycle*.

It starts with $y_1 y_2$ =00, then input changes from 0 to 1.

The sequence is as follows,



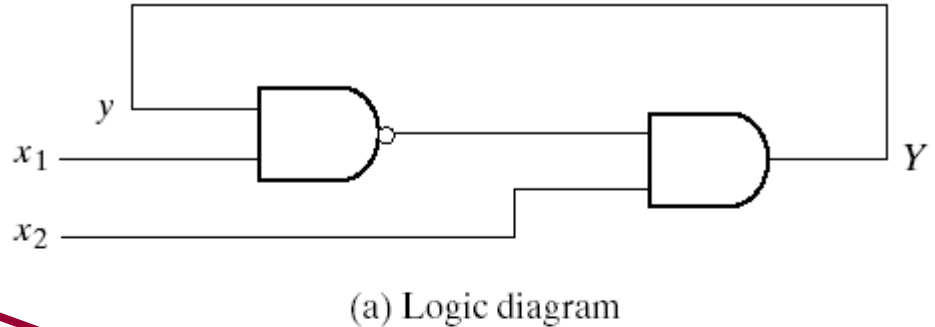
(c) Unstable

Analysis Procedure

Stability Consideration

Column 11 has no stable state. With input $x_1 x_2 = 11$, Y and y are never the same.

This will cause instability.



(a) Logic diagram

y	$x_1 x_2$ = 00	01	11	10
0	0	1	1	0
1	0	1	0	0

(b) Transition table