QUESTION BANK

Switching Theory and Logic Design

1) Define binary logic?

Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

2) Convert (634) 8 to binary

6 3 4

110 011 100

Ans = 110011100

3) Convert (9B2 - 1A) H to its decimal equivalent.

$N = 9 \times 16^2 + B \times 16^1 + 2 \times 16^0 + 1 \times 16^{-1} + A\ (10) \times 16^{-2}$

$= 2304 + 176 + 2 + 0.0625 + 0.039$

$= \mathbf{2482.1_{10}}$

4) State the different classification of binary codes?

1. Weighted codes
2. Non - weighted codes
3. Reflective codes
4. Sequential codes
5. Alphanumeric codes
6. Error Detecting and correcting codes.

5) Convert 0.640625 decimal numbers to its octal equivalent.

0.640625 x 8 = 5.125

0.125 x 8 = 1.0

= 0.640 625 10 = **(0.51) 8**

6) Convert 0.1289062 decimal number to its hex equivalent

0.1289062 x 16 = 2.0625

0.0625 x 16 = 1.0

$= \mathbf{0.21_{16}}$

7) Convert 22.64 to hexadecimal number.

16 22 -6

16 1 -1

0

0.64 x 16 = 10.24

0.24 x 16 = 3.84

0.84 x 16 = 13.44

.44 x 16 = 7.04

Ans = (16. A 3 D 7) 16

8) State the steps involved in Gray to binary conversion?

The MSB of the binary number is the same as the MSB of the gray code number. So write it down. To obtain the next binary digit, perform an exclusive OR operation between the bit just written down and the next gray code bit. Write down the result.

9) Convert gray code 101011 into its binary equivalent. Gray Code: 1 0 1 0 1 1

Binary Code: **1 1 0 0 1 0**

10) Substract (0 1 0 1) 2 from (1 0 1 1) 2

1 0 1 0

0 1 0 1

Answer = 0 1 1 0

11) Add (1 0 1 0) 2 and (0 0 1 1) 2

1 0 1 0 0 0 1 1

Answer = (1 1 0 1) 2

12) Using 10's complement subtract 72532 - 3250

M = 72532

10's complement of N = + 96750

Sum = 169282

Discard end carry

Answer = 69282

13) Find 2'S complement of (1 0 1 0 0 0 1 1) 2

0 1 0 1 1 1 0 0 1 - 1's Complement

\+ 1

0 1 0 1 1 1 0 1 0 - 2's complement.

14) Substract 1 1 1 0 0 1 2 from 1 0 1 0 1 1 2 using 2's complement method

1 0 1 0 1 1

+ 0 0 0 1 1 1 - 2's comp. of 1 1 1 0 0

1 1 1 0 0 1 0 in 2's complement form

Answer (0 0 1 1 1 0)2

15) Find the excess -3 code and 9's complement of the number 403_{10}

4 0 3

0 1 0 0 0 0 0 0 0 0 1 1 0

0 1 1 0 0 1 1 0 0 1 1 +

0 1 1 1 0 0 1 1 0 1 1 0 ----- excess 3 code

9's complement 1 0 0 0 1 1 0 0 1 0 0 1

16) What is meant by bit?

A binary digit is called bit

17) Define byte? Group

of 8 bits.

18) List the different number systems?

i) Decimal Number system

ii) Binary Number system

iii) Octal Number system

iv) Hexadecimal Number system

19) State the abbreviations of ASCII and EBCDIC code?

ASCII-American Standard Code for Information Interchange.

EBCDIC-Extended Binary Coded Decimal Information Code.

20) What are the different types of number complements?

i) r's Complement

ii) (r-1)'s Complement.

21) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction

(a) X -Y and (b) Y - X using 2's complements.
a) X = 1010100

2's complement of Y = 0111101

Sum = 10010001 Discard end carry

Answer: **X - Y = 0010001**

b) Y = 1000011 2's complement of X = + 0101100

Sum = 1101111 There is no end carry, The MSB BIT IS 1.

Answer is Y-X = -(2's complement of 1101111) = - 0010001

22) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction

(a) X -Y and (b) Y - X using 1's complements.

a) X - Y = 1010100 - 1000011

X = 1010100

1's complement of Y = + 0111100

Sum = 10010000

End -around carry = + 1

Answer: **X - Y = 0010001**

b) Y - X = 1000011 - 1010100

Y = 1000011

1's complement of X = + 0101011

Sum = +1101110

There is no end carry.

Therefore the answer is Y - X = -(1's complement of 1101110) = -0010001

23) Write the names of basic logical operators.

1. NOT / INVERT

2. AND

3. OR

24) What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative property and distributive property.

25) State the associative property of boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows:

A+ (B+C) = (A+B) +C

26) State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is:

A+B=B+A

27) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the the several variables and then AND ing the sums. The distributive property is:

A+BC= (A+B) (A+C)

28) State the absorption law of Boolean algebra.

The absorption law of Boolean algebra is given by X+XY=X, X(X+Y) =X.

29) Simplify the following using De Morgan's theorem [((AB)'C)" D]' [((AB)'C)" D]' = ((AB)'C)" + D' [(AB)' = A' + B']

= (AB)' C + D'

= (A' + B')C + D'

30) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra.

They are,

1) The complement of a product is equal to the sum of the complements.
(AB)' = A' + B'

2) The complement of a sum term is equal to the product of the complements.

(A + B)' = A'B'

31) Reduce A.A'C

A.A'C = 0.C [A.A' = 1]

= 0

31) Reduce A(A + B)

A(A + B) = AA + AB

= A(1 + B) [1 + B = 1]

= A.

32) Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]

= A'(C' + BC)

= A'(C' + B) [A + A'B = A + B]

33) Reduce AB + (AC)' + AB'C(AB + C)

AB + (AC)' + AB'C(AB + C) = AB + (AC)' + AAB'BC + AB'CC

= AB + (AC)' + AB'CC [A.A' = 0]

= AB + (AC)' + AB'C [A.A = 1]

= AB + A' + C' =AB'C [(AB)' = A' + B']

= A' + B + C' + AB'C [A + AB' = A + B]

= A' + B'C + B + C' [A + A'B = A + B]

= A' + B + C' +

B'C =A' + B + C' +

B' =A' + C' + 1

= 1 [A + 1 =1]

34) Simplify the following expression Y = (A + B)(A + C')(B' + C'

) Y = (A + B)(A + C')(B' + C')

= (AA' + AC +A'B +BC)(B' + C') [A.A' = 0]

= (AC + A'B + BC)(B' + C')

= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'

= AB'C + A'BC'

35) Show that (X + Y' + XY)(X + Y')(X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X)(X + Y')(X' + Y) [A + A'B = A + B]

= (X + Y')(X + Y')(X'Y) [A + A = 1]

= (X + Y')(X'Y) [A.A = 1]

= X.X' + Y'.X'.Y

= 0 [A.A' = 0]

36) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C + A'BC =AB + AB'C + A'BC

=A(B + B'C) + A'BC

=A(B + C) + A'BC

=AB + AC + A'BC

=B(A + C) + AC

=AB + BC + AC

=AB + AC +BC ...Proved

37) Convert the given expression in canonical SOP form Y = AC + AB + BC Y = AC + AB + BC

=AC(B + B') + AB(C + C') + (A + A')BC

=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC

=ABC + ABC' +AB'C + AB'C' [A + A =1]

38) Define duality property.

Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

39) Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x(y'z' + yz).

By applying De-Morgan's theorem.

F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z') F2' = [x(y'z' + yz)]' = x' + (y'z' + yz)'

= x' + (y'z')'(yz)'

= x' + (y + z)(y' + z')

40) Simplify the following expression

Y = (A + B) (A = C) (B + C)

= (A A + A C + A B + B C) (B + C)

= (A C + A B + B C) (B + C)

= A B C + A C C + A B B + A B C + B B C + B C C

= A B C

41) What are the methods adopted to reduce Boolean function?

i) Karnaug map

ii) Tabular method or Quine Mc-Cluskey method

iii) Variable entered map technique.

42) State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.

ii) The map method is restricted in its capability since they are useful for

simplifying only Boolean expression represented in standard
form. 43) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map
diagram is made up of squares, with each squares representing one minterm of the function.

44) Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC' Y = A'B'C' + A'B'C + A'BC + ABC'

=m0 + m1 +m3
+m6 =_m(0, 1, 3, 6)

45) Write the maxterms corresponding to the logical expression

Y = (A + B + C')(A + B' + C')(A' + B' + C)
= (A + B + C')(A + B' + C')(A' + B' +
C) =M1.M3.M6
=_ M(1,3,6)

46) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

47) What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

48) What is an essential implicant?

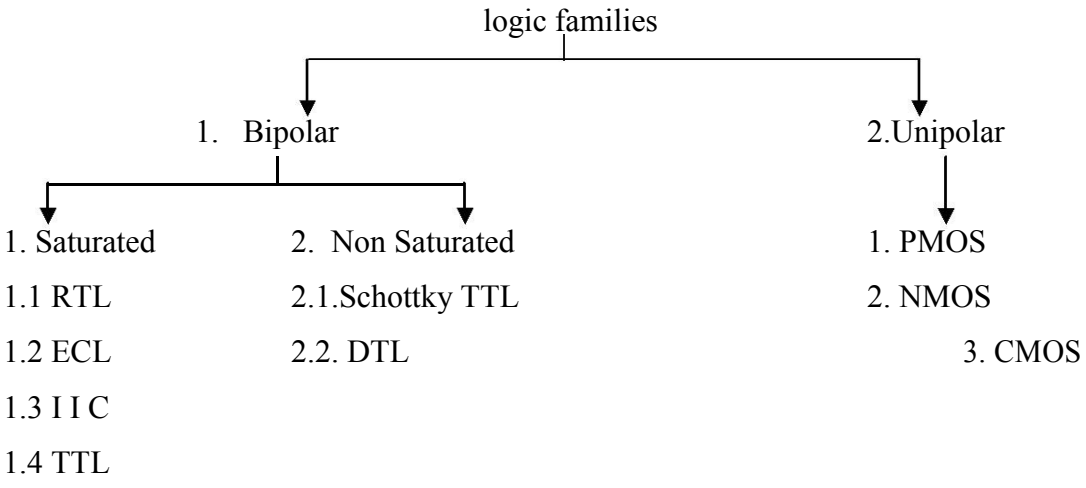
If a min term is covered by only one prime implicant, the prime implicant is said to be essential

Unit – II

49. What is a Logic gate?

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

50. Give the classification of logic families



51. What are the basic digital logic gates?

The three basic logic gates are

1. AND gate
2. OR gate
3. NOT gate

52. Which gates are called as the universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

53. Classify the logic family by operation?

The Bipolar logic family is classified into

1. Saturated logic

2. Unsaturated logic.

The RTL, DTL, TTL, I2L, HTL logic comes under the saturated logic family.

The Schottky TTL, and ECL logic comes under the unsaturated logic family.

54.State the classifications of FET devices.

FET is classified as

1. Junction Field Effect Transistor (JFET)
2. Metal oxide semiconductor family (MOS).

55.Mention the classification of saturated bipolar logic families.

The bipolar logic family is classified as follows:

1. RTL- Resistor Transistor Logic
2. DTL- Diode Transistor logic
3. I2L- Integrated Injection Logic
4. TTL- Transistor Transistor Logic
5. ECL- Emitter Coupled Logic

56.Mention the different IC packages?

1. DIP- Dual in line package
2. LCC- Leadless Chip Carrier
3. PLCC- Plastic Leaded Chip carrier
4. PQFP- Plastic Quad Flat Pack
5. PGA- Pin Grid Array

57. Mention the important characteristics of digital IC's?

1. Fan out
2. Power dissipation
3. Propagation Delay
4. Noise Margin
5. Fan In
6. Operating temperature
7. Power supply requirements

58. Define Fan-out?

Fan out specifies the number of standard loads that the output of the gate can drive with out impairment of its normal operation.

59. Define power dissipation?

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs.

60. What is propagation delay?

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

61. Define noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

62. Define fan in?

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

63. What is Operating temperature?

All the gates or semiconductor devices are temperature sensitive in nature. The temperature in which the performance of the IC is effective is called as operating temperature. Operating temperature of the IC vary from 00 C to 700 c.

64.What is High Threshold Logic?

Some digital circuits operate in environments, which produce very high noise signals. For operation in such surroundings there is available a type of DTL gate which possesses a high threshold to noise immunity. This type of gate is called HTL logic or High Threshold Logic.

65. What are the types of TTL logic?

1. Open collector output
2. Totem-Pole Output
3. Tri-state output.

66. What is depletion mode operation MOS?

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

67. What is enhancement mode operation of MOS?

If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

68. Mention the characteristics of MOS transistor?

1. The n- channel MOS conducts when its gate- to- source voltage is positive.

2. The p- channel MOS conducts when its gate- to- source voltage is negative

3. Either type of device is turned of if its gate- to- source voltage is zero.

69. How schottky transistors are formed and state its use?

A schottky diode is formed by the combination of metal and semiconductor. The presence of schottky diode between the base and the collector prevents the transistor from going into saturation. The resulting transistor is called as schottky transistor. The use of schottky transistor in TTL decreases the propagation delay without a sacrifice of power dissipation.

70. List the different versions of TTL

1.TTL (Std.TTL) 2.LTTL (Low Power TTL)

3.HTTL (High Speed TTL) 4.STTL (Schottky TTL)

5.LSTTL (Low power Schottky TTL)

71. Why totem pole outputs cannot be connected together.

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

72. State advantages and disadvantages of TTL

Adv:

Easily compatible with other ICs

Low output impedance

Disadv:

Wired output capability is possible only with tristate and open collector types Special circuits in Circuit layout and system design are required.

73. When does the noise margin allow digital circuits to function properly.

When noise voltages are within the limits of VNA(High State Noise Margin) and VNK for a particular logic family.

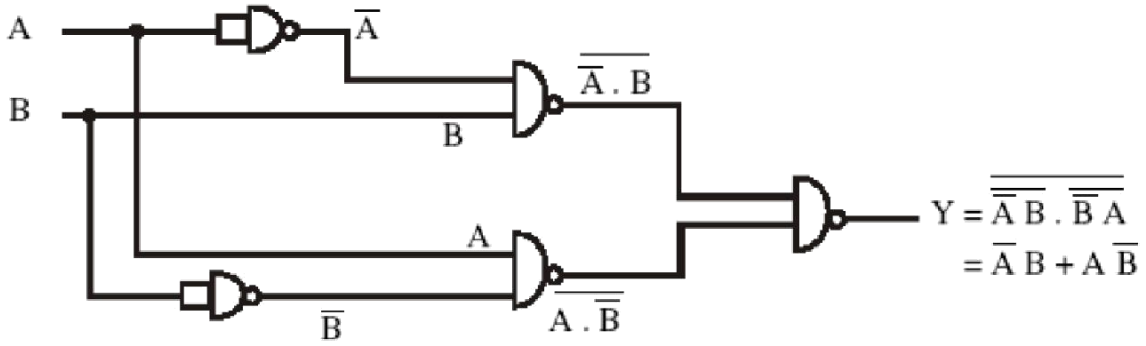
74. What happens to output when a tristate circuit is selected for high impedance.

Output is disconnected from rest of the circuits by internal circuitry.

75. What is 14000 series.

It is the oldest and standard CMOS family. The devices are not pin compatible or electrically compatible with any TTL Series.

76. Implement the Boolean Expression for EX – OR gate using NAND Gates.



77. Define combinational logic

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

78. Explain the design procedure for combinational circuits

1. The problem definition
2. Determine the number of available input variables & required O/P variables.
3. Assigning letter symbols to I/O variables
4. Obtain simplified Boolean expression for each O/P.
5. Obtain the logic diagram.

79. Define Half adder and full adder

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

90. Draw the logic Symbol and construct the truth table for the two input EX – OR gate.

Logic Symbol

Truth Table

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

81. Define Decoder?

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

82. What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

83. Define Encoder?

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

84. What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

85. Define multiplexer?

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

86. What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

87. List basic types of programmable logic devices.

1. Read only memory
2. Programmable logic Array
3. Programmable Array Logic

88. Define ROM

Read only memory is a device that includes both the decoder and the OR gates within a single IC package.

89. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

90. State the types of ROM

1. Masked ROM.
2. Programmable Read only Memory
3. Erasable Programmable Read only memory.

4. Electrically Erasable Programmable Read only Memory.

91. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

92. Which gate is equal to AND-invert Gate? NAND gate.

93. Which gate is equal to OR-invert Gate?
NOR gate.

94. Bubbled OR gate is equal to----------
NAND gate

95. Bubbled AND gate is equal to----------
NOR gate

Unit –III

96. What are the classification of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

1)Synchronous sequential circuit.
2)Asynchronous sequential circuit.

97. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

98.What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are, RS flip-flop

SR flip-flop

D flip-flop

JK flip-flop

T flip-flop

99.What is the operation of RS flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change
- When both the inputs R and S are high the output is unpredictable.

100.What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

101.What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

102. What is the operation of JK flip-flop?

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.

103. What is the operation of T flip-flop?

T flip-flop is also known as Toggle flip-flop.

- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output

toggles.

104. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

105. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

106. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

107.Define rise time.

The time required to change the voltage level from 10% to 90% is known as rise time(tr).

108.Define fall time.

The time required to change the voltage level from 90% to 10% is known as fall time(tf).

109.Define skew and clock skew.

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

110.Define setup time.

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{setup} .

111. Define hold time.

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{hold}.

112. Define propagation delay.

A propagation delay is the time required to change the output after the application of the input.

113.Define registers.

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

114.Define shift registers.

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

115.What are the different types of shift type? There are five types. They are,

Serial In Serial Out Shift Register
Serial In Parallel Out Shift Register
Parallel In Serial Out Shift Register
Parallel In Parallel Out Shift Register
Bidirectional Shift Register

116.Explain the flip-flop excitation tables for RS FF. RS flip-flop

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

0 ⟶0 transition: This can happen either when R=S=0 or when R=1 and S=0. 0 ⟶1 transition: This can happen only when S=1 and R=0.

1 ⟶0 transition: This can happen only when S=0 and R=1.

1 ⟶1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

117.Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state. They are,

0⟶0 transition: This can happen when J=0 and K=1 or K=0.

0⟶1 transition: This can happen either when J=1 and K=0 or when J=K=1.

1 → 0 transition: This can happen either when J=0 and K=1 or when J=K=1.

1 → 1 transition: This can happen when K=0 and J=0 or J=1.

118.Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Q_{n+1} has to 0,and if Q_{n+1} has to be 1 regardless the value of Q_n.

119. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0,the state of the flip-flop remains unchanged. Therefore, for 0 → 0 and 1 → 1transitions T must be 0 and or 0 → 1 and 1 → 0 transitions must be 1.

120. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

121.Give the comparison between combinational circuits and sequential circuits.

Combinational circuits	Sequential circuits
1. Memory unit is not required	1. Memory unity is required
2. Parallel adder is a combinational circuit	2. Serial adder is a sequential circuit

122. What do you mean by present state?

The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

123. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

124. State the types of sequential circuits?

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

125. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

126. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

127.Give the comparison between synchronous & Asynchronous sequential circuits?

Synchronous sequential circuits	Asynchronous sequential circuits.
1.Memory elements are clocked flip-flops	1.Memory elements are either unlocked flip - flops or time delay elements.
2. Easier to design	2. More difficult to design

128.Define flip-flop

Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

129. Draw the logic diagram for SR latch using two NOR gates.

130. The following wave forms are applied to the inputs of SR latch. Determine the Q waveform Assume initially Q = 1

Here the latch input has to be pulsed momentarily to cause a change in the latch output state, and the output will remain in that new state even after the input pulse is over.

131.What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

132.What are the types of shift register?

1. Serial in serial out shift register?
2. Serial in parallel out shift register
3. Parallel in serial out shift register
4. Parallel in parallel out shift register
5. Bidirectional shift register shift register

133.State the types of counter?

1. Synchronous counter
2. Asynchronous Counter

134.Give the comparison between synchronous & Asynchronous counters.

Asynchronous counters	Synchronous counters

In this type of counter flip-flops are connected in such a way that output of 1st flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip - flop
All the flip-flops are Not clocked simultaneously	All the flip-flops are clocked simultaneously

135.The t pd for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter.

f max (ripple) = 5 x 50 ns = 4 MHZ

Unit-IV

136. What are secondary variables?

-present state variables in asynchronous sequential circuits 137.What are excitation variables?

-next state variables in asynchronous sequential circuits 138. What is fundamental mode sequential circuit?

-input variables changes if the circuit is stable -inputs are levels, not pulses

-only one input can change at a given time

139. What are pulse mode circuit?

-inputs are pulses

-width of pulses are long for circuit to respond to the input

-pulse width must not be so long that it is still present after the new state is reached

140. What are the significance of state assignment?

In synchronous circuits-state assignments are made with the objective of circuit reduction

Asynchronous circuits-its objective is to avoid critical races

141. When do race condition occur?

-two or more binary state variables change their value in response to the change in i/p variable

142.What is non critical race?

-final stable state does not depend on the order in which the state variable changes

-race condition is not harmful

143.What is critical race?

-final stable state depends on the order in which the state variable changes

-race condition is harmful

144. When does a cycle occur?

-asynchronous circuit makes a transition through a series of unstable state

145.What are the different techniques used in state assignment?

-shared row state assignment

-one hot state assignment

146.What are the steps for the design of asynchronous sequential circuit?

-construction of primitive flow table

-reduction of flow table -

state assignment is made

-realization of primitive flow table

147.What is hazard?

-unwanted switching transients

148.What is static 1 hazard?

-output goes momentarily 0 when it should remain at 1

149.What is static 0 hazard?

-output goes momentarily 1 when it should remain at 0

150. What is dynamic hazard?

-output changes 3 or more times when it changes from 1 to 0 or 0 to 1 151.What is the cause for essential hazards?

-unequal delays along 2 or more path from same input 151.What is flow table?

-state table of an synchronous sequential network 152.What is SM chart?

-describes the behavior of a state machine

-used in hardware design of digital systems

152.What are the advantages of SM chart?

-easy to understand the operation

-east to convert to several equivalent forms

153. What is primitive flow chart?

-one stable state per row

154.What is combinational circuit?

Output depends on the given input. It has no storage element.

155.What is state equivalence theorem ?

Two states SA and SB, are equivalent if and only if for every possible input X sequence, the outputs are the same and the next states are equivalent

i.e., if SA (t + 1) = SB (t + 1) and ZA = ZB then SA = SB.

156.What do you mean by distinguishing sequences?

Two states, SA and SB of sequential machine are distinguishable if and only if their

exists at least one finite input sequence. Which, when applied to sequential machine causes different output sequences depending on whether SA or SB is the initial state.

157. Prove that the equivalence partition is unique

Consider that there are two equivalence partitions exists : PA and PB, and PA) PB. This states that, there exist 2 states Si & Sj which are in the same block of one partition and not in the same block of the other. If Si & Sj are in different blocks of say PB, there exists at least on input sequence which distinguishes Si & Sj and therefore, they cannot be in the same block of PA.

158.Define compatibility

States Si and Sj said to be compatible states, if and only if for every input sequence

that affects the two states, the same output sequence, occurs whenever both outputs are specified and regardless of whether Si on Sj is the initial state.

159.Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each

compatible state pair. It two states are incompatible no connecting line is drawn.

160.Define incompatibility

The states are said to be incompatible if no line is drawn in between them. If implied

states are incompatible, they are crossed & the corresponding line is ignored.

161.Explain the procedure for state minimization.

1. Partition the states into subsets such that all states in the same subsets are 1 - equivalent.

2. Partition the states into subsets such that all states in the same subsets are 2 - equivalent.

3. Partition the states into subsets such that all states in the same subsets are 3 - equivalent.

162.Define closed covering

A Set of compatibles is said to be closed if, for every compatible contained in the set, all its implied compatibles are also contained in the set. A closed set of compatibles, which contains all the states of M, is called a closed covering.

163.Define machine equivalence

Two machines, M1 and M2 are said to be equivalent if and only if, for every state in M1, there is a corresponding equivalent state in M2 & vice versa.

164.Define state table.

For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

165. Define total state

The combination of level signals that appear at the inputs and the outputs of the delays define what is called the total state of the circuit.

166.What are the steps for the design of asynchronous sequential circuit?

1. Construction of a primitive flow table from the problem statement.
2. Primitive flow table is reduced by eliminating redundant states using the state reduction
3. State assignment is made
4. The primitive flow table is realized using appropriate logic elements.

167. Define primitive flow table :

It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.

168.What are the types of asynchronous circuits ?

1. Fundamental mode circuits
2. Pulse mode circuits

169.Give the comparison between state Assignment Synchronous circuit and state assignment asynchronous circuit.

In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.

170.What are races?

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

171.Define non critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.

172.Define critical race?

If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

173What is a cycle?

A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.

174.List the different techniques used for state assignment.

1. Shared row state assignment
2. One hot state assignment.

175.Write a short note on fundamental mode asynchronous circuit.

Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.

176. Write a short note on pulse mode circuit.

Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and the pulse width must not be so long that it is still present after the new state is reached.

177.Define secondary variables

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.

178. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to .flow. from one to another.

179. A pulse mode asynchronous machine has two inputs. If produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine.

180.What is fundamental mode.

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode.

181. Write short note on shared row state assignment.

Races can be avoided by making a proper binary assignment to the state variables. Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state variable can change at any one time when a state transition occurs. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary are said to be adjacent if they differ in only one variable.

182. Write short note on one hot state assignment.

The one hot state assignment is another method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, ie, it requires one state variable for each row of the flow table. Additional row are introduced to provide single variable changes between internal state transitions.

Unit-V

183. Explain ROM

A read only memory(ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines.

Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2_n

184. What are the types of ROM?

1.PROM

2.EPROM

3.EEPROM

185. Explain PROM.

PROM (Programmable Read Only Memory)

It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

186. Explain EPROM.

EPROM(Erasable Programmable Read Only Memory)

EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

187. Explain EEPROM.

EEPROM(Electrically Erasable Programmable Read Only Memory)

EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device.EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

189. What is RAM?

Random Access Memory. Read and write operations can be carried out.

190. Define ROM

A read only memory is a device that includes both the decoder and the OR gates within a single IC package.

191. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

192. What are the types of ROM.

1. Masked ROM.
2. Programmable Read only Memory
3. Erasable Programmable Read only memory.
4. Electrically Erasable Programmable Read only Memory.

193. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM. 194.What is mask - programmable?

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

195. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the EPLA.

196. List the major differences between PLA and PAL

PLA:

1. Both AND and OR arrays are programmable and Complex

Costlier than PAL

PAL

1. AND arrays are programmable OR arrays are fixed

Cheaper and Simpler

197. Define PLD.

Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions. 198. Give the classification of PLDs.

PLDs are classified as PROM(Programmable Read Only Memory), Programmable Logic Array(PLA), Programmable Array Logic (PAL), and Generic Array Logic(GAL)

199. Define PROM.

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

200. Define PLA

PLA is Programmable Logic Array(PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.

201. Define PAL

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

202. Why was PAL developed ?

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

203. Define GAL

GAL is Generic Array Logic. GAL consists of a programmable AND array and a fixed OR array with output logic.

204. Why the input variables to a PAL are buffered

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

205. What does PAL 10L8 specify ?

PAL - Programmable Logic
Array 10 - Ten inputs
L - Active LOW Ouput
8 - Eight Outputs

206. What is CPLD ?

CPLDs are Complex Programmable Logic Devices. They are larger versions of PLDs with a centralized internal interconnect matrix used to connect the device macro cells together.

207.Define bit, byte and word.

The smallest unit of binary data is bit. Data are handled in a 8 bit unit called byte. A complete unit of information is called a word which consists of one or more bytes.

208. How many words can a 16x8 memory can store ?

A 16x8 memory can store 16,384 words of eight bits each

209. Define address of a memory.

The location of a unit of data in a memory is called address. 210. Define Capacity of a memory.

It is the total number of data units that can be stored.

211. What is Read and Write operation ?

The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

212. Why RAMs are called as Volatile ?

RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

212.Define ROM.

ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation

213. Define RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into from any selected address in any sequence.

214. List the two categories of RAMs.

The two categories of RAMs are static RAM(SRAM) and dynamic RAM (DRAM).

215. Define Static RAM and dynamic RAM

Static RAM uses flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

216. List the two types of SRAM

1. Asynchronous SRAMs

2. Synhronous Burst SRAMs

217.List the basic types of DRAMs

Fast Page Mode DRAM,Extended Data Out DRAM(EDO DRAM),Burst EDO DRAM and Synchronous DRAM. 218. Define a bus

A bus is a set of conductive paths that serve to interconnect two or more functional components of a system or several diverse systems.

219. Define Cache memory

It is a relatively small, high-speed memory that can store the most recently used instructions or data from larger but slower main memory.

220. What is the technique adopted by DRAMs.

DRAMs use a technique called address multiplexing to reduce the number of address lines.

221.Give the feature of UV EPROM

UV EPROM is electrically programmable by the user, but the store data must be erased by exposure to ultra violet light over a period of several minutes.

222.Give the feature of flash memory.

The ideal memory has high storage capacity, non-volatility; in-system read and write capability, comparatively fast operation. The traditional memory technologies such as ROM, PROM, EEPROM individually exhibits one of these characteristics, but no single technology has all of them except the flash memory.

223.What are Flash memories ?

They are high density read/write memories that are non-volatile, which means data can be stored indefinitely with out power.

224. List the three major operations in a flash memory.

Programming, Read and Erase operation

225. What is a FIFO memory ?

The term FIFO refers to the basic operation of this type of memory in which the first data bit written into the memory is to first to be read out.

226.List basic types of programmable logic devices.

1. Read only memory
2. Programmable logic Array
3. Programmable Array Logic

227. Define ROM

A read only memory is a device that includes both the decoder and the OR gates within a single IC package.

228.Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

229. What are the types of ROM ?

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minterms as in the
ROM. 301.What is
mask - programmable?

With a mask programmable PLA, the user must submit a PLA PLA program table to the

manufacturer.

302.Give the comparison between PROM and PLA.

PROM	PLA
And array is fixed and OR array is programmable.	Both AND and OR arrays are Programmable.
Cheaper and simple to use.	Costliest and complex than PROMS.