UNIT-1
Lecture-6

Device parameters; DC Analysis of 741

THE DEVICE PARAMETERS

For the standard *npn* and *pnp* transistors, the following parameters will be used:

pnp: $I_s = 10^{-14}$ A, $\beta = 50$, $V_A = 50$ V

- In 741 circuit the nonstandard devices are Q_{13}, Q_{14} and Q_{20}.
- For transistor Q_{13}, $I_{SA} = 0.25 \times 10^{-14}$ A $\quad I_{SB} = 0.75 \times 10^{-14}$ A,
- Transistors Q_{14} and Q_{20} have an area three time that of a standard device.

DC ANALYSIS OF 741

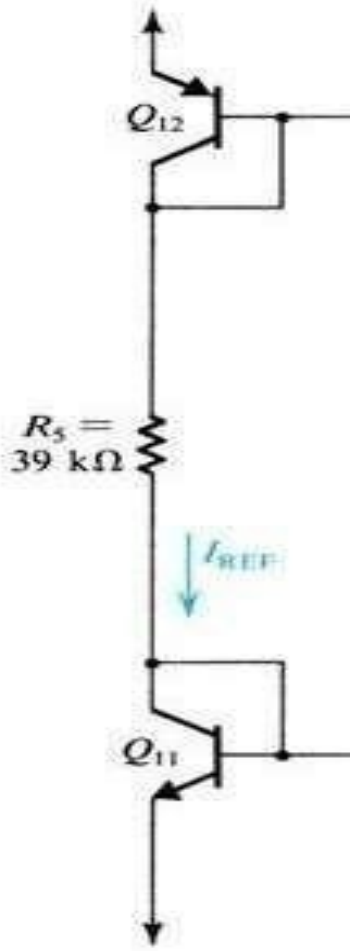
For the dc analysis of an op-amp circuit, the Input terminals are grounded.

- This should result in zero dc voltage at the output.
- However, because the op amp has very large gain, the output voltage is close to either $+V_{CC}$ or $-V_{EE}$.
- To overcome this problem In the dc analysis, it will be assumed that the op amp is connected in a negative feedback loop that stabilizes the output dc voltage to zero volts.

REFERENCE BIAS CURRENT

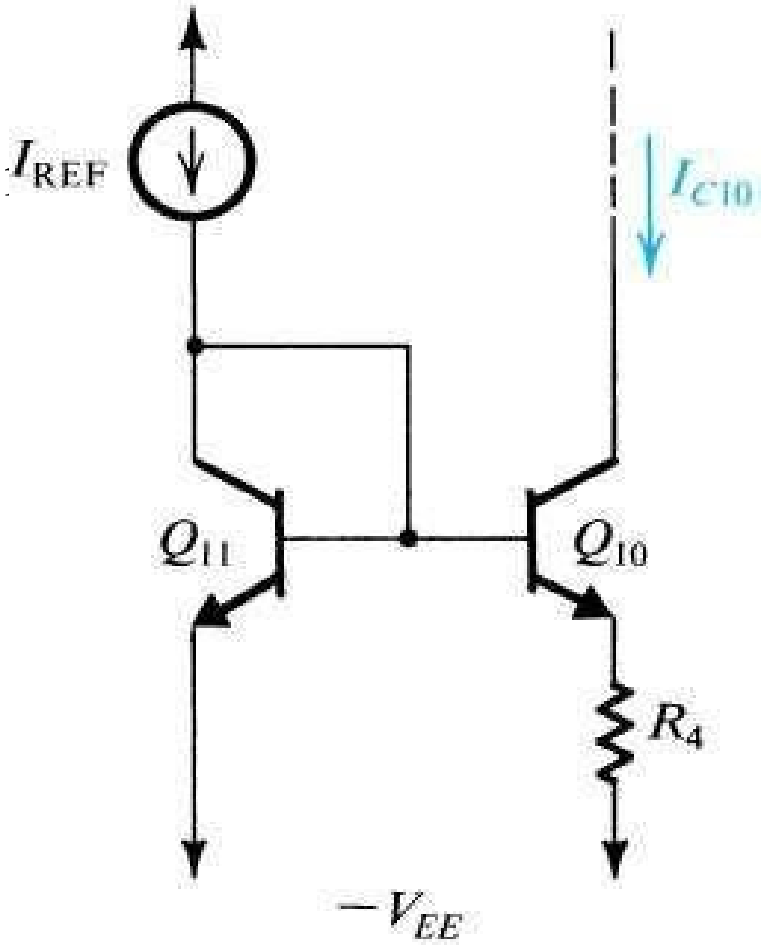
The reference Bias current I_{REF} can be obtained as:

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$



INPUT-STAGE BIAS

Transistor Q_{11} is biased by I_{REF}, and the voltage developed across is used to bias Q_{10} which has a series emitter resistance R_4.



Now we can determine dc current in each of the input-stage transistors.

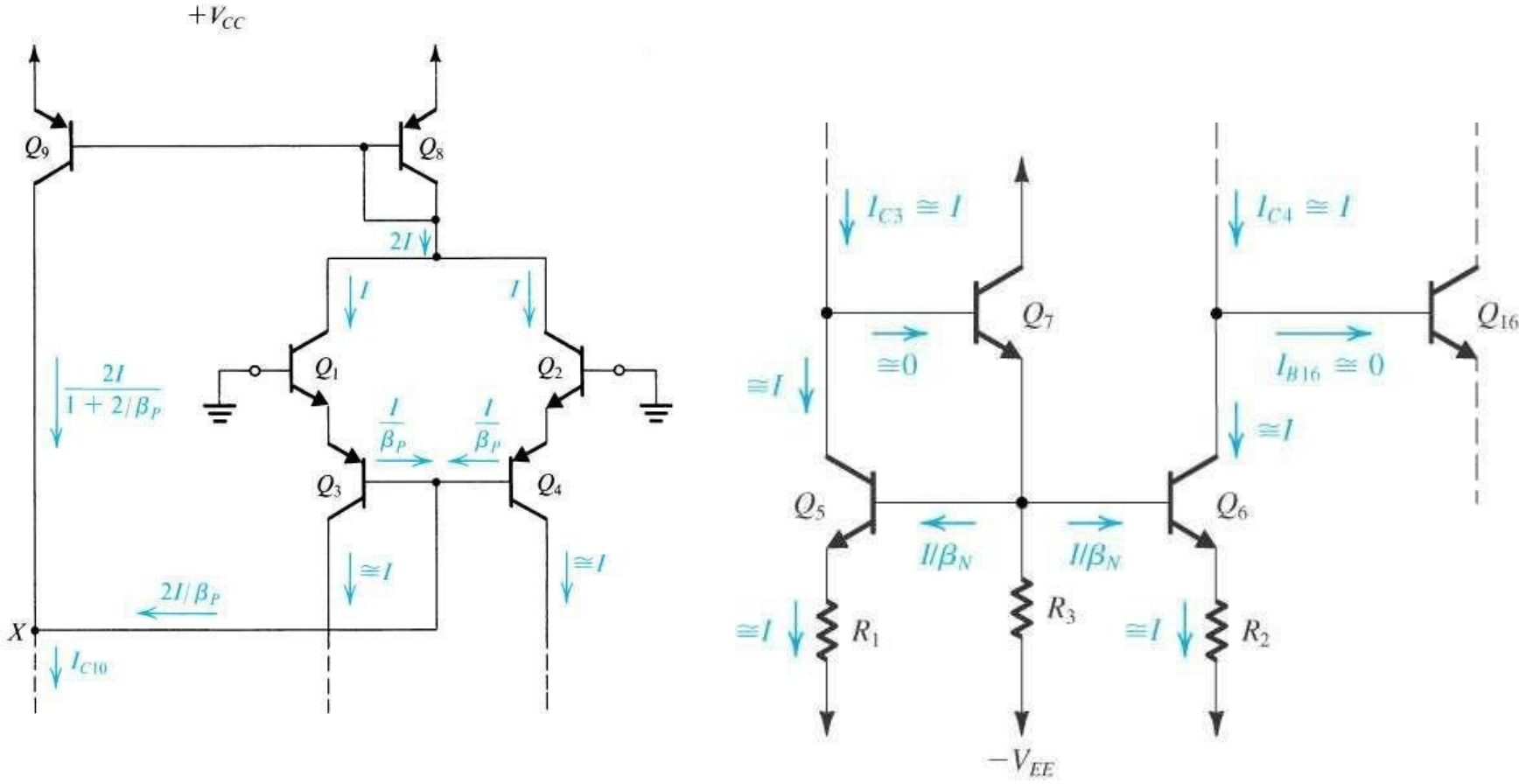


Figure: The dc analysis of the 741 input stage.

INPUT BIAS AND OFFSET CURRENTS

- Because of possible mismatches in the β values of Q_1 and Q_2 the input base currents will not be equal.

- In this case, input offset current is defined as,

$$I_B = I_{B1} - I_{B2}$$