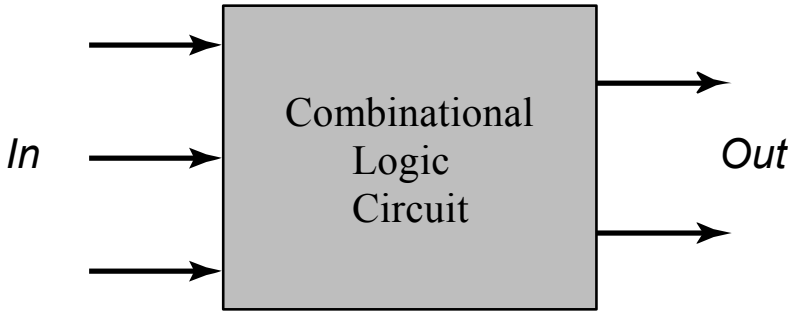
UNIT-3
Lecture-2

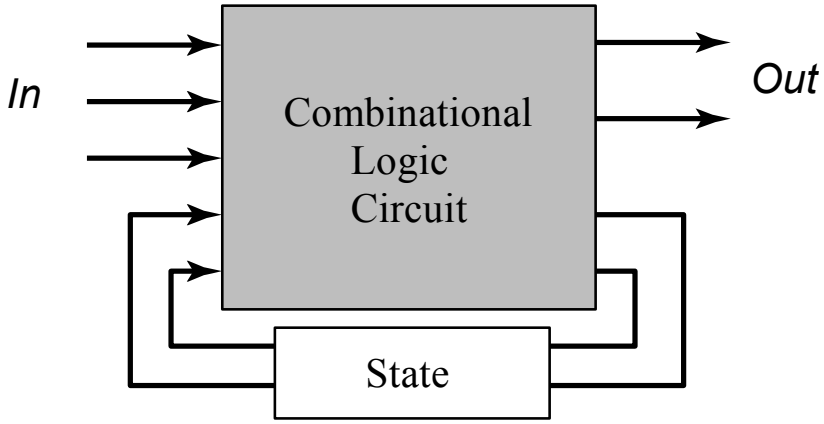
AND, OR, NAND and NOR Gates

Combinational vs. Sequential Logic



Combinational

Output = *f*(*In*)

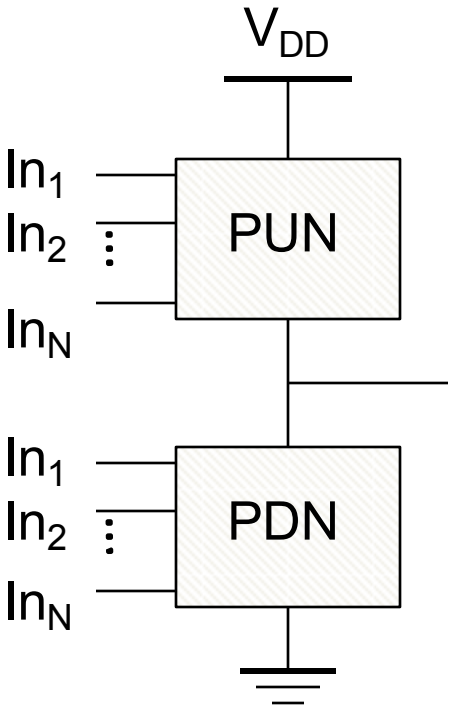


Sequential

Output = *f*(*In*, *Previous In*)

Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

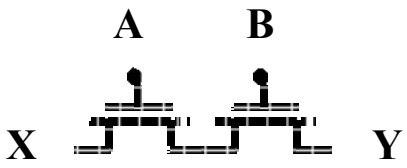
NMOS transistors only

PUN and PDN are dual logic networks

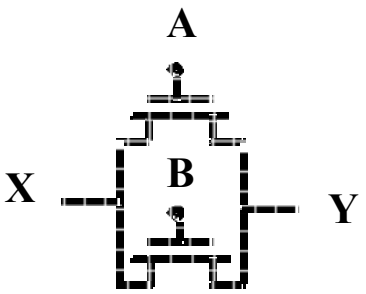
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

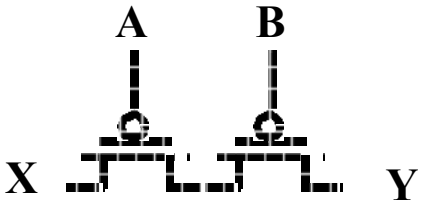


Y = X if A OR B

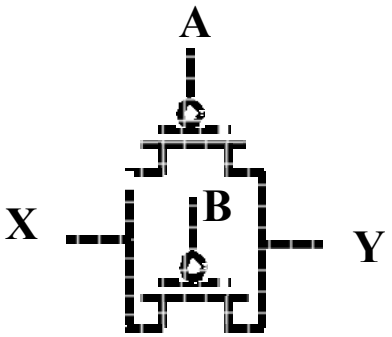
NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



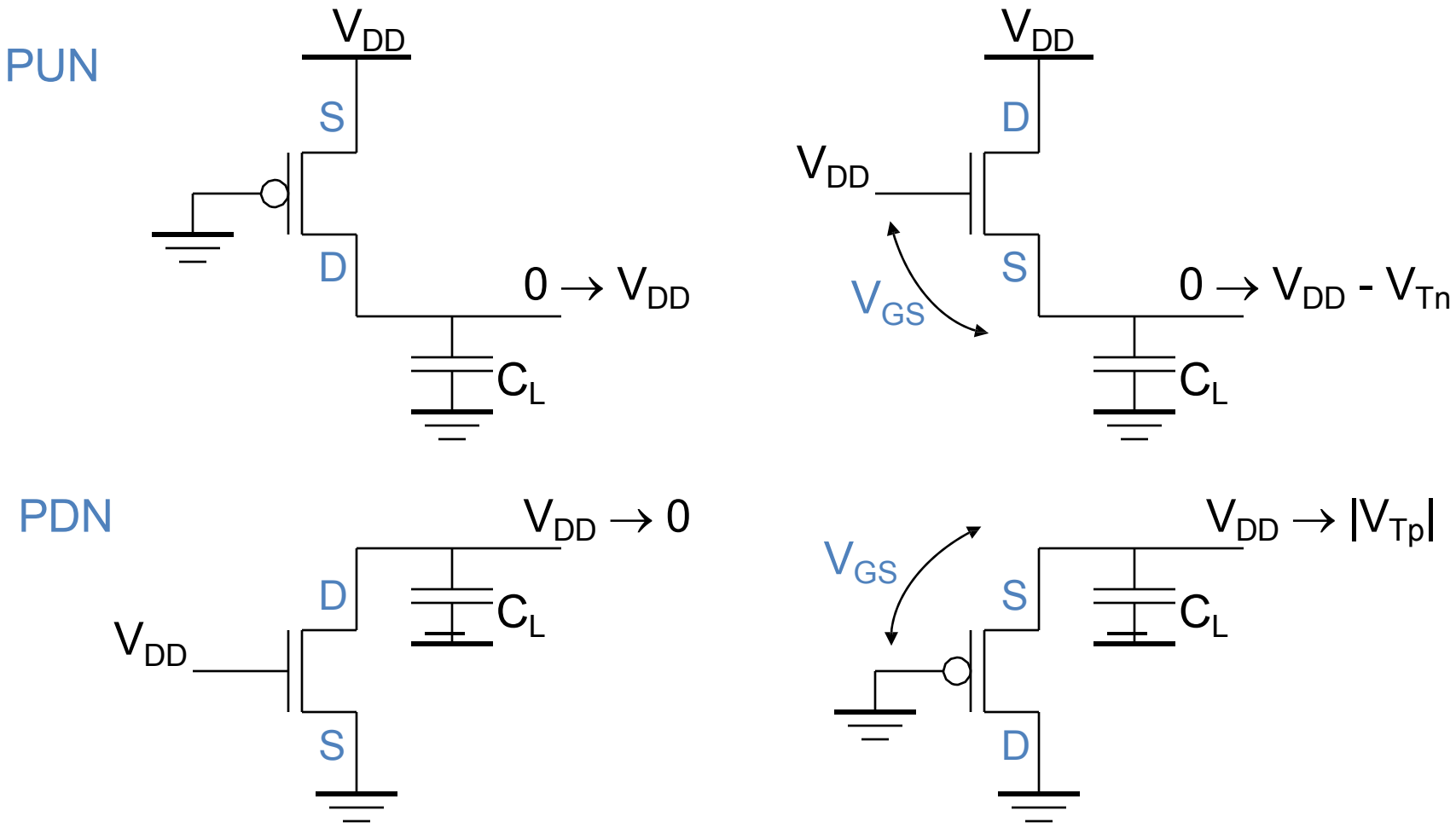
$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$



$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

Threshold Drops



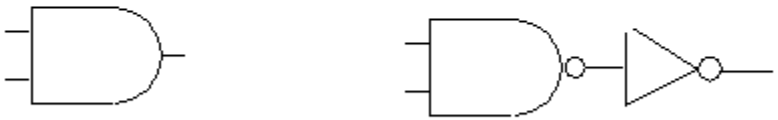
Complementary CMOS Logic Style

- **PUP is the DUAL of PDN**
  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- **The complementary gate is inverting**



AND = NAND + INV