UNIT-3
Lecture-5

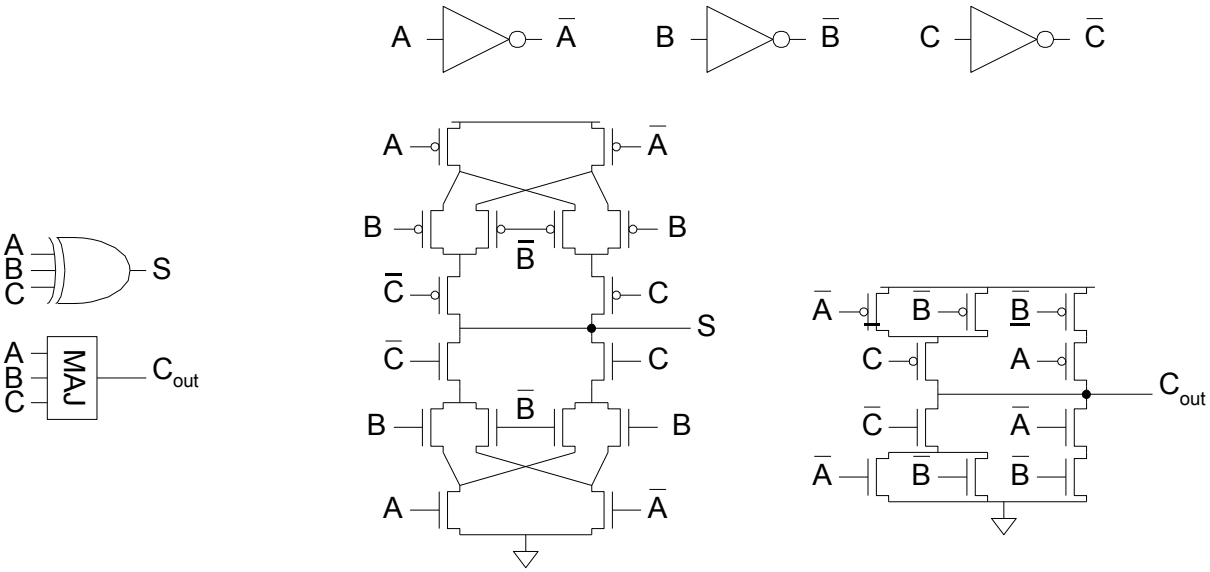
Combinational Circuits

Full Adder Design I

- Brute force implementation from eqns

$$S = A \oplus B \oplus C$$

$$C_{out} = MAJ(A, B, C)$$



Carry-Skip Adder

- Carry-ripple is slow through all N stages
- Carry-skip allows carry to skip over groups of n bits
  - Decision based on n-bit propagate signal