# Microprocessor memory & I/O devices

# Lecture 4

Dronacharya Group of Institutions

# The Design and Operation of Memory

Memory in a microprocessor system is where information (data and instructions) is kept.

It can be classified into two main types:

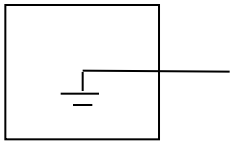
- Main memory (RAM and ROM)
- Storage memory (Disks , CD ROMs, etc.)
- The simple view of RAM is that it is made up of registers that are made up of flip-flops (or memory elements).
- The number of flip-flops in a "memory register" determines the size of the memory word.
- ROM on the other hand uses diodes instead of the flip-flops to permanently hold the information.

# Accessing Information in Memory

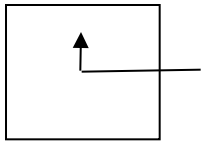
- For the microprocessor to access (Read or Write) information in memory (RAM or ROM), it needs to do the following:
  - Select the right memory chip (using part of the address bus).
  - Identify the memory location (using the rest of the address bus).
  - Access the data (using the data bus).

# Tri-State Buffers

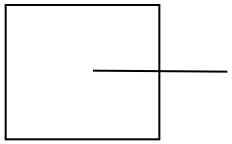
- An important circuit element that is used extensively in memory.
- This buffer is a logic circuit that has three states:
  - Logic 0, logic1, and high impedance.
  - When this circuit is in high impedance mode it looks as if it is disconnected from the output completely.



The Output is Low



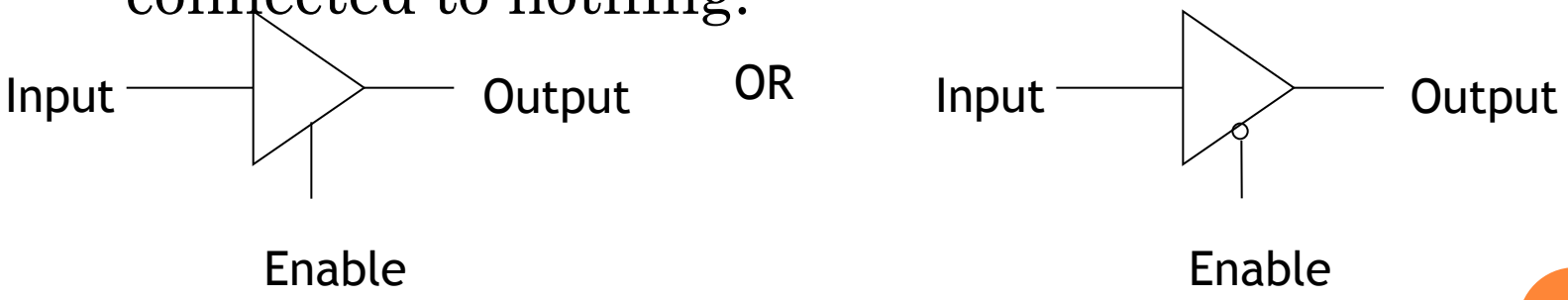
The Output is High



High Impedance

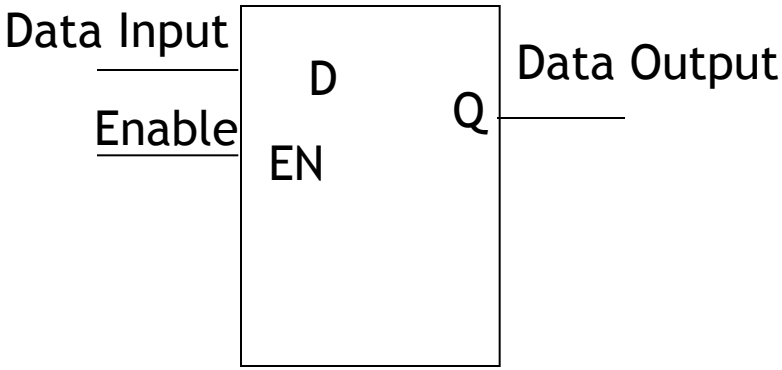
# The Tri-State Buffer

- This circuit has two inputs and one output.
  - The first input behaves like the normal input for the circuit.
  - The second input is an "**enable**".
    - If it is set high, the output follows the proper circuit behavior.
    - If it is set low, the output looks like a wire connected to nothing.



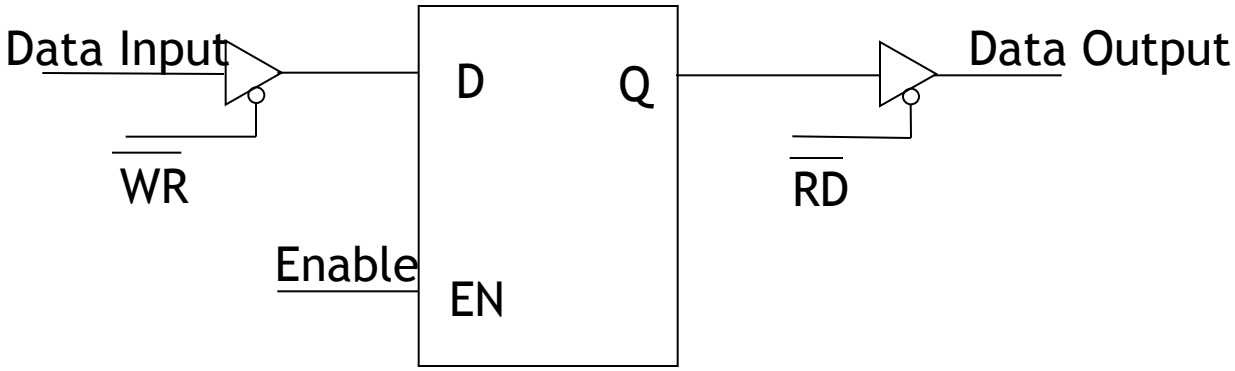
# The Basic Memory Element

- The basic memory element is similar to a D latch.
- This latch has an input where the data comes in. It has an enable input and an output on which data comes out.



# The Basic Memory Element

- However, this is not safe.
  - Data is always present on the input and the output is always set to the contents of the latch.
  - To avoid this, tri-state buffers are added at the input and output of the latch.

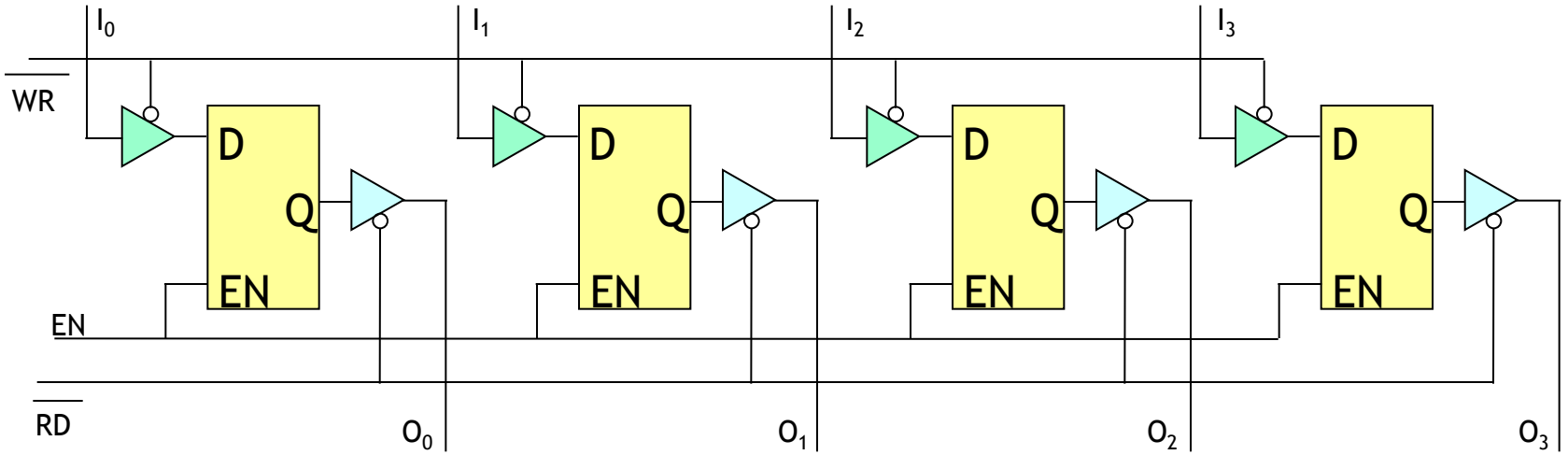


# The Basic Memory Element

- The WR signal controls the input buffer.
  - The bar over WR means that this is an active low signal.
  - So, if WR is 0 the input data reaches the latch input.
  - If WR is 1 the input of the latch looks like a wire connected to nothing.
- The RD signal controls the output in a similar manner.

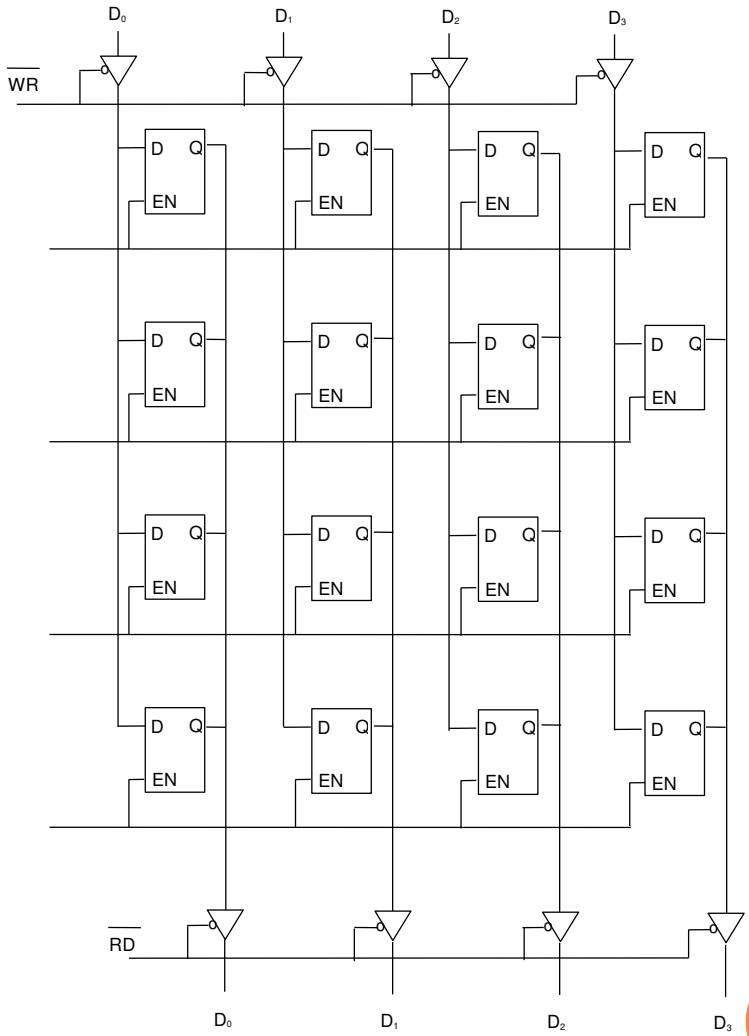
# A Memory "Register"

- If we take four of these latches and connect them together, we would have a 4-bit memory register



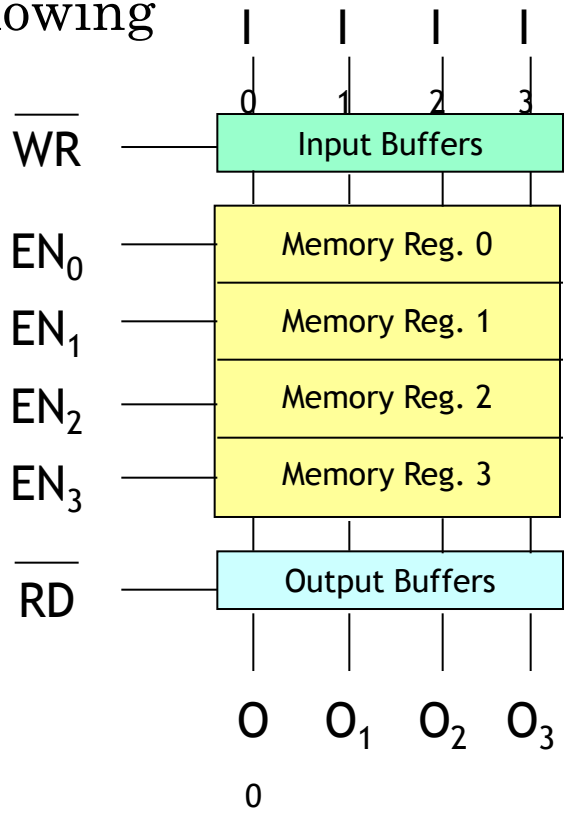
# A GROUP OF MEMORY REGISTERS

Expanding on this scheme to add more memory registers we get the diagram to the right.



# A GROUP OF MEMORY REGISTERS

- If we represent each memory location (Register) as a block we get the following



# The Design of a Memory Chip

- Using the RD and WR controls we can determine the direction of flow either into or out of memory. Then using the appropriate Enable input we enable an individual memory register.

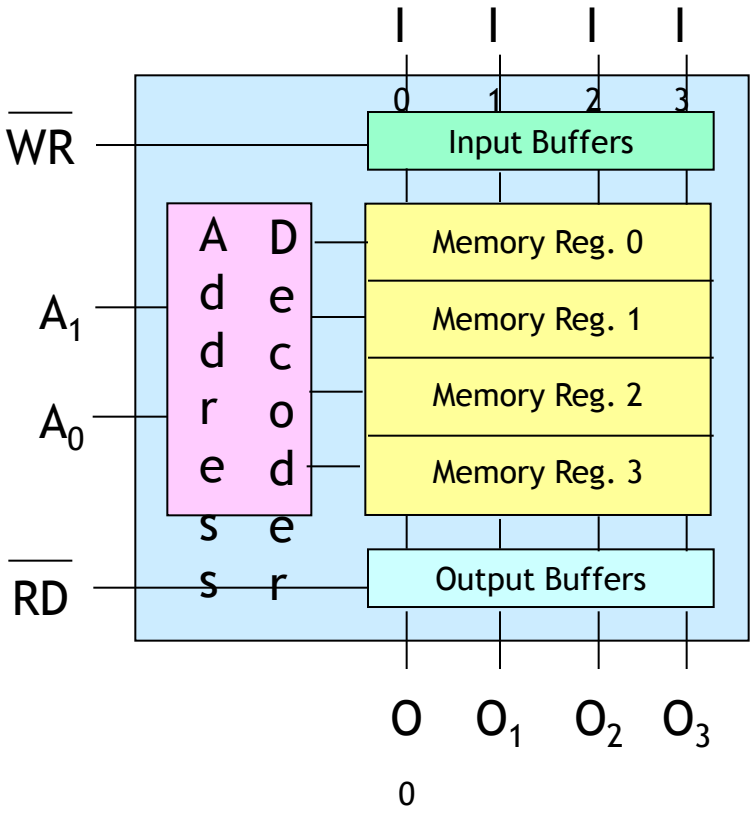
- What we have just designed is a memory with 4 locations and each location has 4 elements (bits). This memory would be called 4 X 4 [Number of location X number of bits per location].

# The Enable Inputs

- How do we produce these enable line?
  - Since we can never have more than one of these enables active at the same time, we can have them encoded to reduce the number of lines coming into the chip.
  - These encoded lines are the address lines for memory.

# The Design of a Memory Chip

- So, the previous diagram would now look like the following:



# The Design of a Memory Chip

- Since we have tri-state buffers on both the inputs and outputs of the flip flops, we can actually use one set of pins only.
  - The chip would now look like this: