# Memory Interfacing Lecture 8

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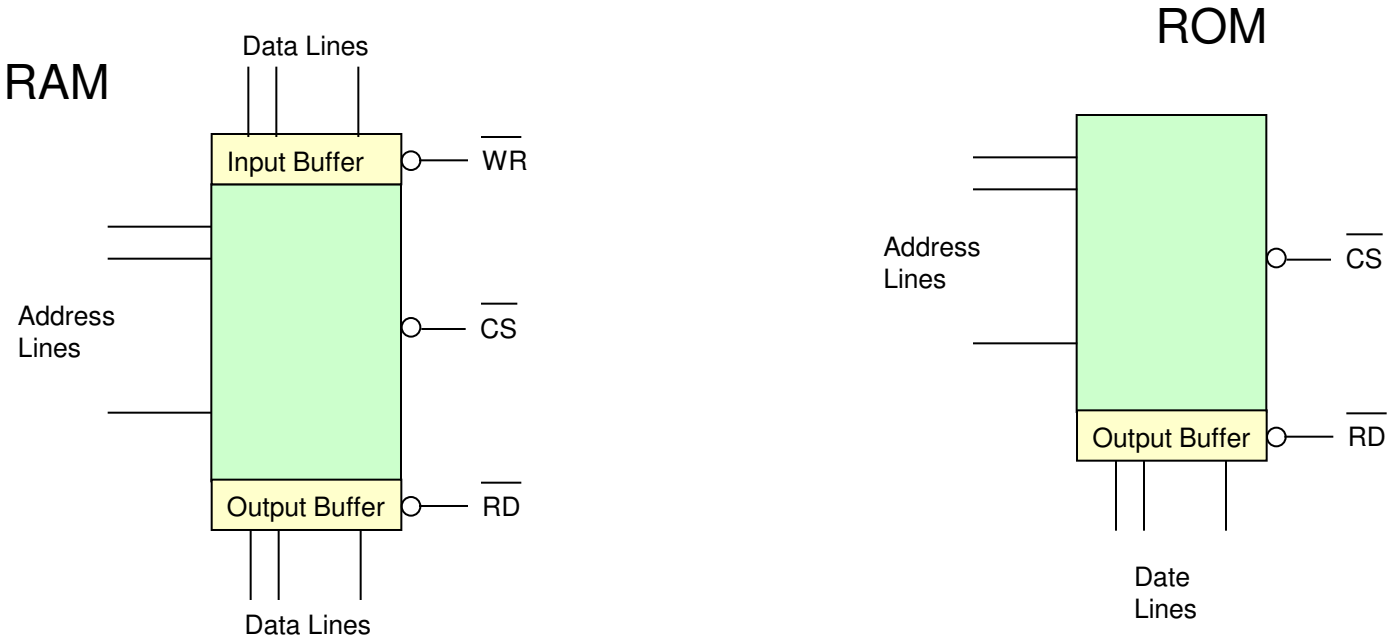
# Memory interfacing

- There needs to be a lot of interaction between the microprocessor and the memory for the exchange of information during program execution.
  - Memory has its requirements on control signals and their timing.
  - The microprocessor has its requirements as well.
- The interfacing operation is simply the matching of these requirements.

# Memory structure & its requirements




- The way of interfacing the above two chips to the microprocessor is the same.
  - However, the ROM does not have a WR signal.

# Interfacing Memory

- Accessing memory can be summarized into the following three steps:
- Select the chip.
- Identify the memory register.
- Enable the appropriate buffer.

- Translating this to microprocessor domain:
- The microprocessor places a 16-bit address on the address bus.
- Part of the address bus will select the chip and the other part will go through the address decoder to select the register.
- The signals IO/M and RD combined indicate that a memory read operation is in progress. The MEMR signal can be used to enable the RD line on the memory chip.

# Control and Status Signals

**TABLE 4.1**

8085 Machine Cycle Status and Control Signals

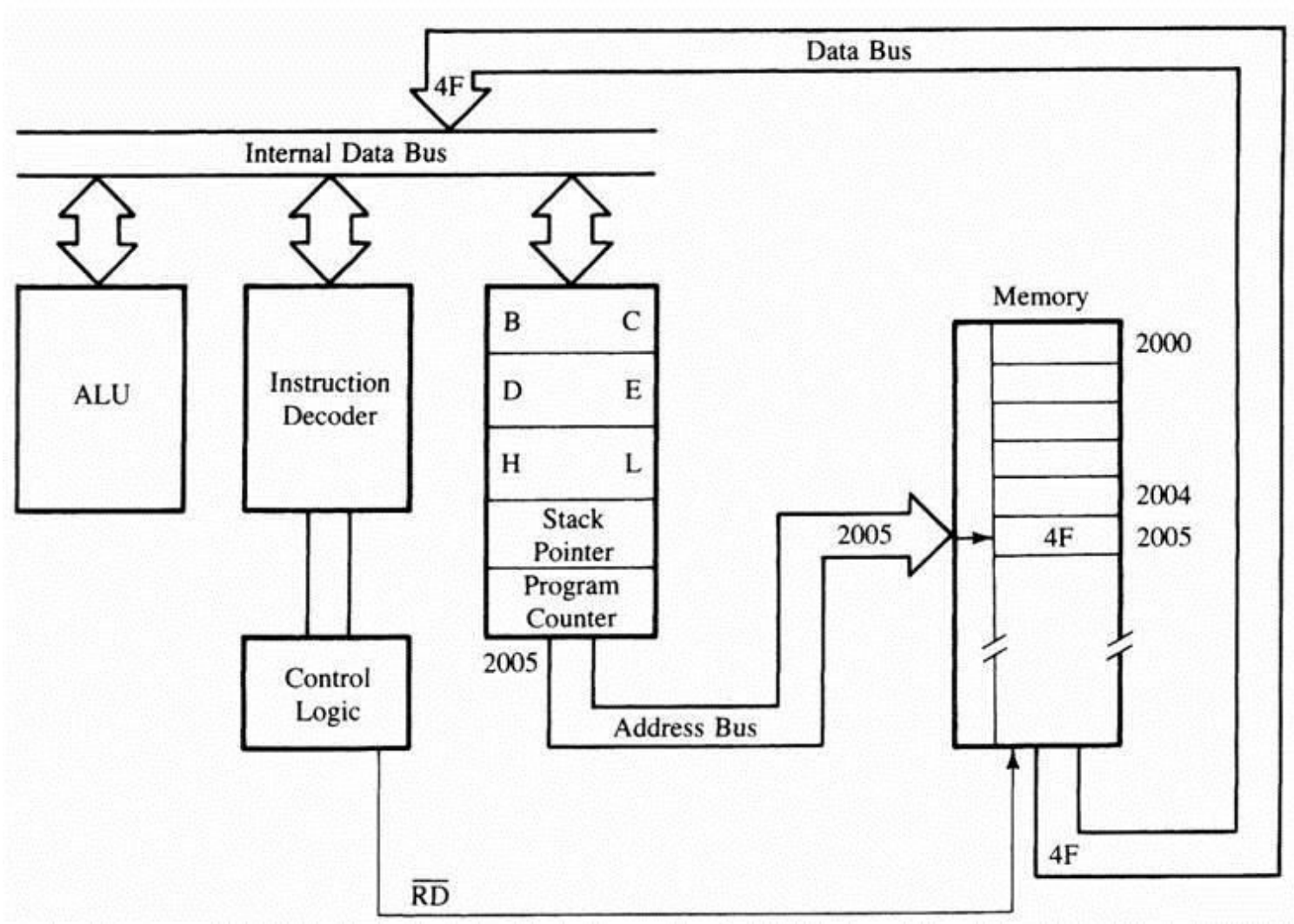
| Machine Cycle | Status | | | Control Signals |
|---|---|---|---|---|
| | IO/$\overline{M}$ | $S_1$ | $S_0$ | |
| Opcode Fetch | 0 | 1 | 1 | $\overline{RD} = 0$ |
| Memory Read | 0 | 1 | 0 | $\overline{RD} = 0$ |
| Memory Write | 0 | 0 | 1 | $\overline{WR} = 0$ |
| I/O Read | 1 | 1 | 0 | $\overline{RD} = 0$ |
| I/O Write | 1 | 0 | 1 | $\overline{WR} = 0$ |
| Interrupt Acknowledge | 1 | 1 | 1 | $\overline{INTA} = 0$ |
| Halt | Z | 0 | 0 | $\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA} = 1$ |
| Hold | Z | X | X | |
| Reset | Z | X | X | |

NOTE: Z = Tri-state (high impedance)
X = Unspecified

# Direct Memory Access (DMA)

- DMA is an IO technique where external IO device requests the use of the MPU buses.
- Allows external IO devices to gain high speed access to the memory.
  - Example of IO devices that use DMA: disk memory system.
- HOLD and HLDA are used for DMA.
- If HOLD=1, 8085 will place it address, data and control pins at their high-impedance.
- A DMA acknowledgement is signaled by HLDA=1.

# MPU Communication and Bus Timing



# MPU Communication and Bus Timing

- The Fetch Execute Sequence :
  1. The µp placed a 16 bit memory address from PC (program counter) to address bus.
     - Figure 4: at T1
       - The high order address, 20H, is placed at A15 – A8.
       - the low order address, 05H, is placed at AD7 - AD0 and ALE is active high.
       - Synchronously the IO/M is in active low condition to show it is a memory operation.
  2. At T2 the active low control signal, RD, is activated so as to activate read operation; it is to indicate that the MPU is in fetch mode operation.

# MPU Communication and Bus Timing

3. T3: The active low RD signal enabled the byte instruction, 4FH, to be placed on AD7 – AD0 and transferred to the MPU. While RD high, the data bus will be in high impedance mode.
4. T4: The machine code, 4FH, will then be decoded in instruction decoder. The content of accumulator (A) will then copied into C register at time state, T4.

# MPU Communication and Bus Timing