Basic Interfacing Concepts(cont.) Lecture 2

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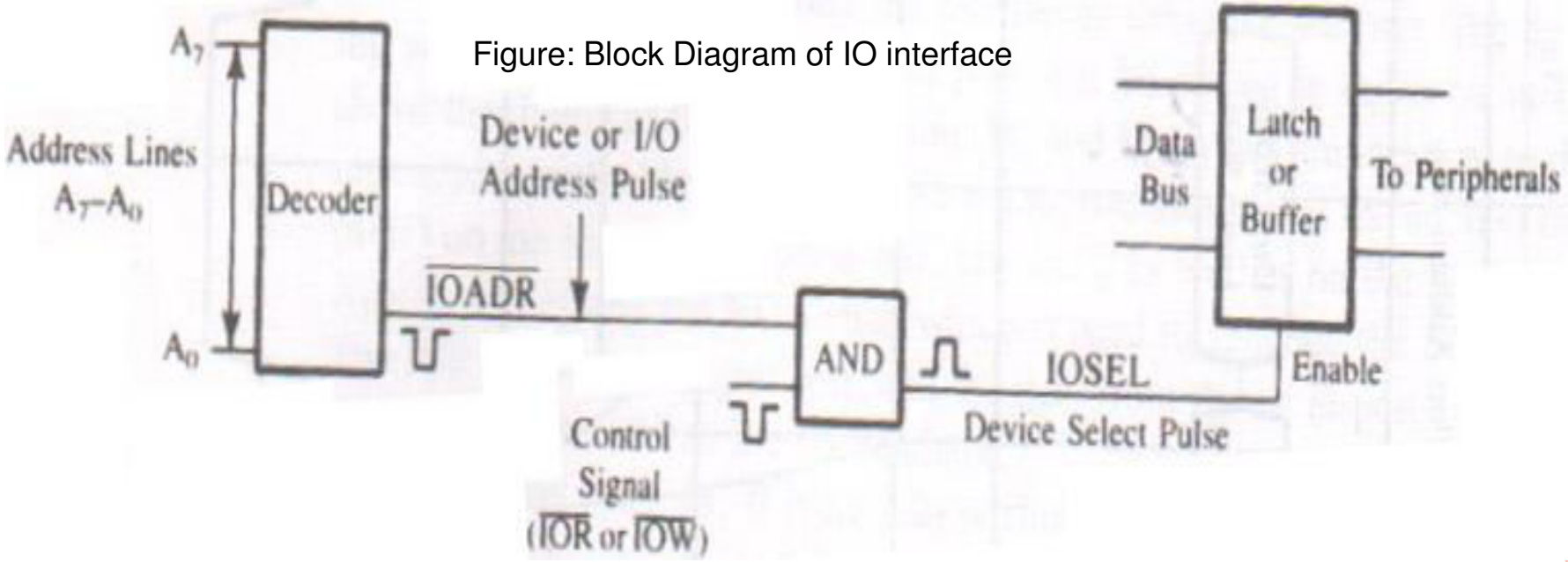
DEVICE SELECTION AND DATA TRANSFER

Steps are summarized as:

- Decode the address bus to generate unique pulse corresponding to device address on the bus called device address bus or I/O address pulse.
- Combine the device address pulse with the control signal to generate a device select pulse(I/O select) that is generated only when both signals are asserted.
- Use the I/O select pulse to activate interfacing device(I/O port).

Figure: Block Diagram of IO interface



Device Selection and Data Transfer

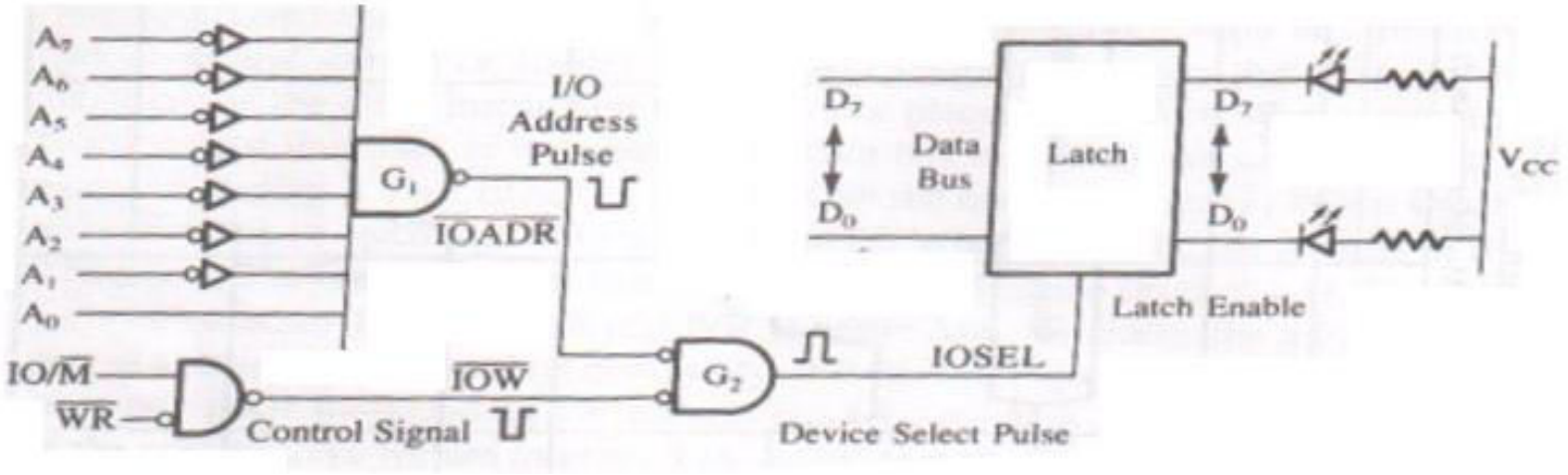


Figure: Practical decoding circuit for the output device with address 01H

- Address lines A7-A0 are connected to 8-input NAND gate that functions as decoder (A0-Directly connected; A7-A1 with inverters).
- When Address bus is carries 01H, gate G1 generated a low pulse otherwise output remain high.
- G1 and G2 are combined to generate I/O select pulse which clocks data (AC content on data bus available for few microsecond) into latch for display by LEDs.

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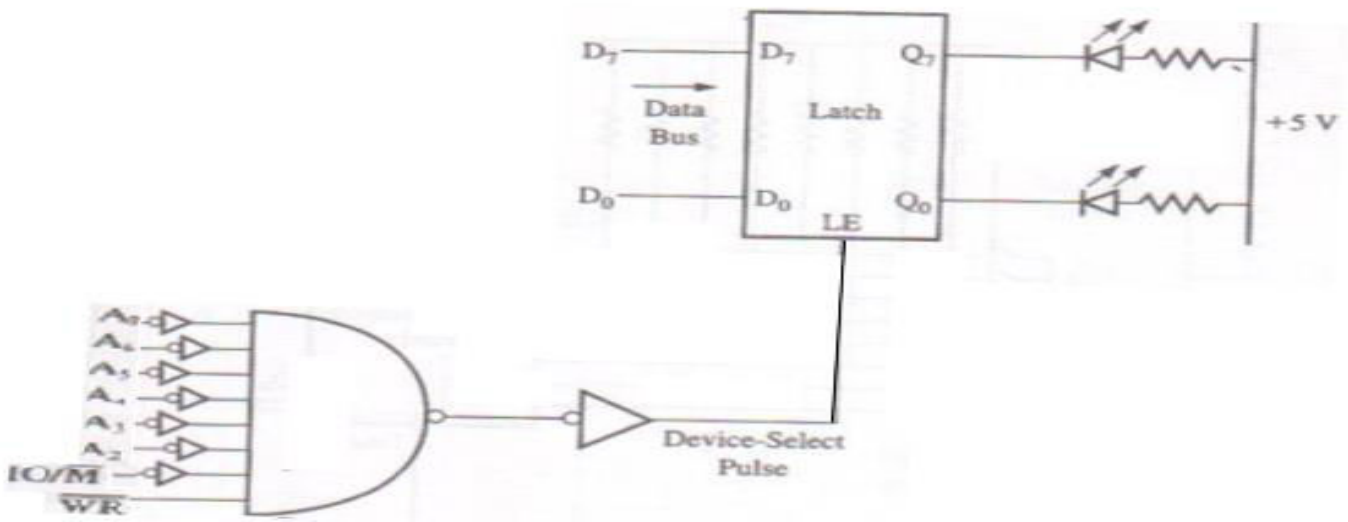
Absolute Vs Partial Decoding

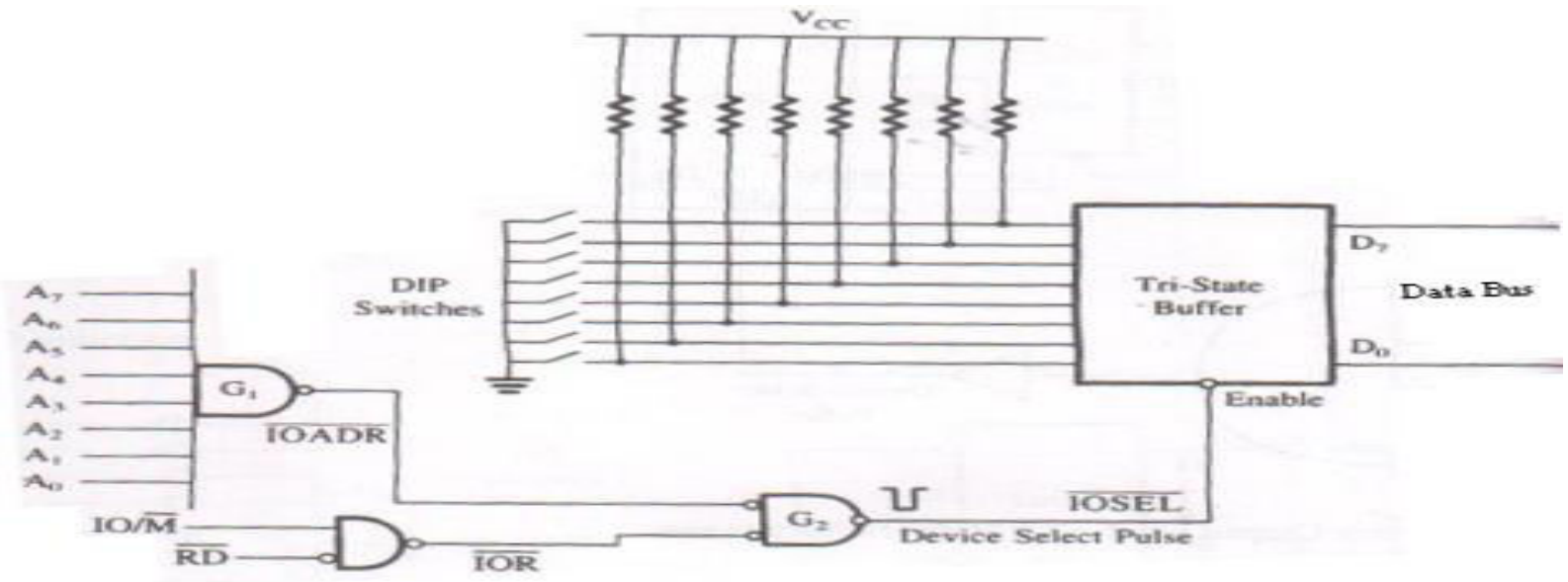
- All eight lines are decoded to generate one unique pulse called absolute decoding like device will be selected only with the address 01H(good design practice).
- To minimize the cost, the output port can be selected by decoding some address lines called partial decoding (device has multiple addresses).
- A1 and A0 are at don't care logic level so output port can access by address 00, 01, 02 and 03(commonly used techniques in small systems).



Partial Decoding Output Latch with Multiple Addresses

INPUT INTERFACING

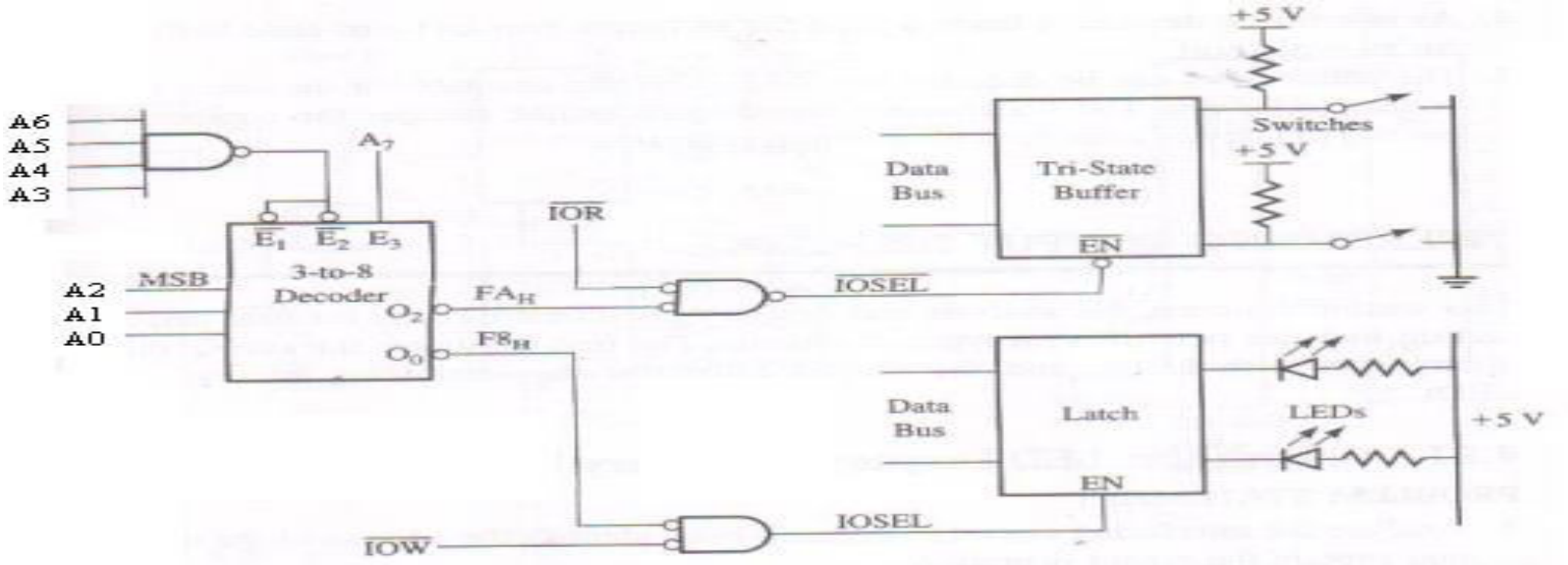
Decode logic for a Dip-Switch Input Port



- Address lines are high(FFH), output of NAND gate goes low which is combined by control signal IOR' which generates Device Select Pulse.

- Device select pulse enable Tri-state Buffer (used as interfacing port). Data flow from keys to the AC.

Interfacing I/O Using Decoders



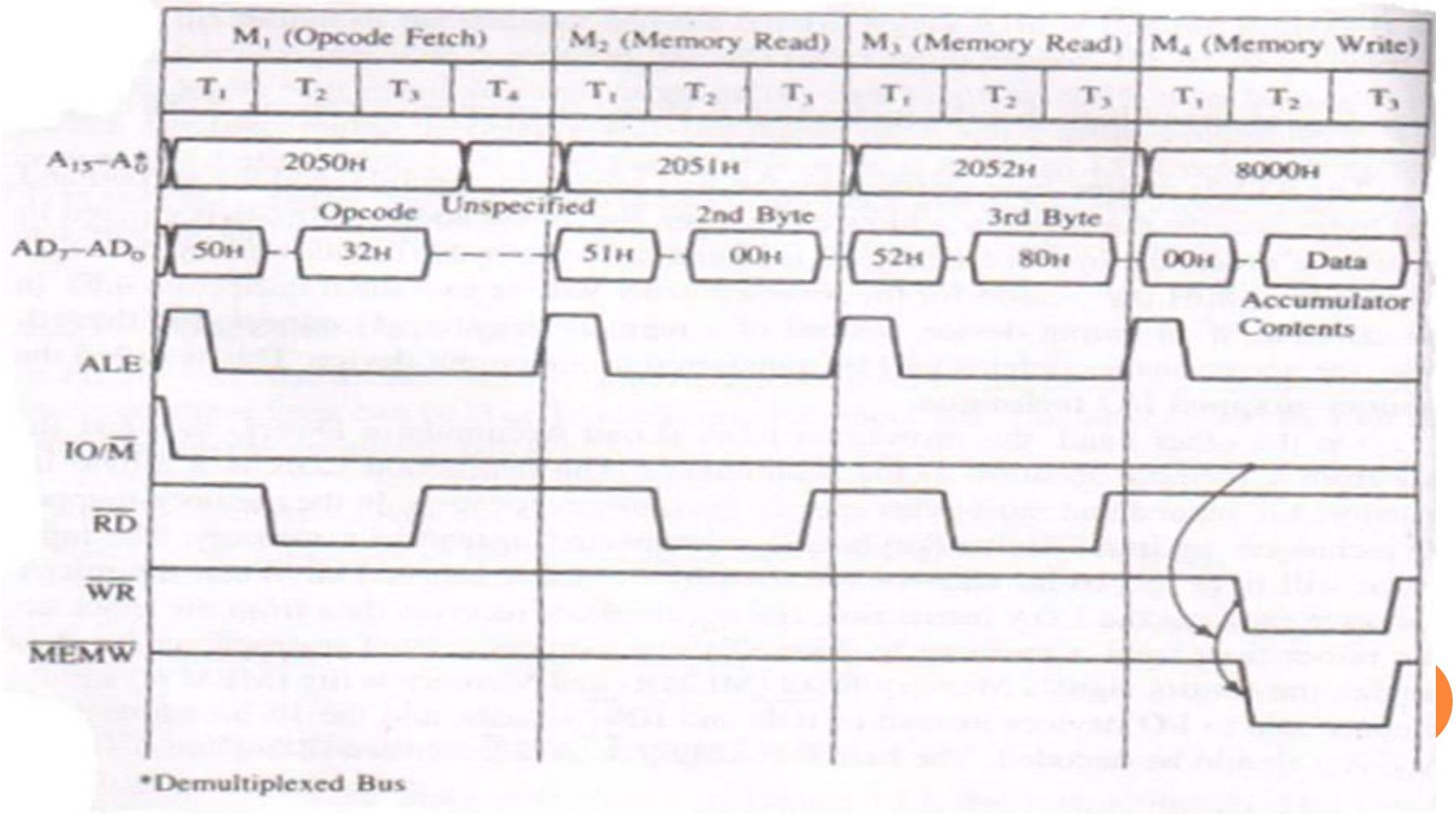
- First Step is to decode the address bus using 3x8 Decoder and 4-input NAND gate. A0 to A2 are used as input and remaining A3 to A7 are used to enable decoder.
- Second step is to decode address with appropriate control signal (IOR'/IOW') output will generate select pulse.
- Third step is to use this pulse to enable I/O port (pulse enables LED latch with the output port address F8H similarly input buffer is enable with address FAH).

Memory Mapped I/O

- Instead of using 8-bit address, the full 16-bits of the address bus must be used.
- Instead of using IORD and IOWR, use MEMR and MEMW.
- To transfer data Memory Related Instructions such as LDA(Load AC Direct transfers data from memory to Accumulator), STA (Store contents of AC into Memory)are used.
- IN STA 8000H output device instead of a memory Register is connected to the address, so that accumulator contents will be transferred to output device.

MEMORY MAPPED I/O

IN LDA 8000H accumulator receives data from input device rather than Memory. Execution of Memory Related data Transfer Instruction STA 8000H



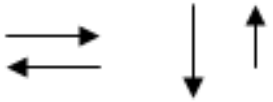
Flow Chart Symbols

Terminal

Input/output

Process

Flow lines



Decision

Connector

Predefined process

Flow Chart Steps