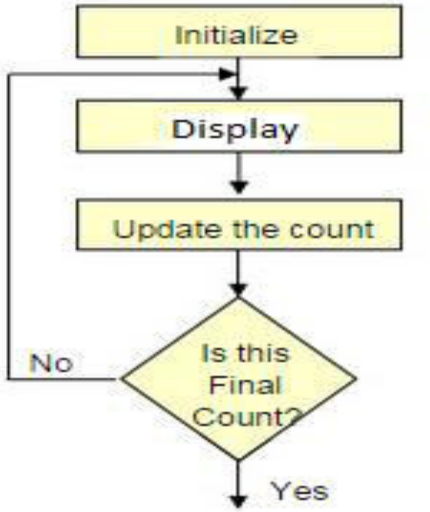
COUNTERS AND TIME DELAYS

LECTURE 3

Dronacharya Group of Institutions

Counter and Time Delays

- A counter is designed simply by loading appropriate number into one of the registers and using INR or DNR instructions.
- Loop is established to update the count.
- Each count is checked to determine whether it has reached final number ;if not, the loop is repeated.

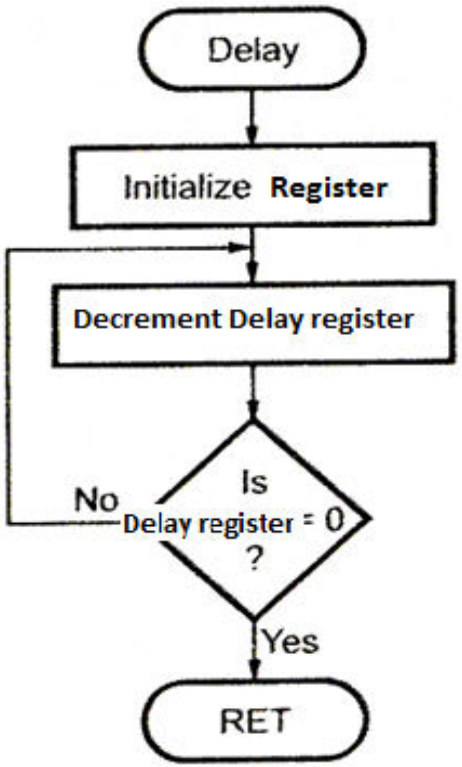


Time Delay

- Procedure used to design a specific delay.
- A register is loaded with a number , depending on the time delay required and then the register is decremented until it reaches zero by setting up a loop with conditional jump instruction.

- **Time delay using**

  One register:



Label Opcode Operand Comments T states

```
        MVI     C,FFH    ;Load register  C     7
LOOP:   DCR     C        ;Decrement C          4
        JNZ     LOOP     ;Jump back to         10/7
                          decrement C
```

Clock frequency of the system = 2 MHz

Clock period= 1/T= 0.5 µs

Time to execute MVI = 7 T states * 0.5= 3.5 µs

Time Delay in Loop T_L= T*Loop T states * N_{10}

= 0.5 * 14* 255

= 1785 µs = 1.8 ms

N_{10} = Equivalent decimal number of hexadecimal count loaded in the delay register

T_{LA}= Time to execute loop instructions

=T_L –(3T states* clock period)=1785-1.5=1783.5 µs

Time Delay using a register pair

Label	Opcode	Operand	Comments	T states
	LXI	B,2384H	Load BC with 16-bit count	10
LOOP:	DCX	B	Decrement BC by 1	**6**
	MOV	A,C	Place contents of C in A	**4**
	ORA	B	OR B with C to set Zero flag	**4**
	JNZ	LOOP	if result not equal to 0 , jump back to loop	**10**/7

Time Delay in Loop T_L= T*Loop T states * N_{10}

= 0.5 * 24* 9092

= 109 ms

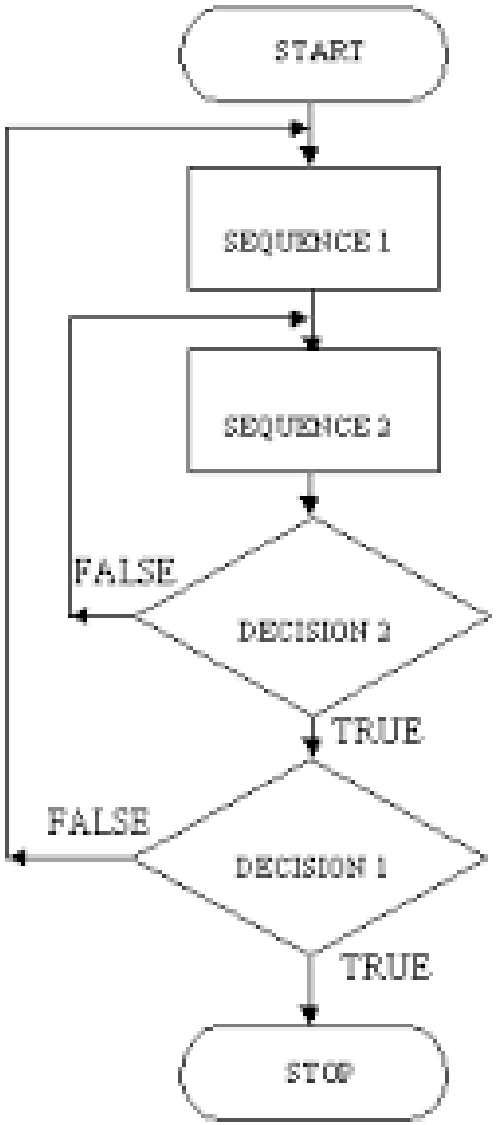
Time Delay using a LOOP within a LOOP

	MVI B,38H	7T
LOOP2:	MVI C,FFH	**7T**
LOOP1:	DCR C	4T
	JNZ LOOP1	10/7 T
	DCR B	**4T**
	JNZ LOOP 2	**10**/7T

Delay in Loop T_{L1}=1783.5 µs

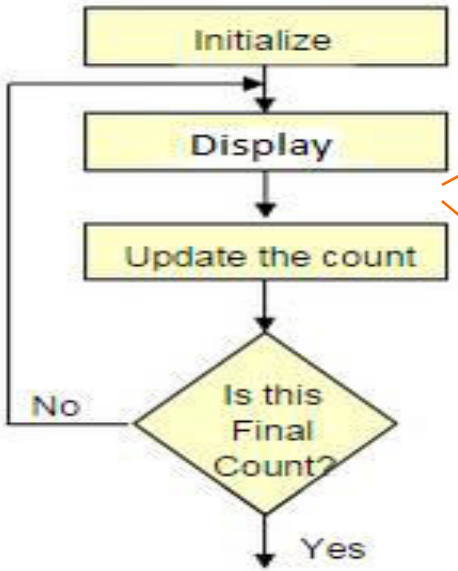
Delay in Loop T_{L2}= (0.5*21+T_{L1})*56

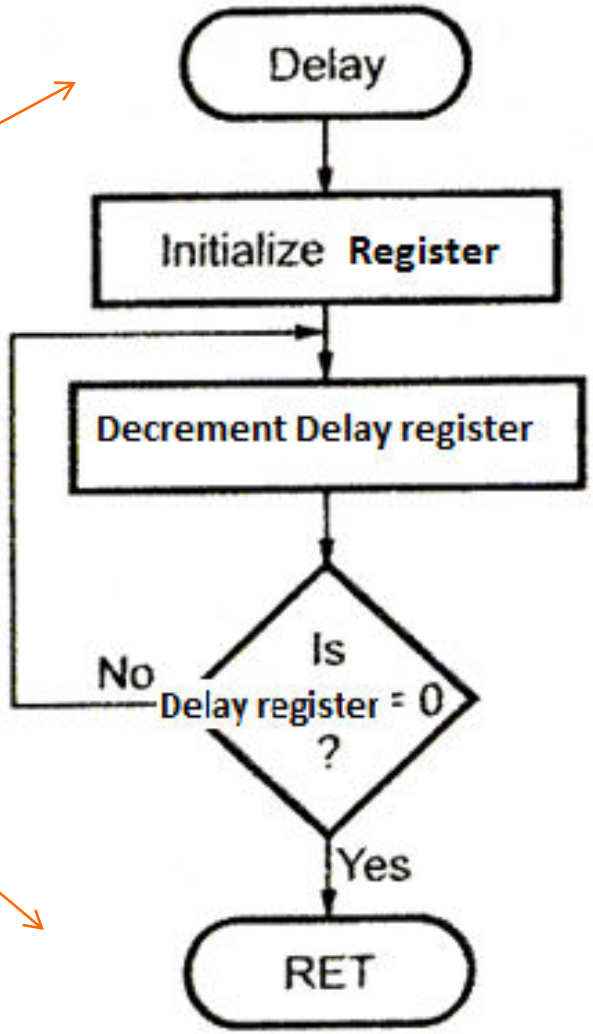
=100.46ms



Flowchart for time delay with two loops

Flowchart of a counter with time delay

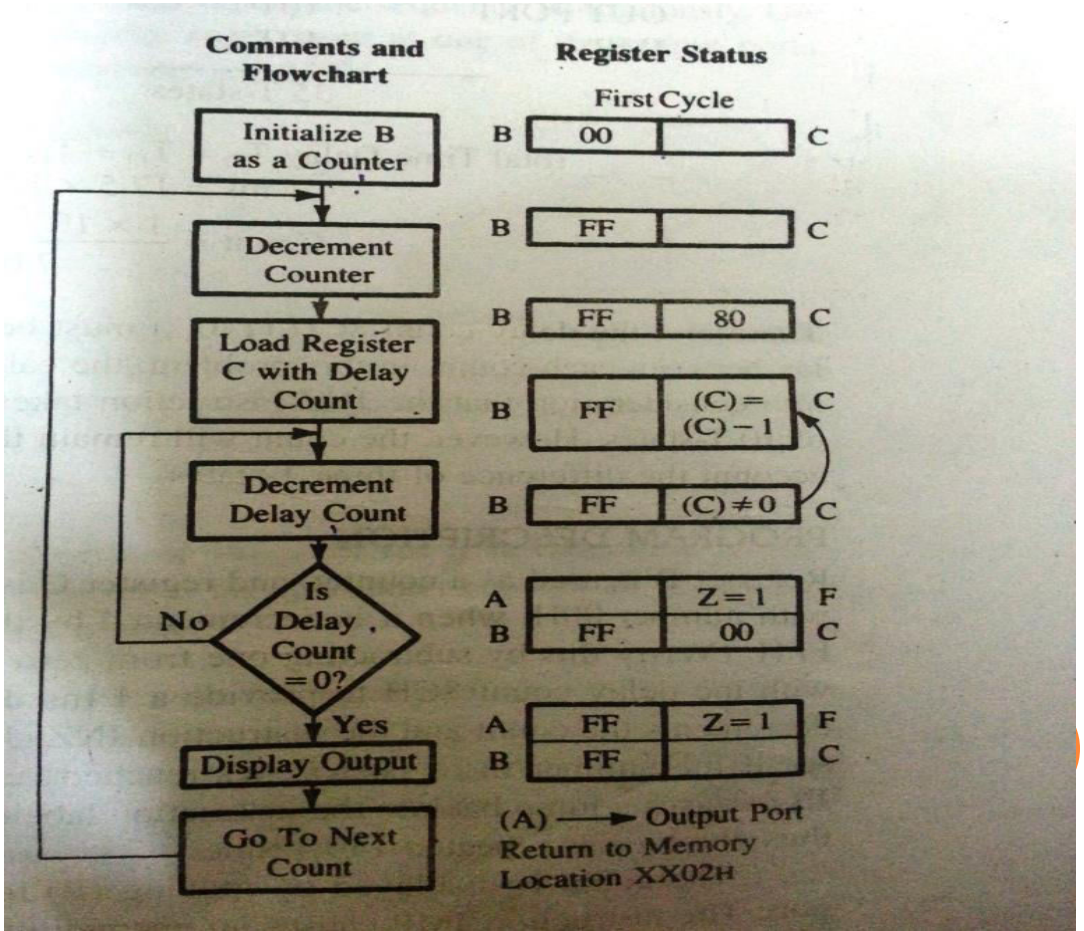




Illustrative Program: Hexadecimal Counter

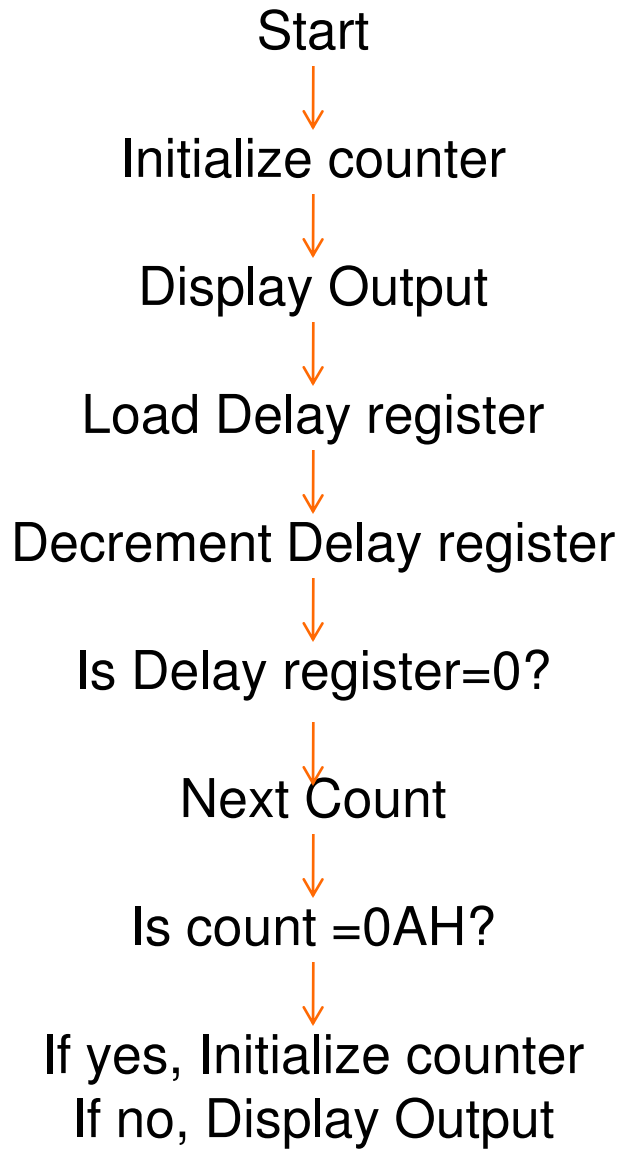
Write a Program to count continuously from FFH to 00H using register C with delay count 8CH between each count and display the number at one of the output ports.

```
        MVI B,00H
NEXT:   DCR B
        MVI C,8CH
DELAY:  DCR C
        JNZ DELAY
        MOV A,B
        OUT PORT#
        JMP NEXT
```



Illustrative Program: Zero to nine (Modulo ten) Counter

```
START:   MVI B,00H
         MOV A,B
DSPLAY:  OUT  PORT #
         LXI H,16-bit
LOOP:    DCX H
         MOV A,L
         ORA H
         JNZ LOOP
         INR B
         MOV A,B
         CPI 0AH
         JNZ DSPLAY
         JZ START
```



Illustrative Program: Generating pulse waveforms

```
      MVI D, AAH
X:    MOV A, D
      RLC
      MOV D, A
      ANI 01H
      OUT PORT1
      MVI B, COUNT
Y:    DCR B
      JNZ Y
      JMP X
```

- Generates a continuous square wave with the period of 500 Micro Sec. Assume the system clock period is 325ns, and use bit D0 output the square wave.
- Delay outside loop: T0=46 T states * 325=14.95 micro sec.
- Loop delay: T_L=4.5 micro sec
- Total Td=To+T_L

Count=34 H

Debugging Counter and time delay programs

- It is designed to count from 100(base 10) to 0 in Hex continuously with a 1 second delay between each count.
- The delay is set up using two loops. The inner loop is executed to provide approximately 100ms delay and is repeated 10 times, using outer loop to provide a total delay of 1 second.
- The clock period of system is 330ns.

MVI A, 64H	7
X: OUT PORT1	10
Y:MVI B, 10H	7
Z:LXI D, X	10
DCX D	6
NOP	4
NOP	4
MOV A, D	4
ORA E	4
JNZ Z	10/7
DCR B	4
JZ Y	10/7
DCR A	4
CPI 00H	7
JNZ X	10/7

Delay in loop1=32T X count x $330x10^{-9}$

100ms =32T X count x $330x10^{-9}$

Count=9470