8086 Microprocessor Register Organization LECTURE 7

Dronacharya Group of Institutions

8086 Programmer's Model

BIU registers
(20 bit adder)

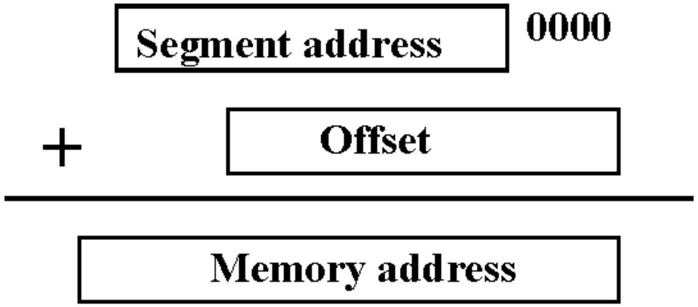
Register	Name
ES	Extra Segment
CS	Code Segment
SS	Stack Segment
DS	Data Segment
IP	Instruction Pointer

EU registers
16 bit arithmetic

	High	Low	Name
AX	AH	AL	Accumulator
BX	BH	BL	Base Register
CX	CH	CL	Count Register
DX	DH	DL	Data Register
	SP		Stack Pointer
	BP		Base Pointer
	SI		Source Index Register
	DI		Destination Index Register
	FLAGS		

Memory Address Calculation

- ❑ Segment addresses must be stored in segment registers
- ❑ Offset is derived from the combination of pointer registers, the Instruction Pointer (IP), and immediate values



Segment address 0000

+ Offset

Memory address

- ❑ Examples

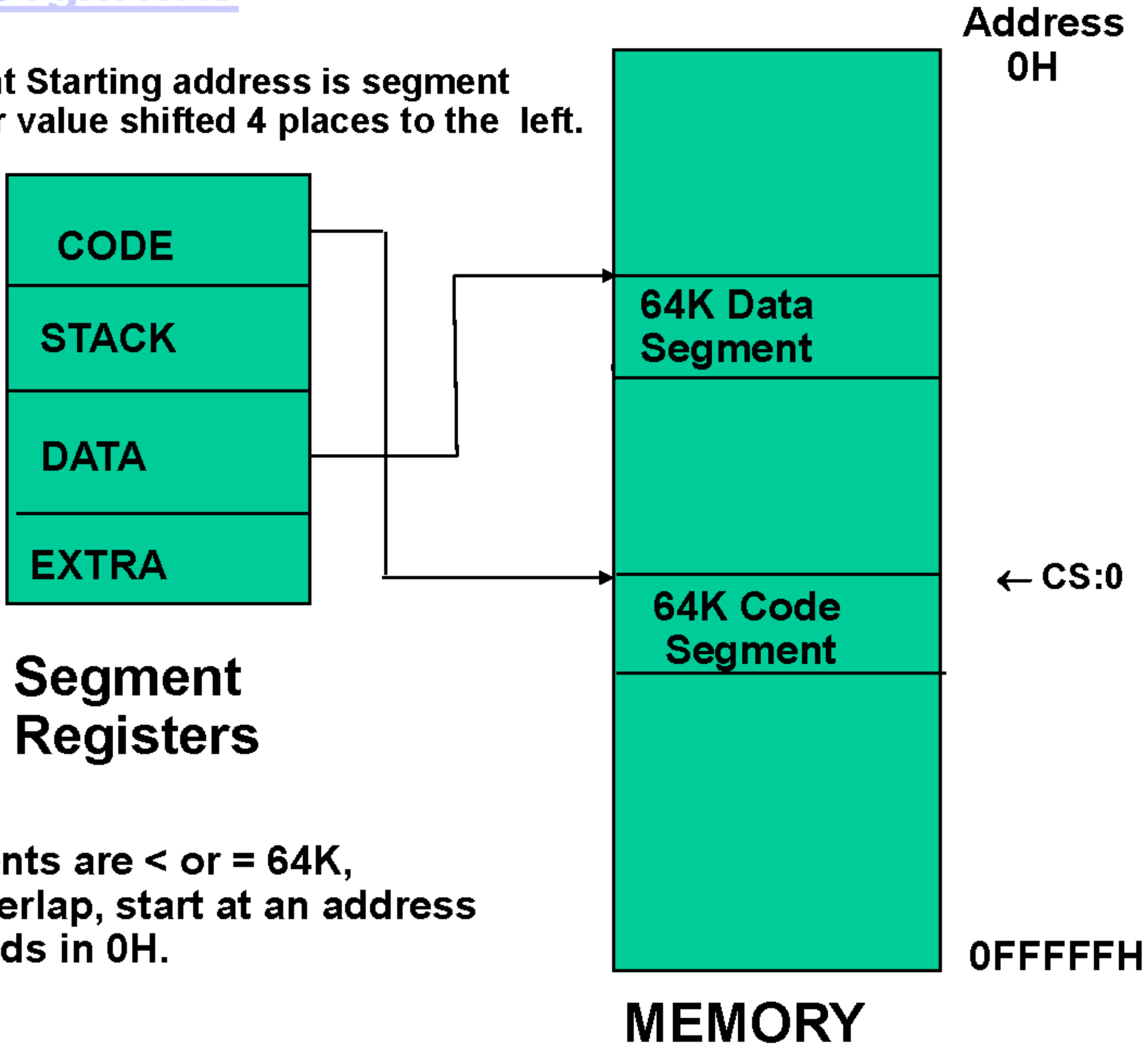
CS	3	4	8	A	0
IP +		4	2	1	4
Instruction address	3	8	A	B	4

SS	5	0	0	0	0
SP +		F	F	E	0
Stack address	5	F	F	E	0

DS	1	2	3	4	0
DI +		0	0	2	2
Data address	1	2	3	6	2

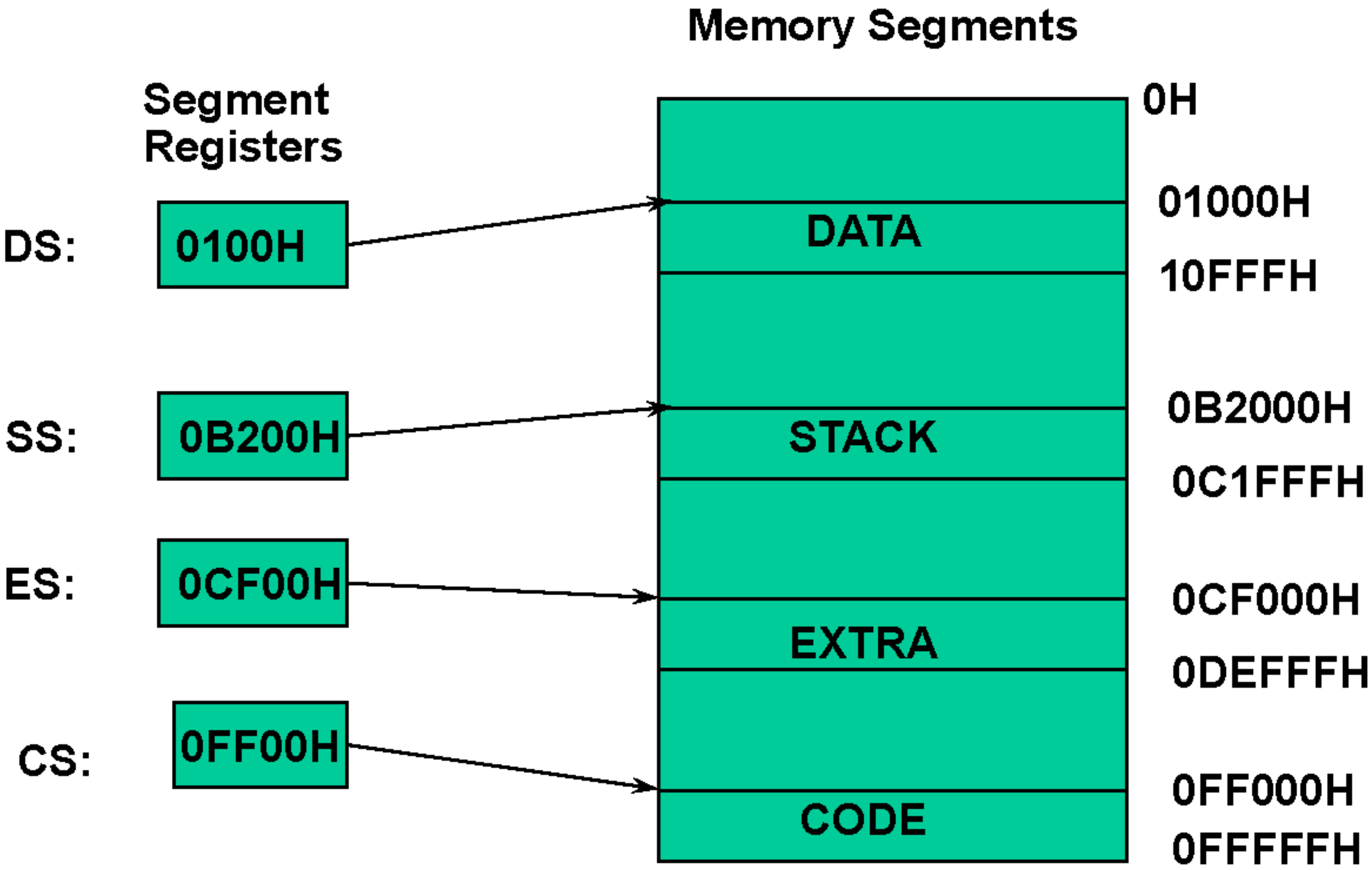
Segments

Segment Starting address is segment register value shifted 4 places to the left.



Segments are < or = 64K, can overlap, start at an address that ends in 0H.

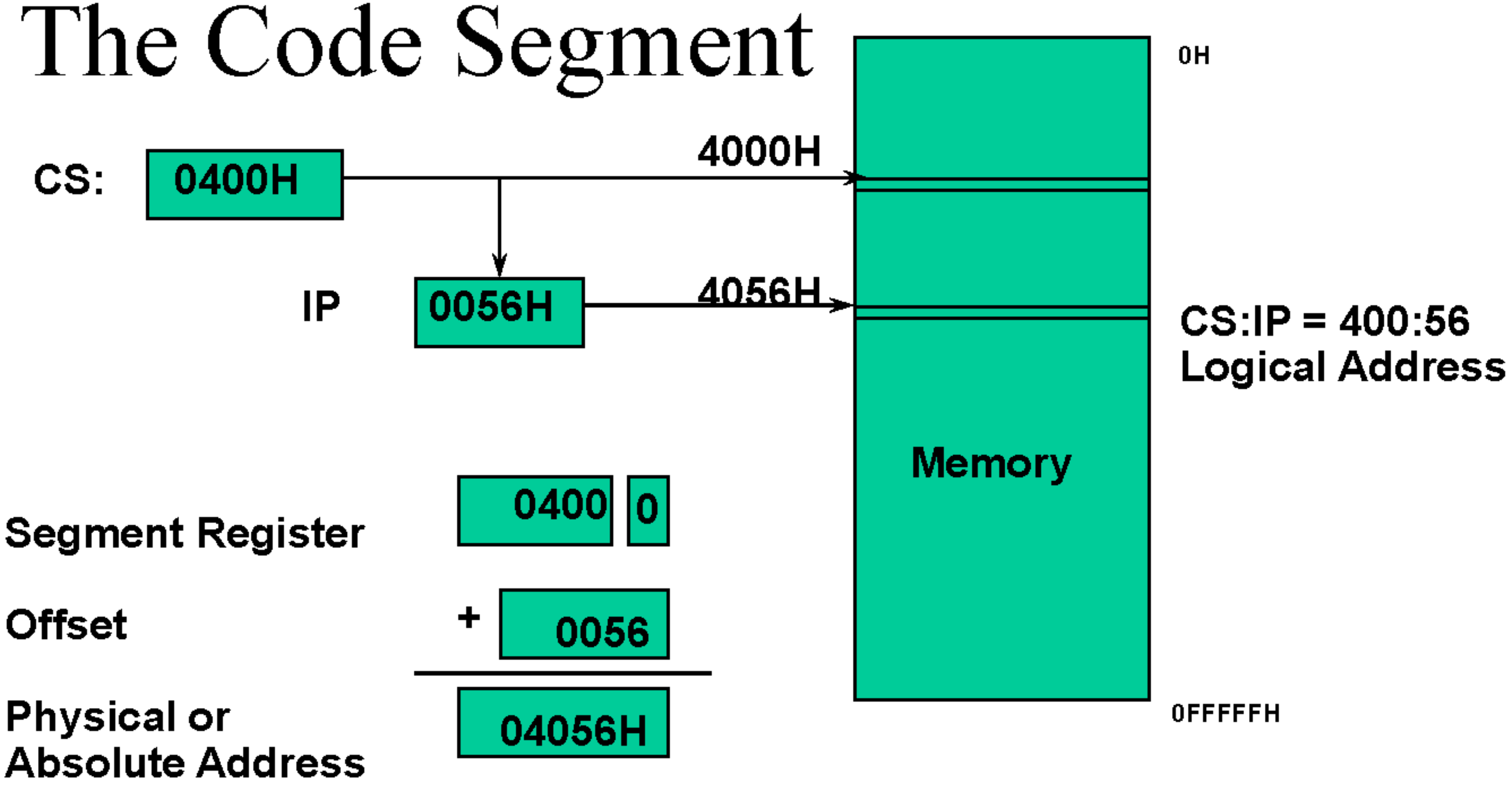
8086 Memory Terminology



Segments are < or = 64K and can overlap.

Note that the Code segment is < 64K since 0FFFFFH is the highest address.

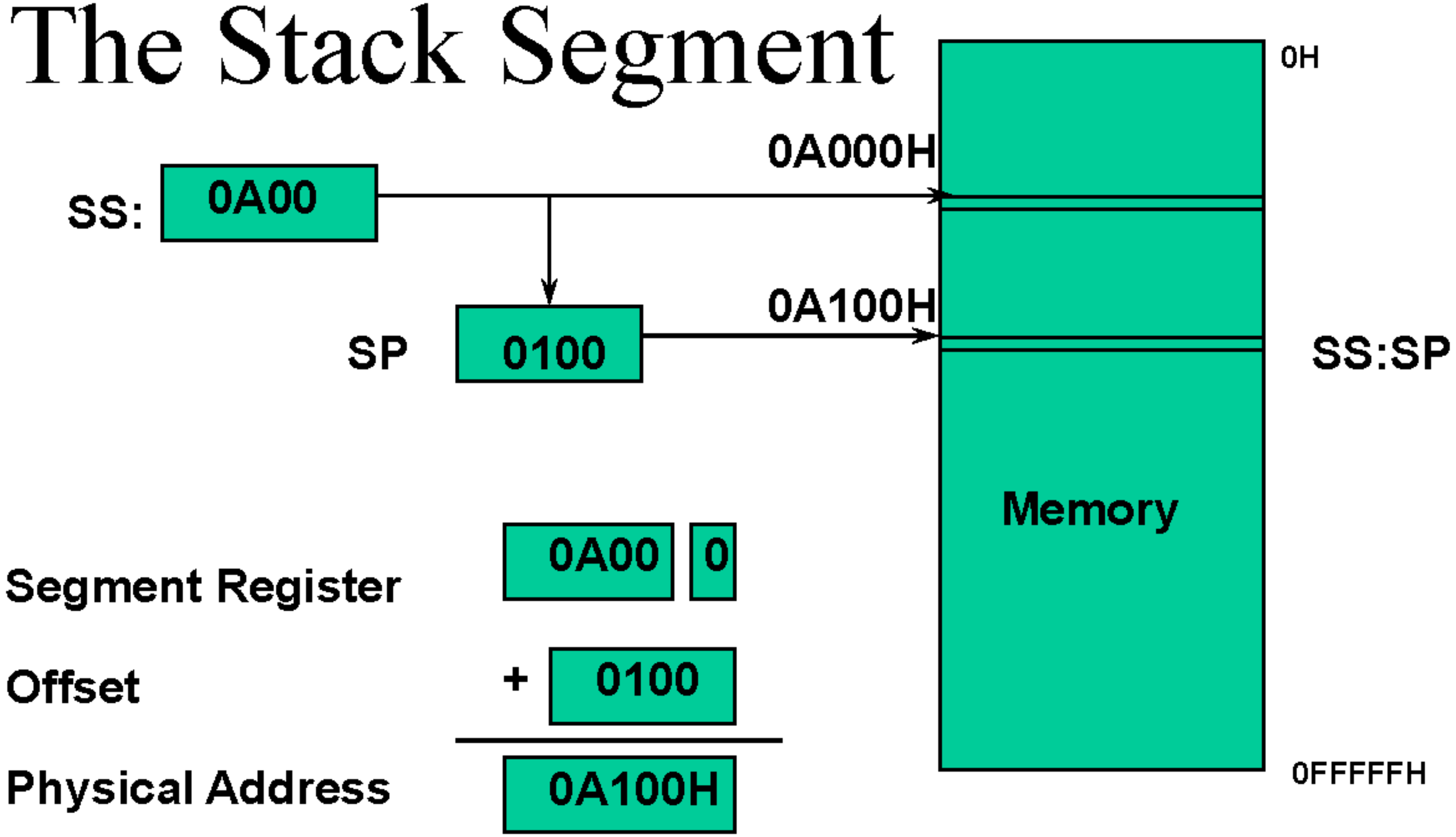
The Code Segment



The offset is the distance in bytes from the start of the segment.
The offset is given by the IP for the Code Segment.
Instructions are always fetched with using the CS register.

The physical address is also called the absolute address.

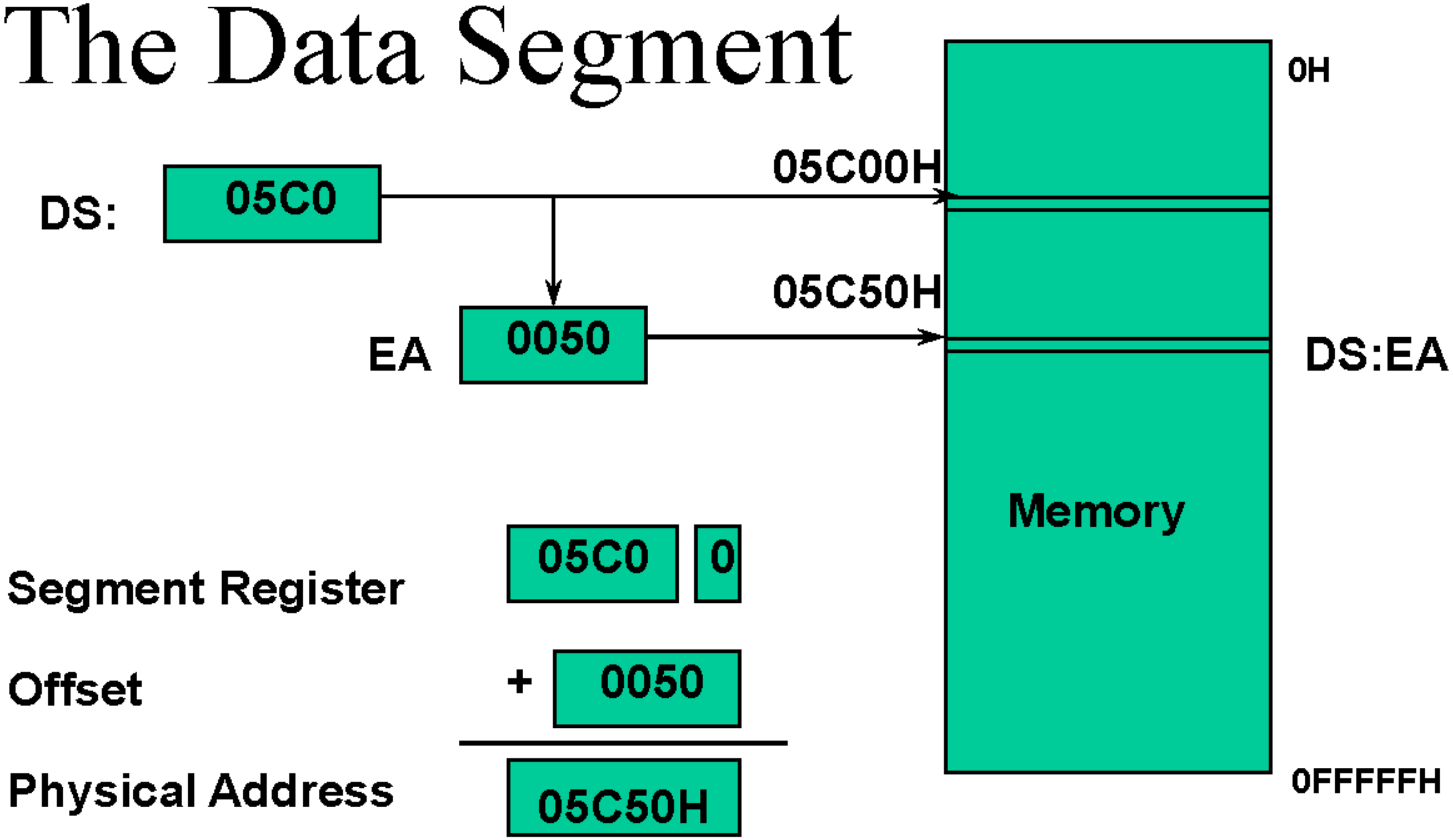
The Stack Segment



The offset is given by the SP register.
The stack is always referenced with respect to the stack segment register.
The stack grows toward decreasing memory locations.
The SP points to the last or top item on the stack.

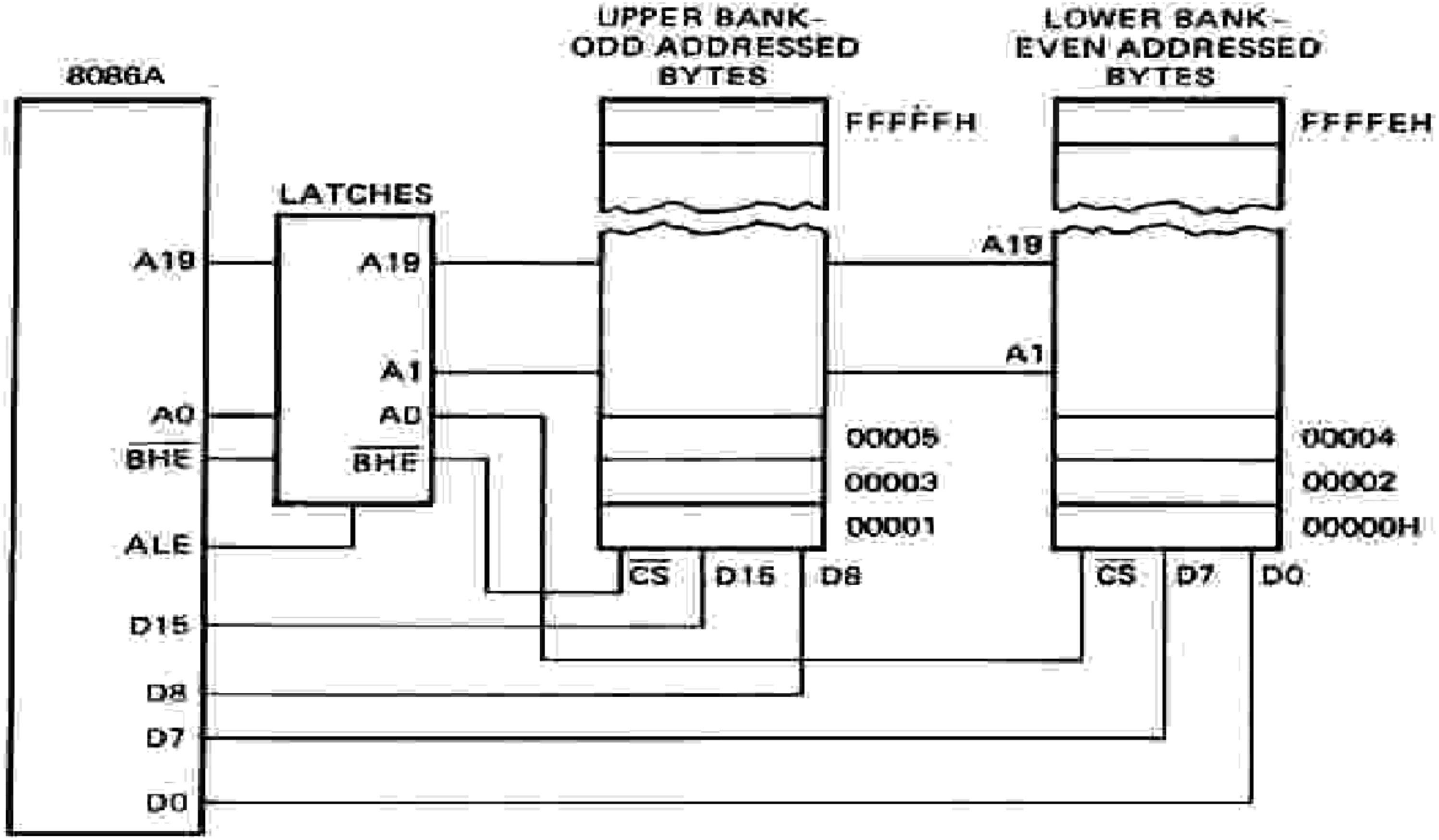
PUSH - pre-decrement the SP
POP - post-increment the SP

The Data Segment



Data is usually fetched with respect to the DS register.
The effective address (EA) is the offset.
The EA depends on the addressing mode.

8086 memory Organization



(a)

ADDRESS	DATA TYPE	$\overline{BHE}$	A0	BUS CYCLES	DATA LINES USED
0000	BYTE	1	0	ONE	D0-D7
0000	WORD	0	0	ONE	D0-D15
0001	BYTE	0	1	ONE	D8-D15
0001	WORD	0	1	FIRST	D0-D8
		1	0	SECOND	D8-D15

Even addresses are on the low half of the data bus (D0-D7).

Odd addresses are on the upper half of the data bus (D8-D15).

A0 = 0 when data is on the low half of the data bus.

BHE’ = 0 when data is on the upper half of the data bus.