

The background is a solid blue gradient. At the top, there are several wavy, horizontal lines in lighter shades of blue and cyan, creating a sense of movement or a horizon line. The text is centered in the upper half of the image.

Unit 1

Introduction



Overview of VLSI Design

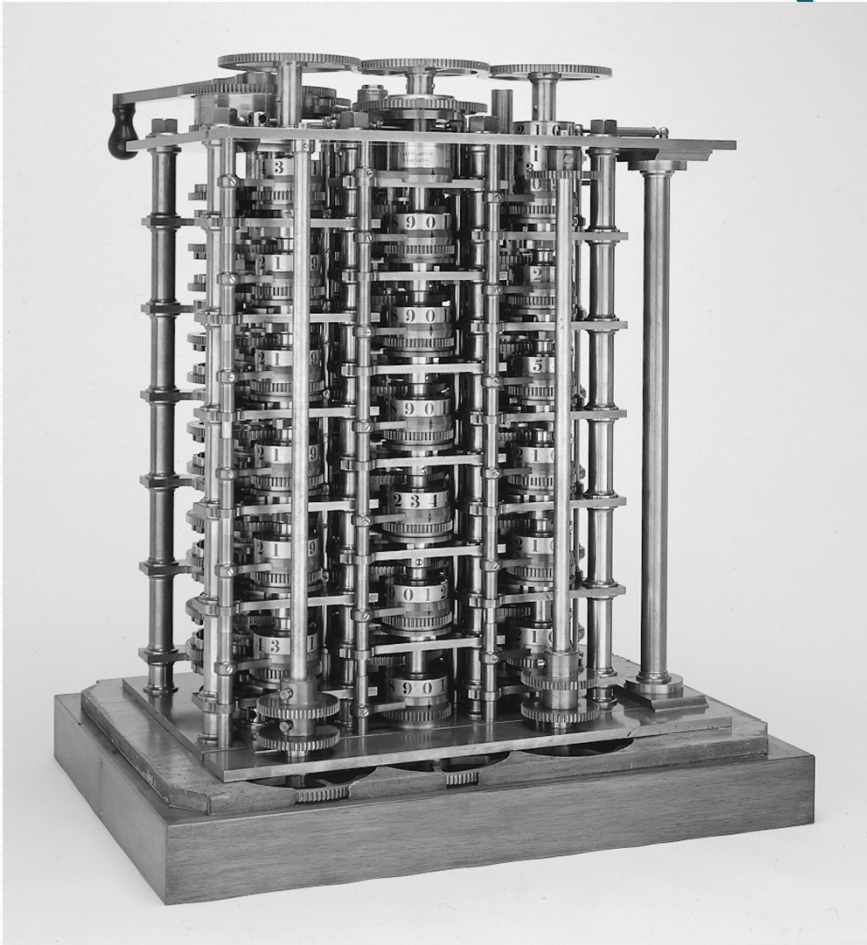
- The unit starts with the basic introduction of Very Large Scale Integrated Circuit.
- After that some basic keywords are introduced and some background is provided.
- After this the VLSI design flow is illustrated.
- After Introduction of design flow MOSFET fabrication steps are introduced.
- In the fabrication, at very first process flow is illustrated and then CMOS fabrication is described
- Layout designing rules and design rule check (DRC) are explained further.
- Stick diagram and mask diagram are also explained in addition to layout design in CMOS fabrication.



Overview of VLSI Design (Contd.)

- After the basic fabrication steps and designing rules, the MOS transistor operation is illustrated.
- The MOS System under external bias is explained further. This provides the conceptual enhancement to the students.
- After this, Operation of MOSFET is explained fully. This helps students to implement it further.
- Then MOSFET - Current /Voltage Characteristics are explained which improves designing skill through MOSFET.
- At the end Scaling and Small geometry effects and capacitances are described.
- The unit build the basic knowledge about CMOS fabrication and design.

The First Computer

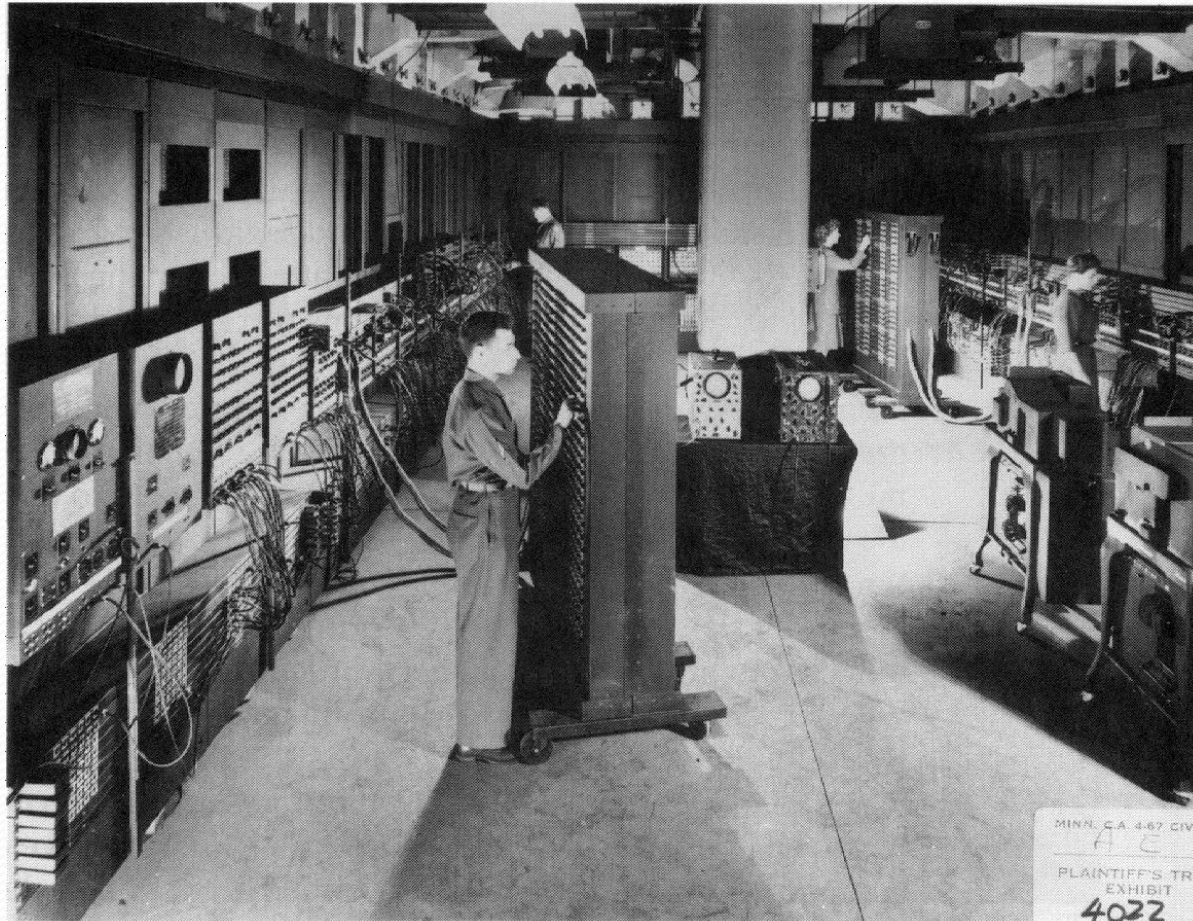


**The Babbage
Difference Engine
(1832)**

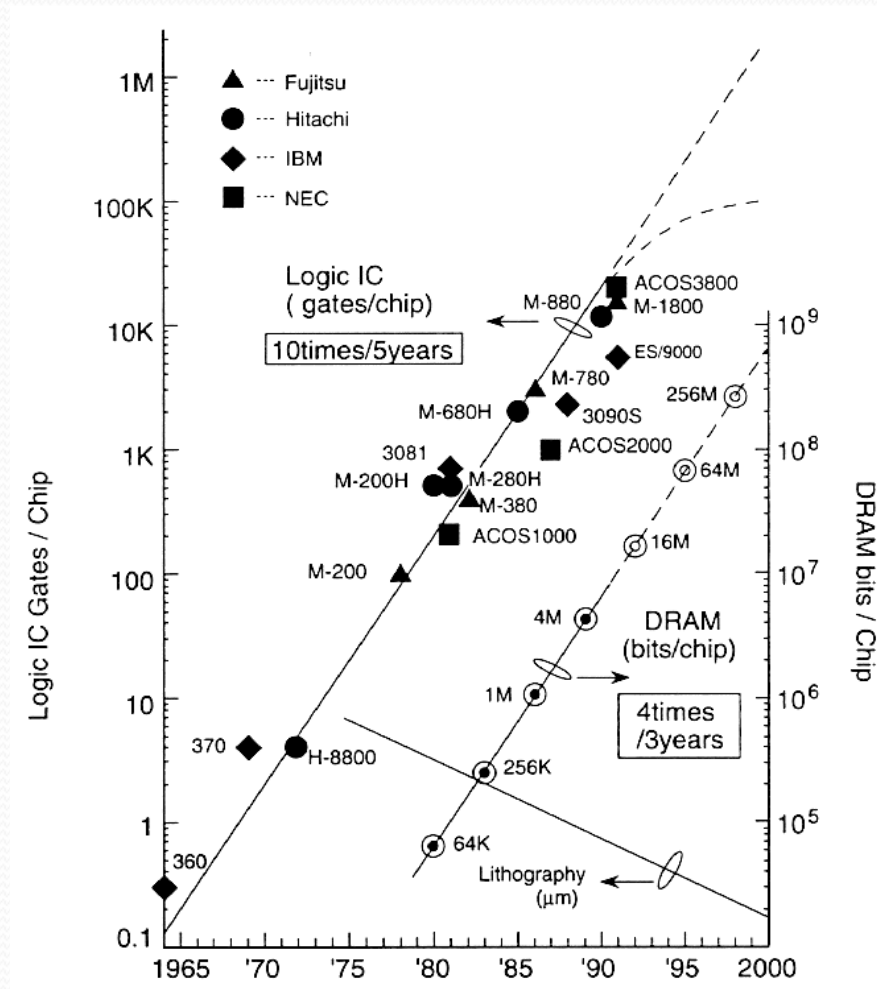
25,000 parts

cost: £17,470

ENIAC - The first electronic computer (1946)



Evolution in Complexity



What is “CMOS VLSI”?

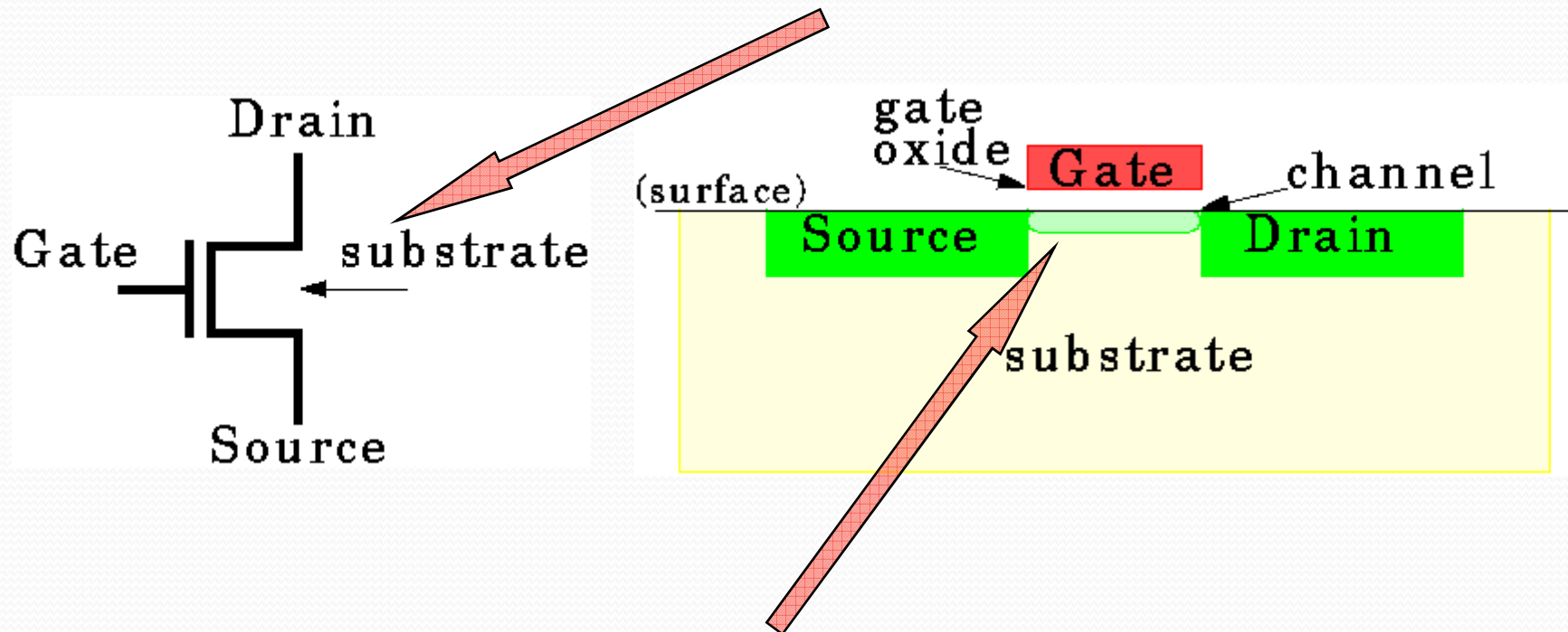
- MOS = Metal Oxide Semiconductor (This used to mean a Metal gate over Oxide insulation)
- Now we use polycrystalline silicon which is deposited on the surface of the chip as a gate. We call this “poly” or just “red stuff” to distinguish it from the body of the chip, the substrate, which is a single crystal of silicon.
- We do use metal (aluminum) for interconnection wires on the surface of the chip.

CMOS: Complementary MOS

- Means we are using both N-channel and P-channel type enhancement mode Field Effect Transistors (FETs).
- Field Effect- NO current from the controlling electrode into the output
 - FET is a voltage controlled current device
 - BJT is a current controlled current device
- N/P Channel - doping of the substrate for increased carriers (electrons or holes)

N-Channel Enhancement mode MOS FET

- Four Terminal Device - substrate bias



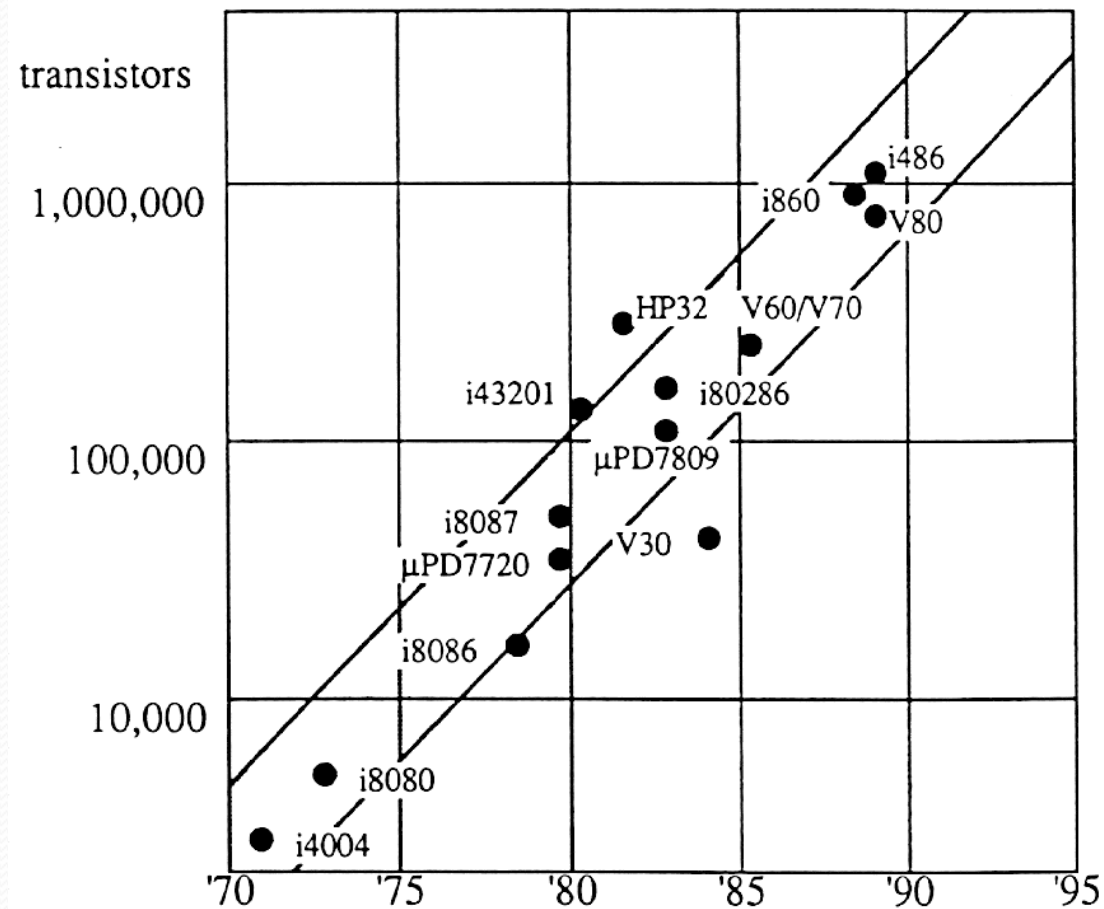
–The “self aligned gate” - key to CMOS



VLSI: Very Large Scale Integration

- Integration: Integrated Circuits
 - multiple devices on one substrate
- How large is Very Large?
 - SSI (small scale integration)
 - 7400 series, 10-100 transistors
 - MSI (medium scale)
 - 74000 series 100-1000
 - LSI 1,000-10,000 transistors
 - VLSI > 10,000 transistors
 - ULSI/SLSI (some disagreement)

Evolution in Transistor Count



Scale Example

- Consider a chip size of 20mm X 20mm
- Consider a transistor size of 2 μ m X 2 μ m
 - With area for wires, etc.
- 1x10⁸ transistors / chip
- Or - plot at 1 transistor : 1 mm
 - 1 chip : 20 meter x 20 meter plot



VLSI Design

- But the real issue is that VLSI is about designing systems on chips.
- The designs are complex, and we need to use structured design techniques and sophisticated design tools to manage the complexity of the design.
- We also accept the fact that any technology we learn the details of will be out of date soon.
- We are trying to develop and use techniques that will transcend the technology, but still respect it.



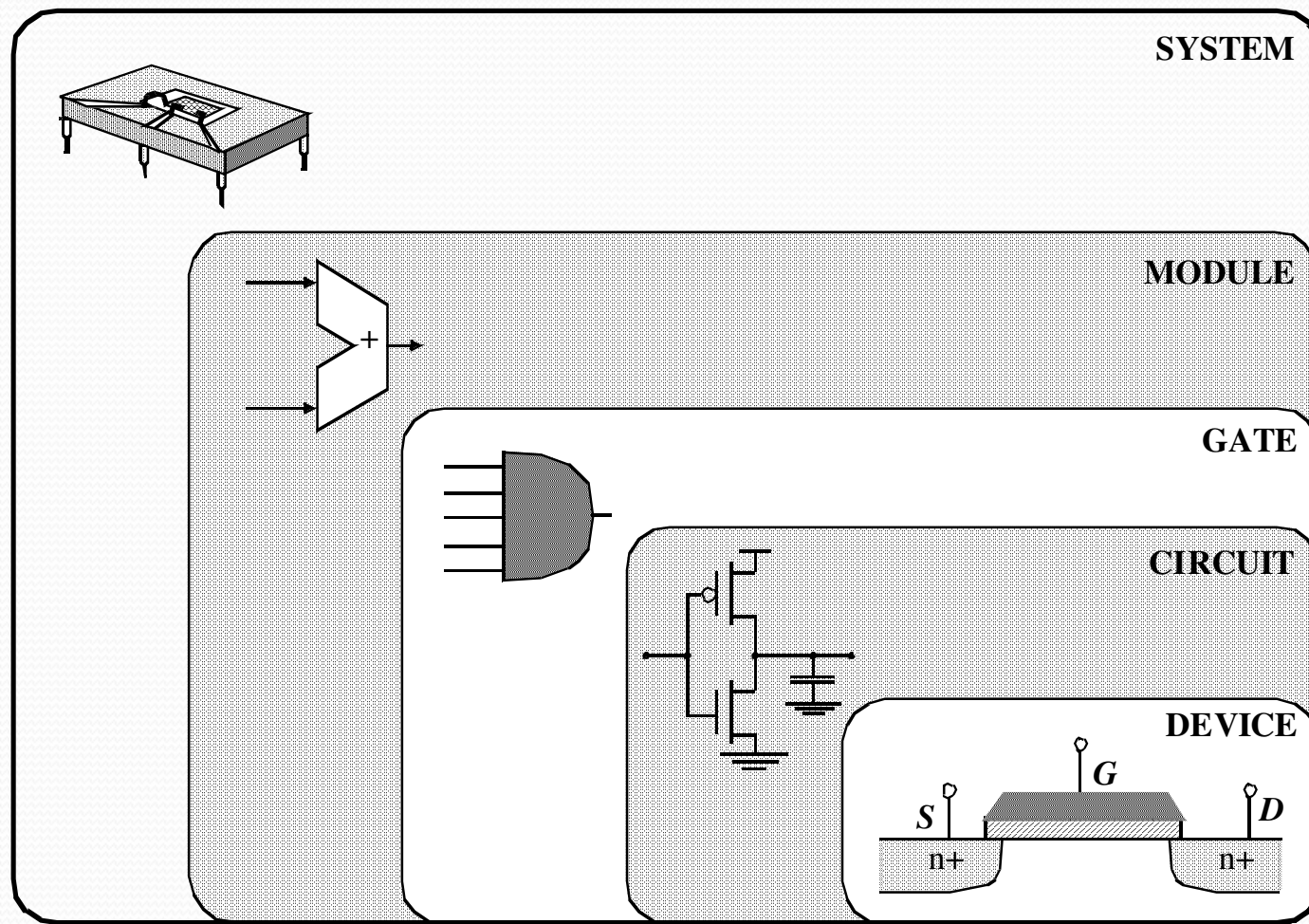
The Process of VLSI Design:

Consists of many different representations/Abstractions of the system (chip) that is being designed.

- System Level Design
- Architecture / Algorithm Level Design
- Digital System Level Design
- Logical Level Design
- Electrical Level Design
- Layout Level Design
- Semiconductor Level Design (possibly more)

Each abstraction/view is itself a Design Hierarchy of refinements which decompose the design.

Design Abstraction Levels



Help from Computer Aided Design tools

- Tools

- Editors
- Simulators
- Libraries
- Module Synthesis
- Place/Route
- Chip Assemblers
- Silicon Compilers

- Experts

- Logic design
- Electronic/circuit design
- Device physics
- Artwork
- Applications - system design
- Architectures

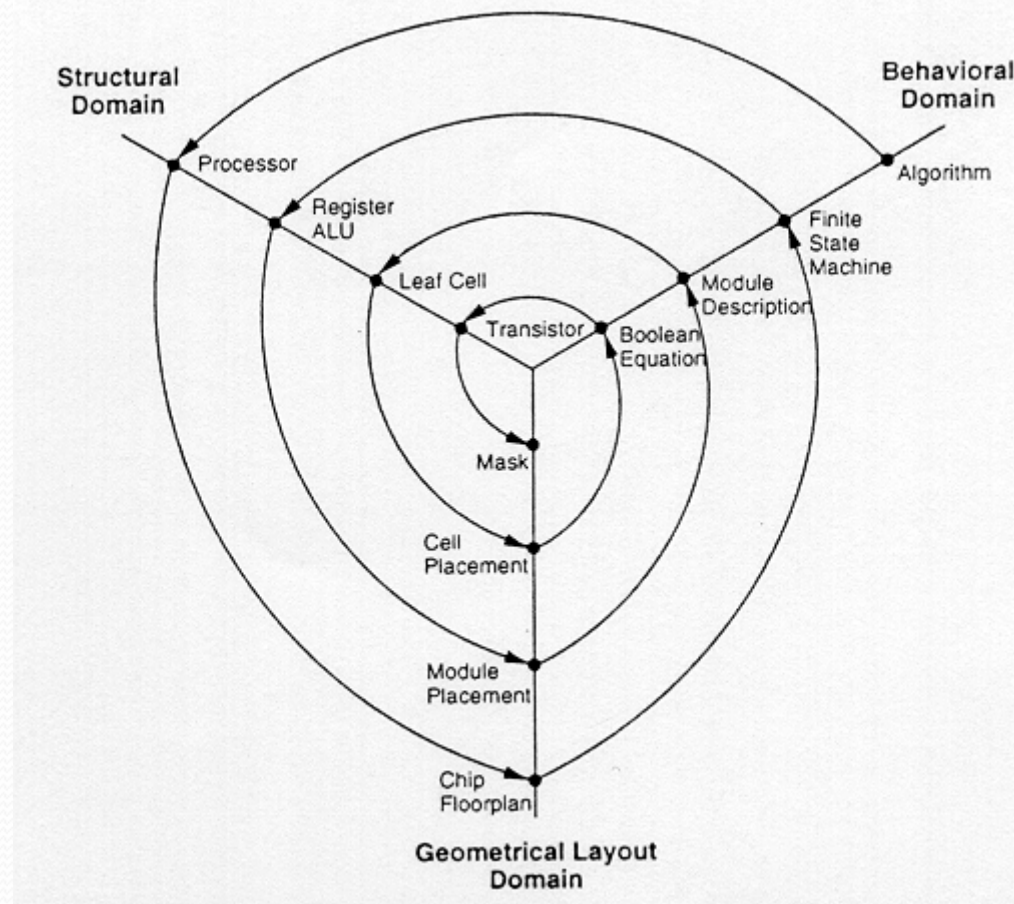


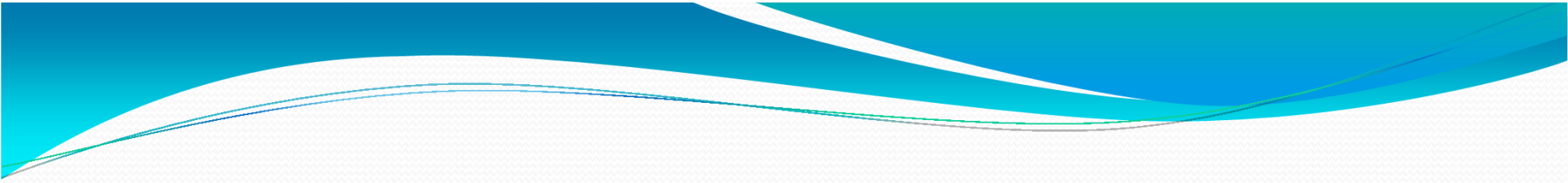
VLSI Design Methodologies

- Methodologies which are based on:
 - System Level Abstractions v.s. Device Characteristic Abstractions
 - Logic structures and circuitry change slowly over time
 - trade-offs do change, but the choices do not
 - Scalable Designs
 - Layout techniques also change slowly.
 - But the minimum feature size steadily decreases with time (also Voltage, Die Size, etc.)

VLSI Design Flow

(Y-chart representation)



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- The Y-chart consists of three major domains, namely:
 - Behavioral domain,
 - Structural domain,
 - Geometrical layout domain.



The design flow starts from the algorithm that describes the behavior of the target chip. The corresponding architecture of the processor is first defined.

- It is mapped onto the chip surface by floorplanning. The next design evolution in the behavioral domain defines finite state machines (FSMs) which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs).
- These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnects area and signal delays. The third evolution starts with a behavioral module description.
- Individual modules are then implemented with leaf cells. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a cell placement & routing program.
- The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In standard-cell based design, leaf cells are already pre-designed and stored in a library for logic design use.

VLSI Design Flow

(Simplified view of VLSI design)

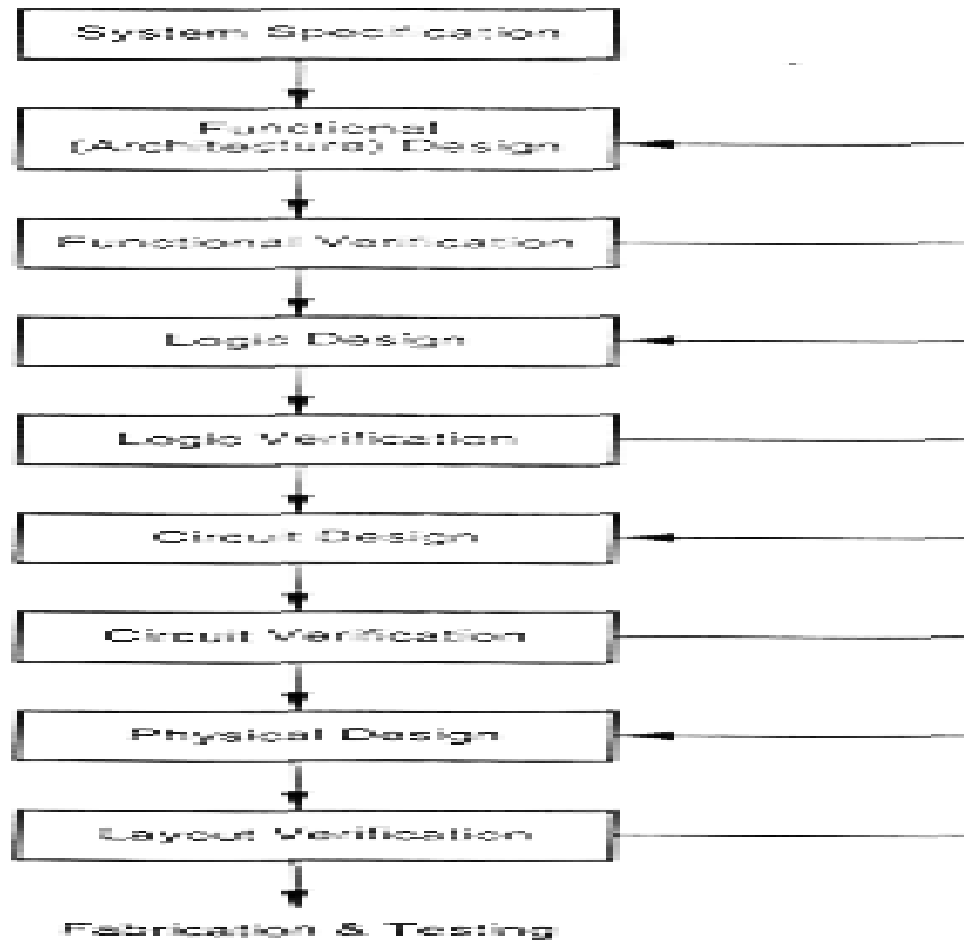
VLSI DESIGN FLOW

Behavioral
Representation

Logic
(Gate-level)
Representation

Circuit
Representation

Layout
Representation



VLSI Design Flow (Contd.)

The design flow is divided in the two parts:

- **1. Front End Design:**

Front-end design includes most of the steps in the flow prior to physical design. (system specification and functional design)

- **2. Back End Design:**

Starting with physical design and beyond is considered the back-end of the design flow.

The physical design stage of the VLSI design flow is also known as the “place and route” stage. This is based upon the idea of physically placing the circuits, which form logic gates and represent a particular design, in such a way that the circuits can be fabricated.