Unit 1
Introduction

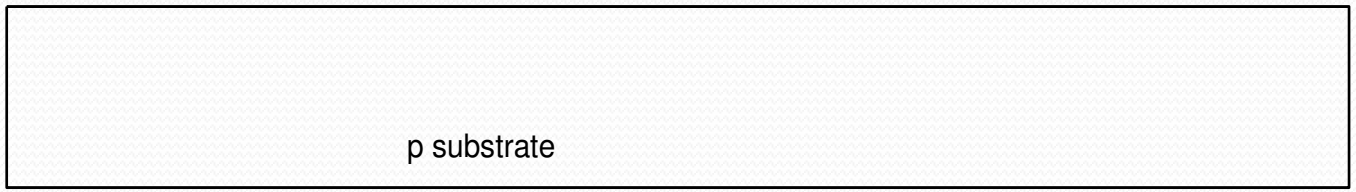
IC Fabrication Process Steps

- The fabrication of integrated circuits consists basically of the following process steps:

- **Lithography:** The process for pattern definition by applying thin uniform layer of viscous liquid (photo-resist) on the wafer surface. The photo-resist is hardened by baking and than selectively removed by projection of light through a reticle containing mask information.
- **Etching:** Selectively removing unwanted material from the surface of the wafer. The pattern of the photo-resist is transferred to the wafer by means of etching agents.
- **Deposition:** Films of the various materials are applied on the wafer. For this purpose mostly two kind of processes are used, physical vapor deposition (PVD) and chemical vapor deposition (CVD).

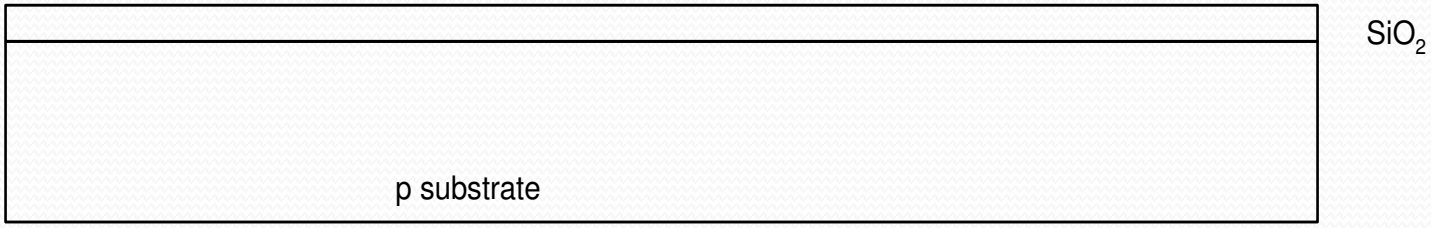
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2



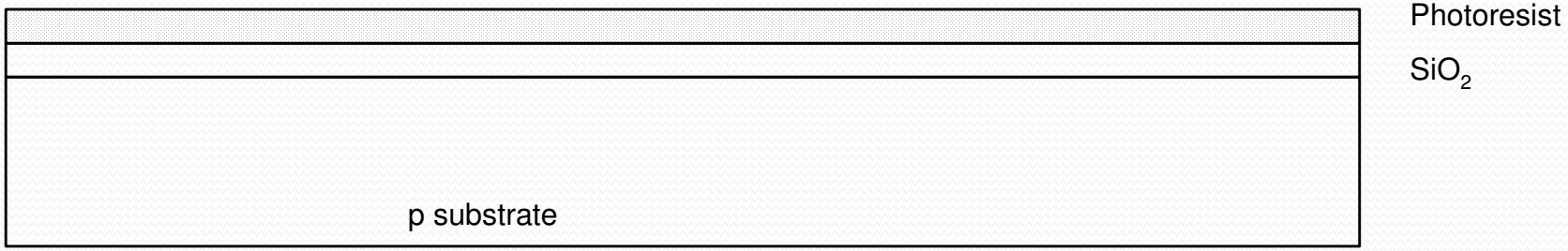
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 Celcius with H_2O or O_2 in oxidation furnace



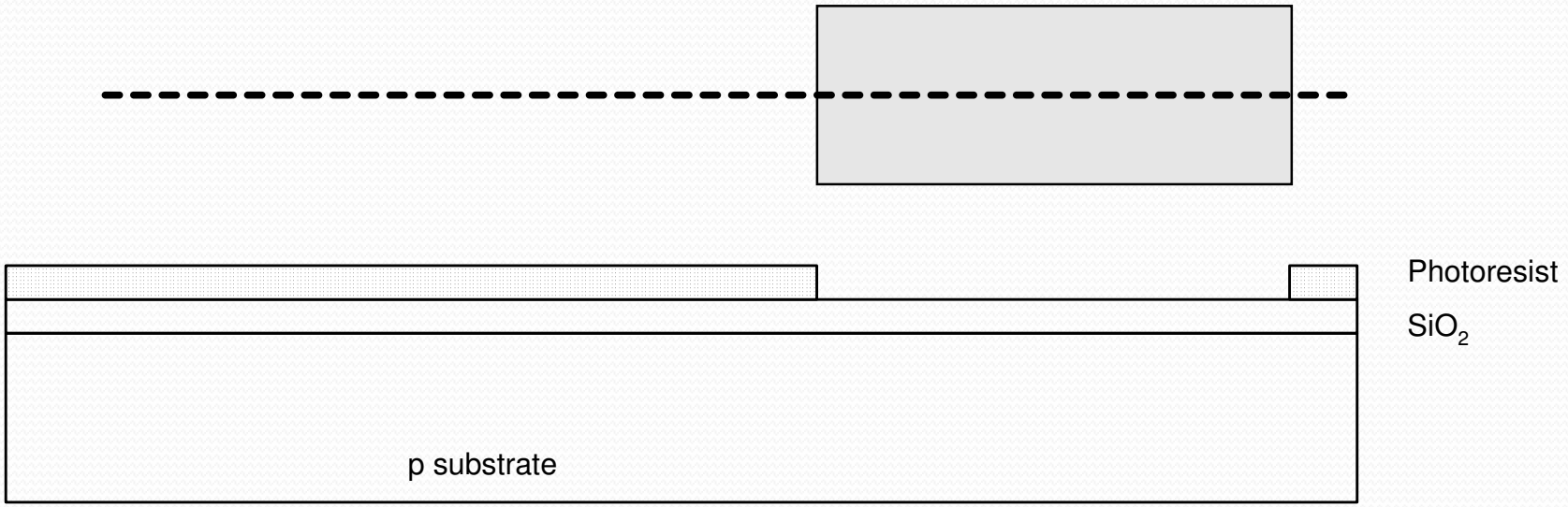
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



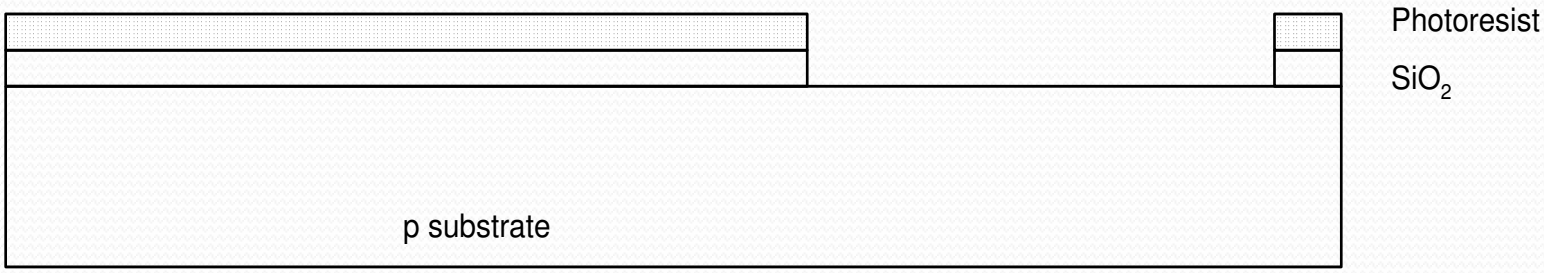
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



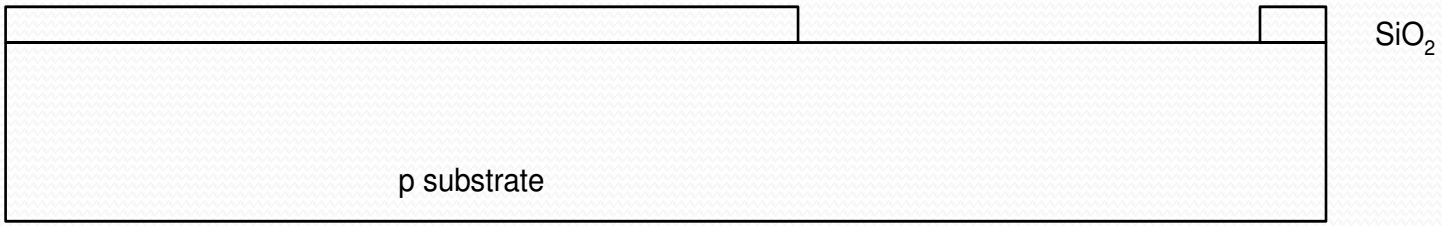
Etch

- Etch oxide with hydrofluoric acid (HF)
- Only attacks oxide where resist has been exposed



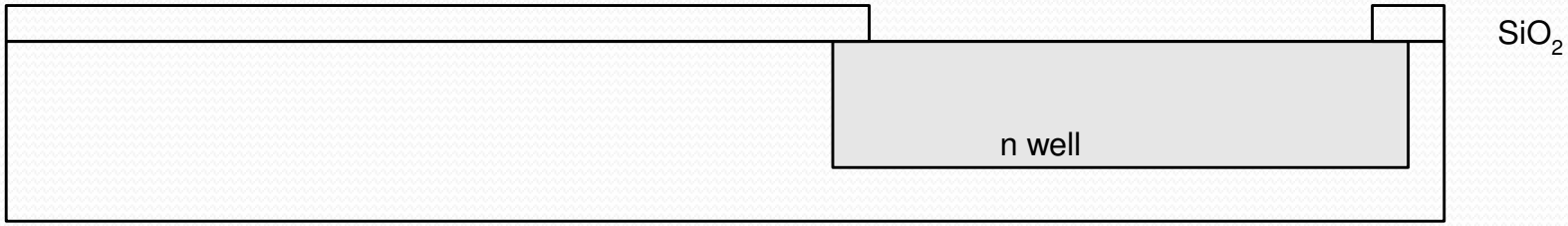
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called *piranha etch*
- Necessary so resist doesn't melt in next step



N-well

- N-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with *arsenic gas*
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

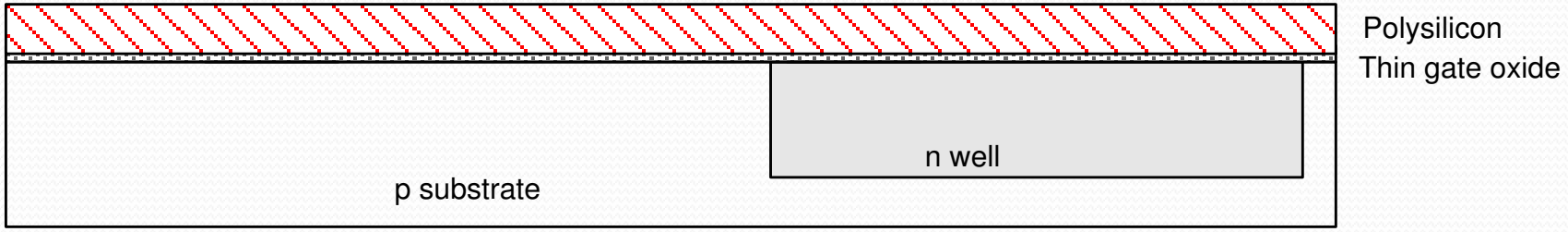


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

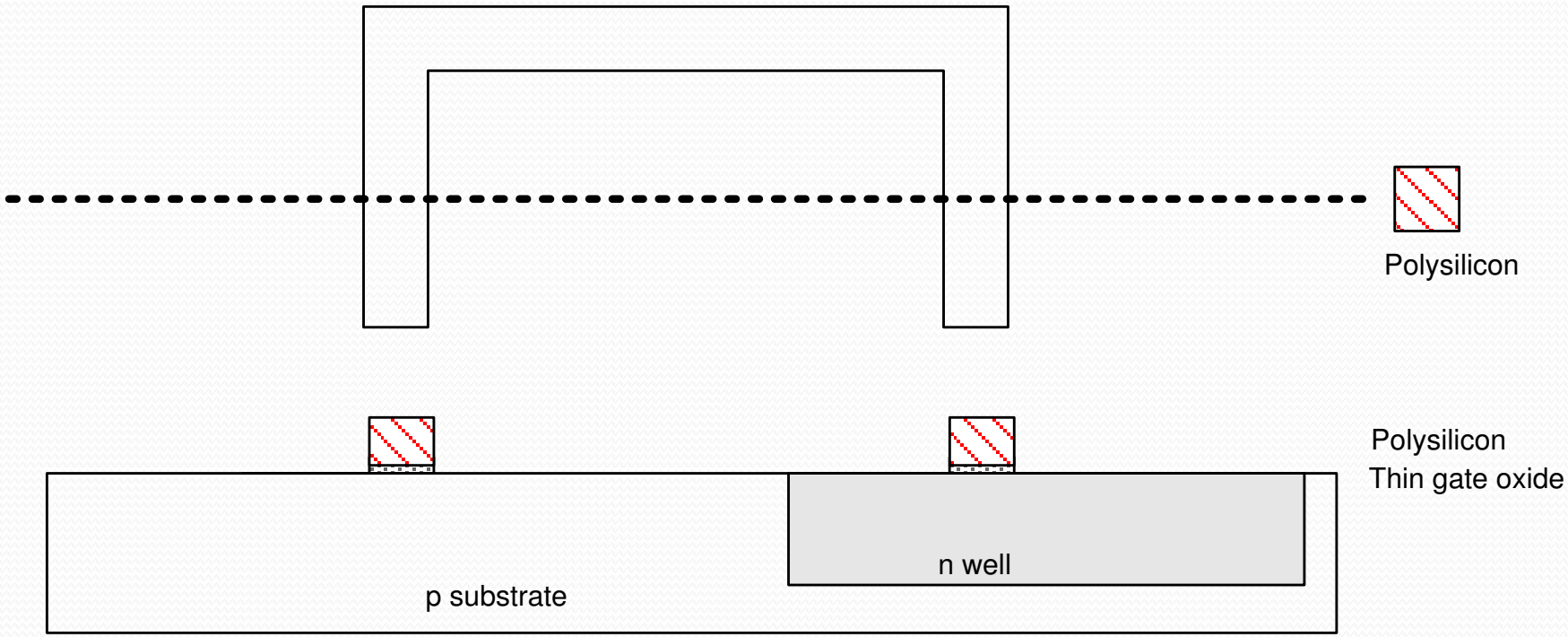
Polysilicon

- Deposit very thin layer of gate oxide (SiO_2)
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



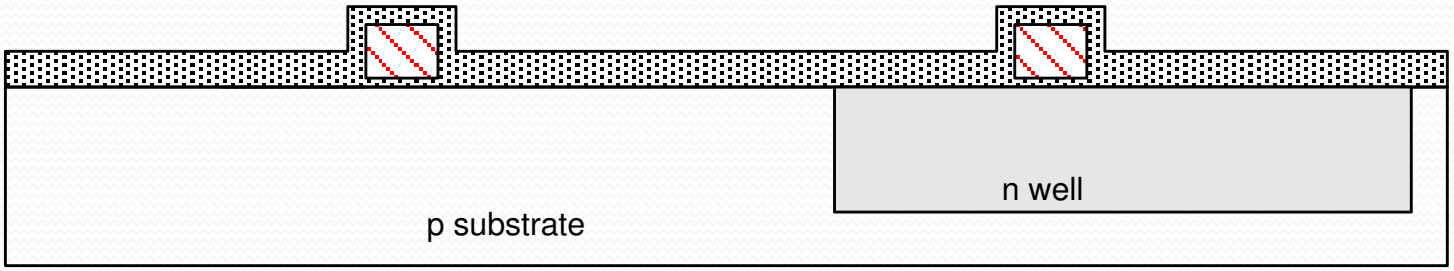
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



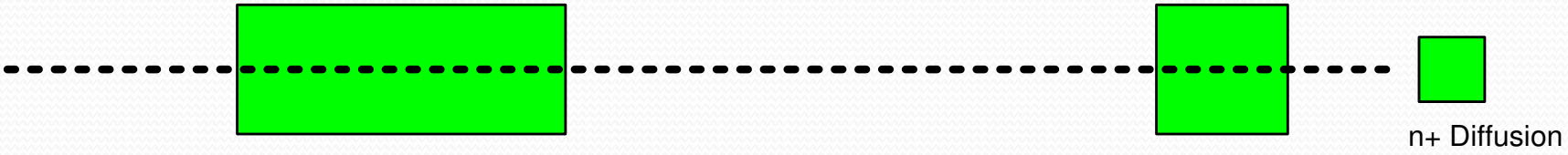
Self-Aligned Process

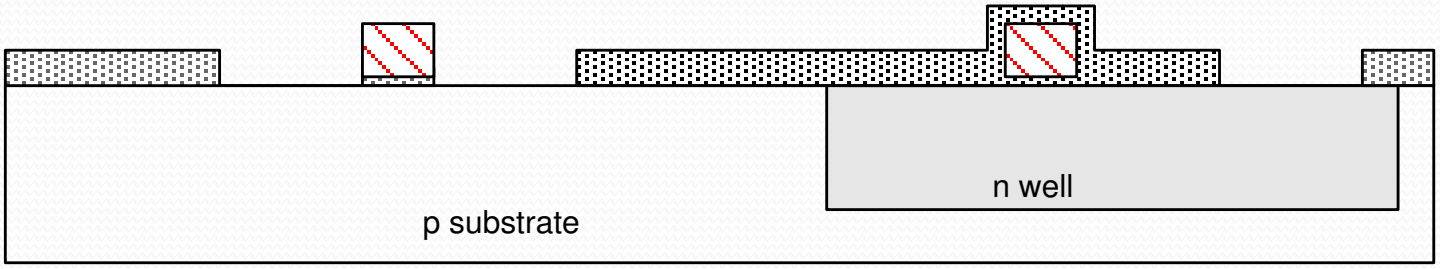
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms NMOS source, drain, and n-well contact



N-diffusion

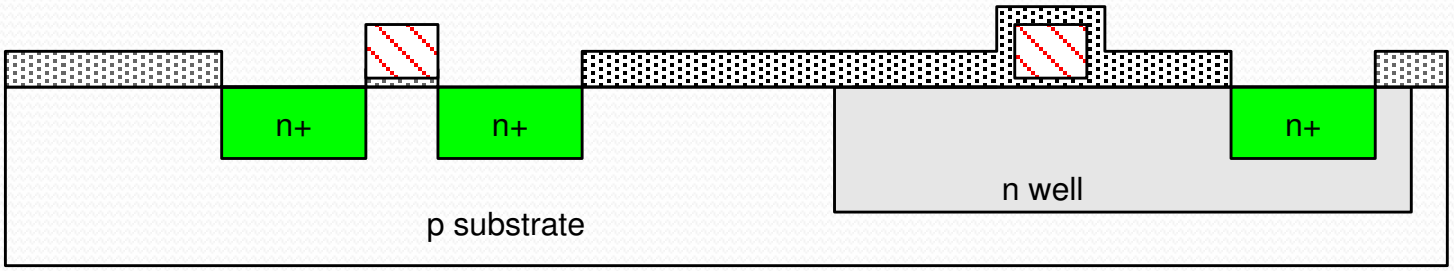
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing





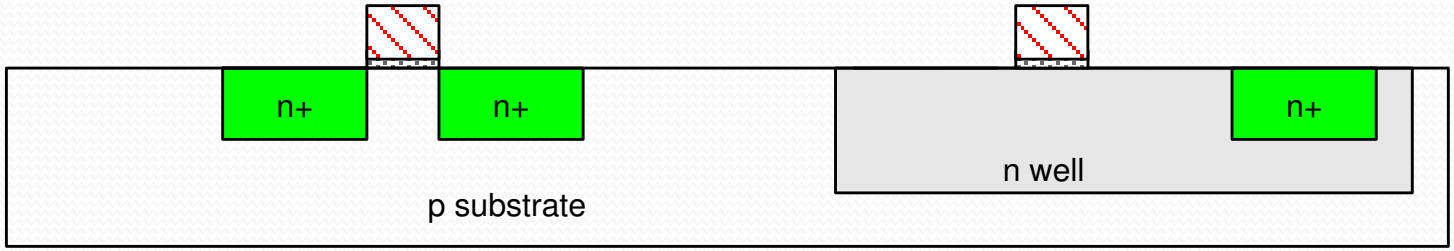
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



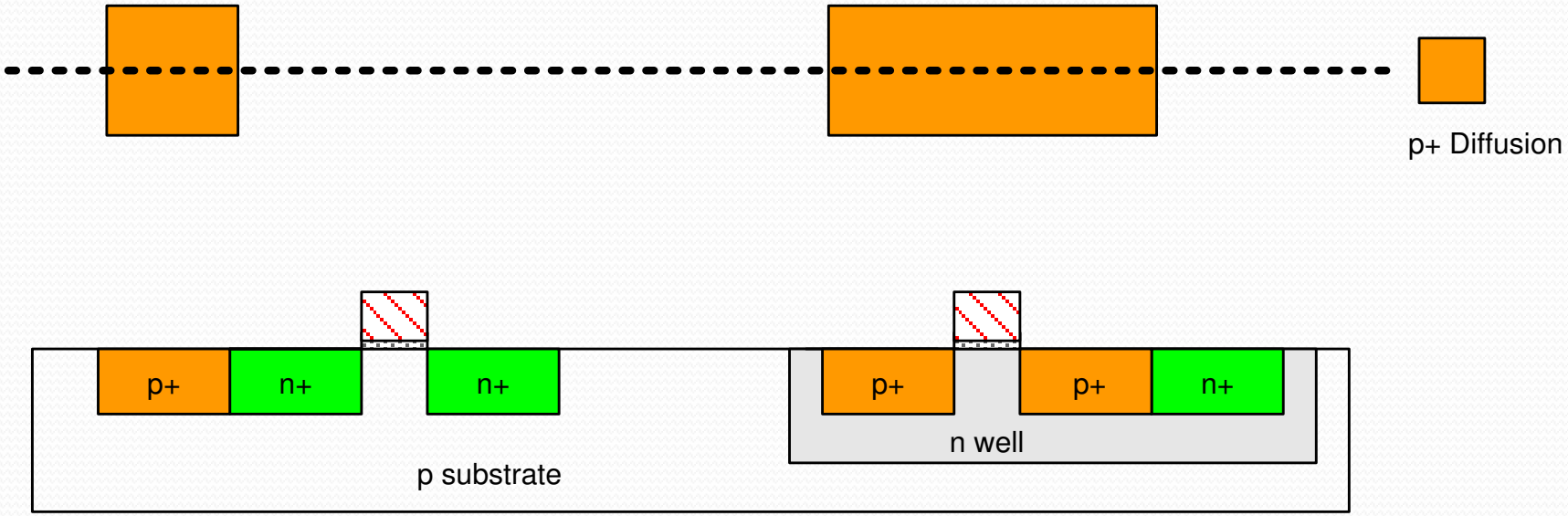
N-diffusion cont.

- Strip off oxide to complete patterning step



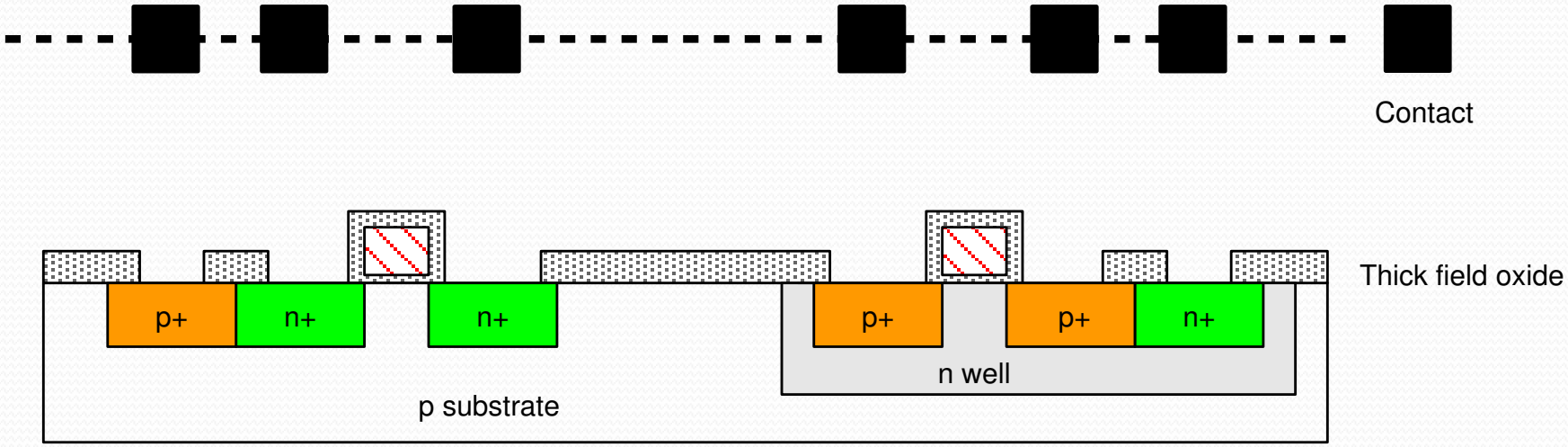
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



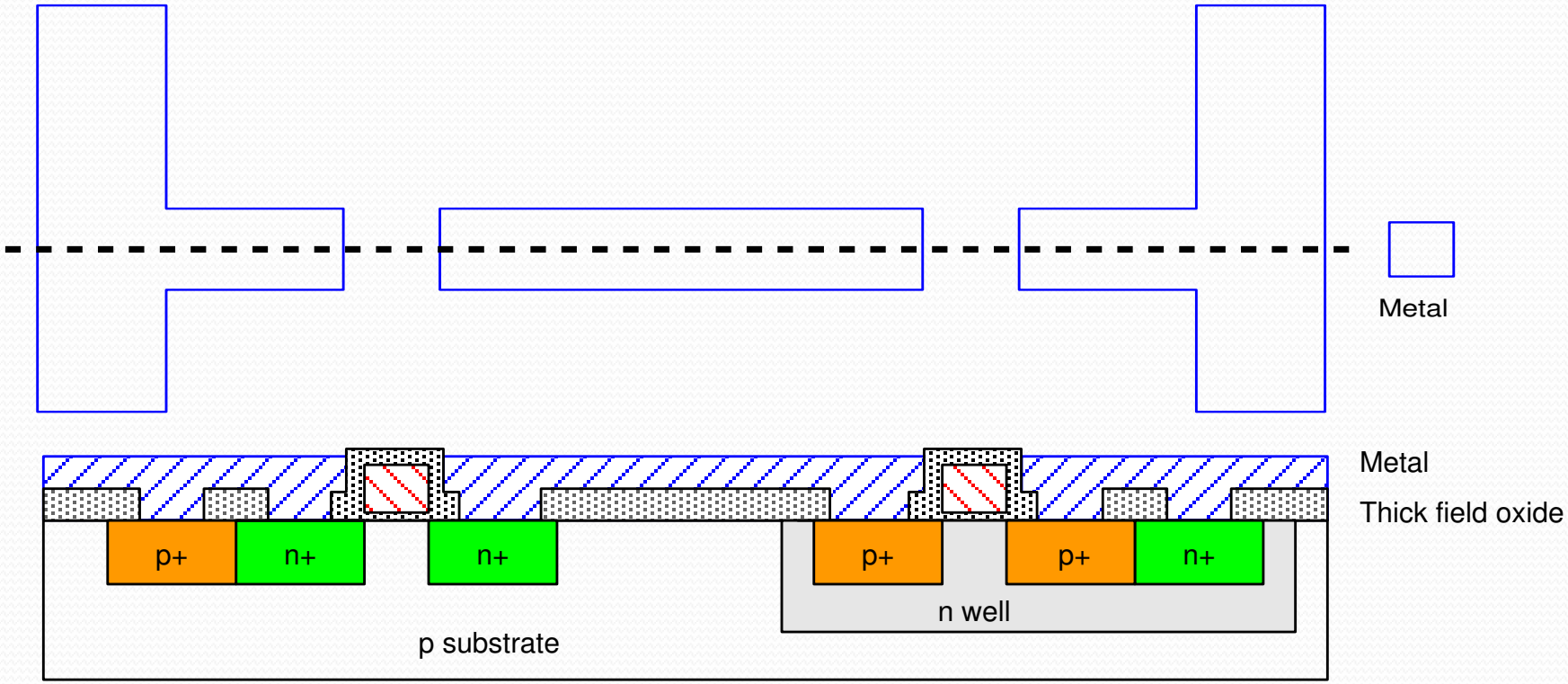
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



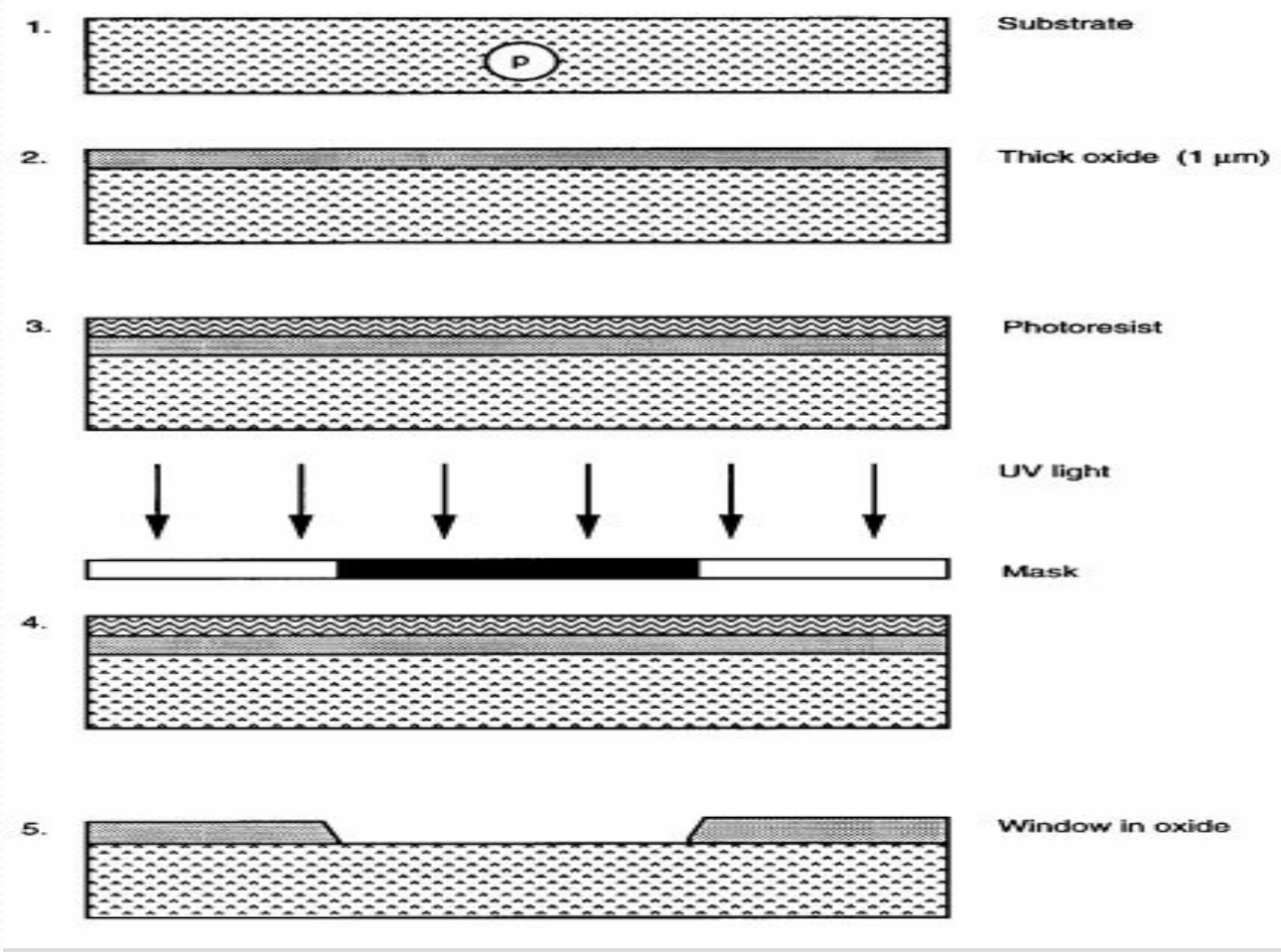
- **Chemical Mechanical Polishing:** A planarization technique by applying a chemical slurry with etchant agents to the wafer surface.

- **Oxidation:** In the oxidation process oxygen (dry oxidation) or HO (wet oxidation) molecules convert silicon layers on top of the wafer to silicon dioxide.

- **Ion Implantation:** Most widely used technique to introduce dopant impurities into semiconductor. The ionized particles are accelerated through an electrical field and targeted at the semiconductor wafer.

- **Diffusion:** A diffusion step following ion implantation is used to anneal bombardment-induced lattice defects.

NMOS Fabrication



NMOS Fabrication (Contd.)