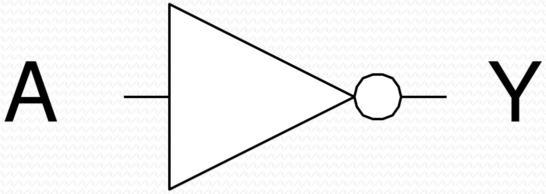
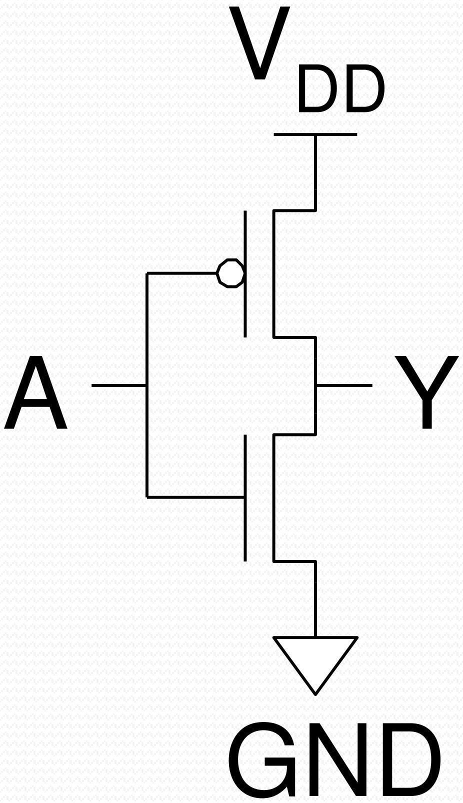
CMOS Inverter

CMOS Inverter

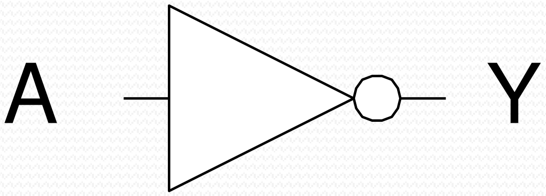
A	Y
0	
1	

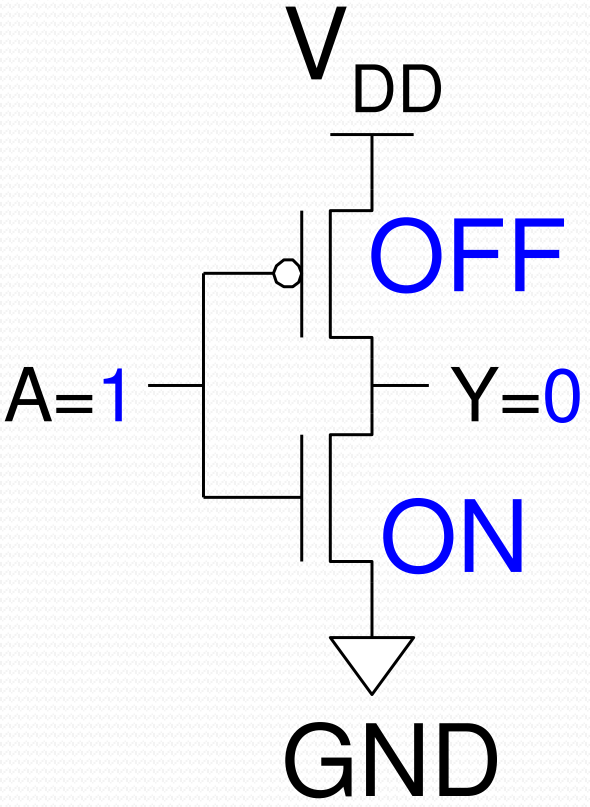




CMOS Inverter

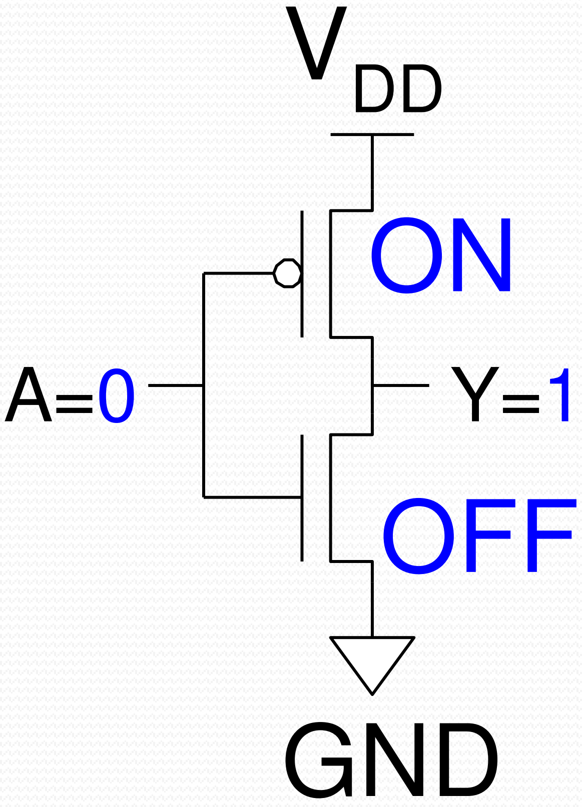
A	Y
0	
1	**0**

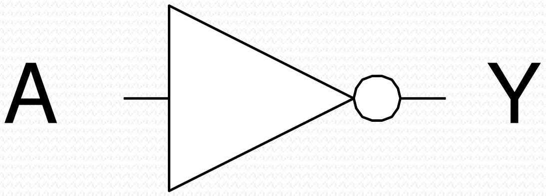




CMOS Inverter

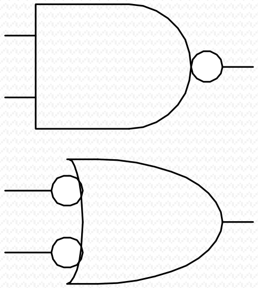
A	Y
0	**1**
1	0

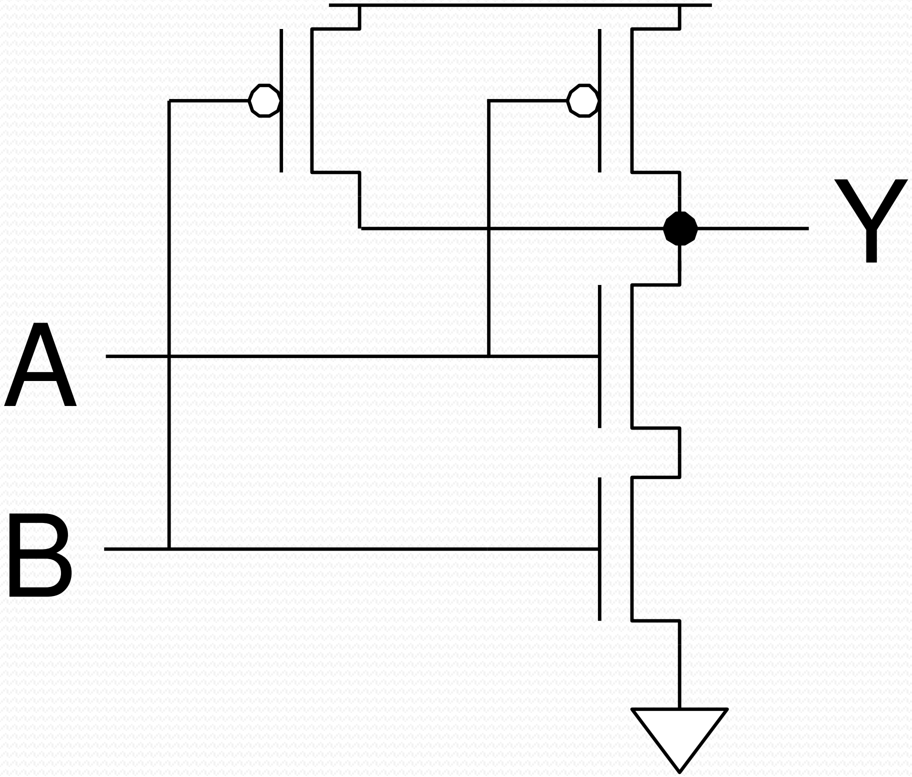




CMOS NAND Gate

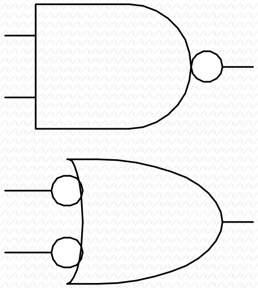
A	B	Y
0	0	
0	1	
1	0	
1	1	

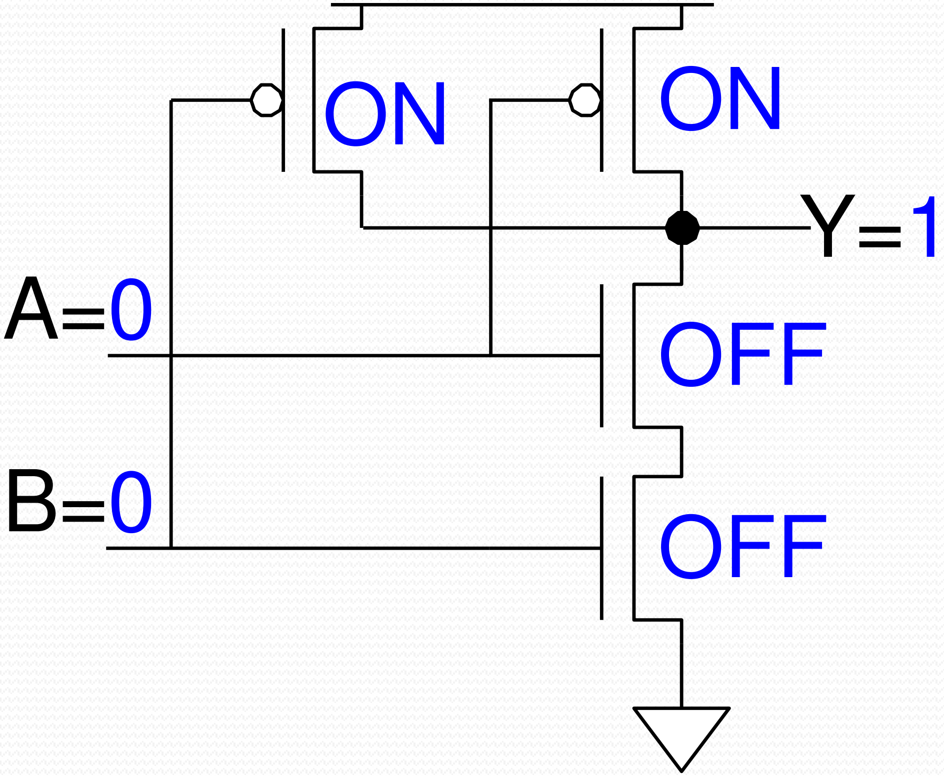




CMOS NAND Gate

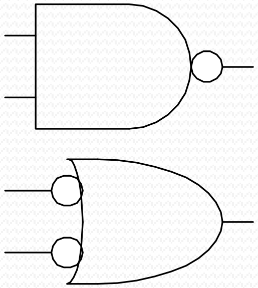
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

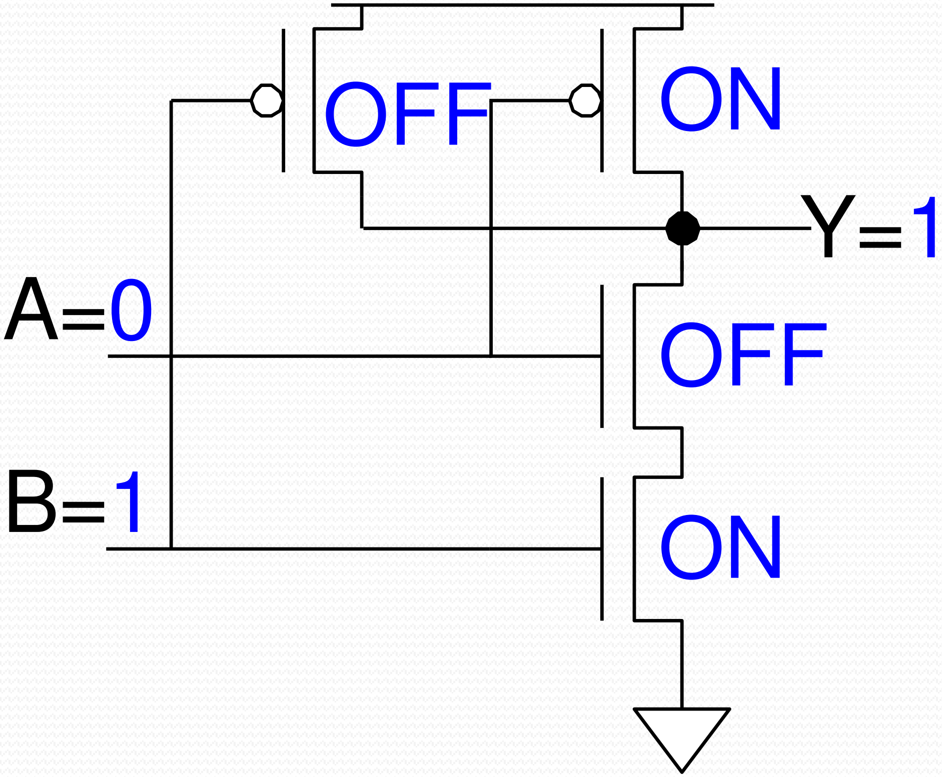




CMOS NAND Gate

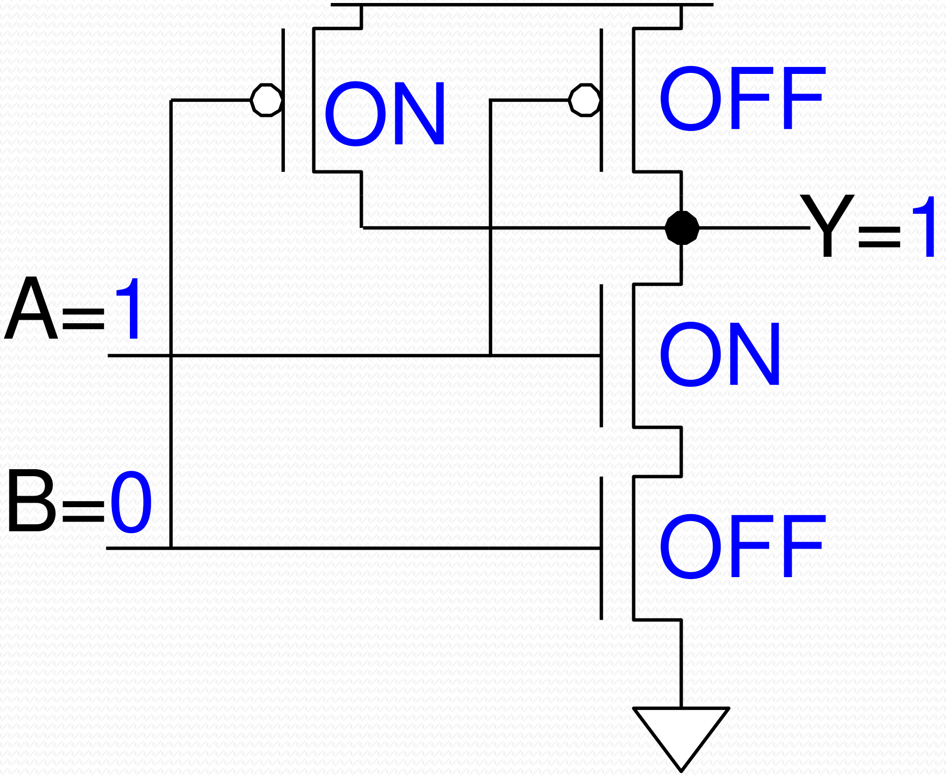
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

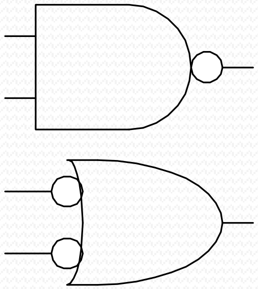




CMOS NAND Gate

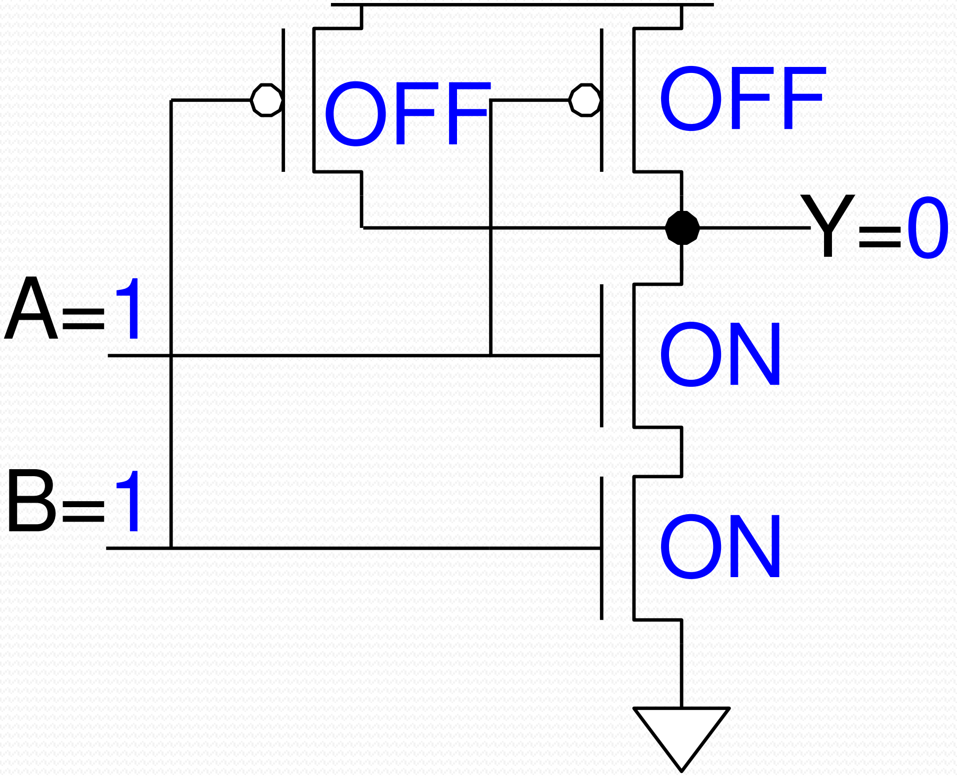
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

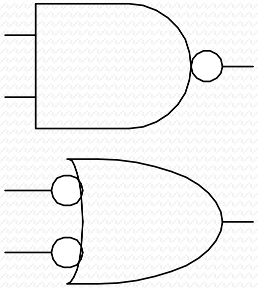




CMOS NAND Gate

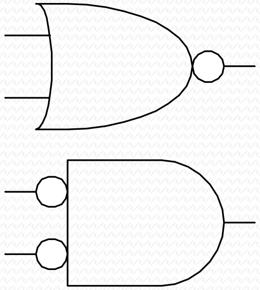
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

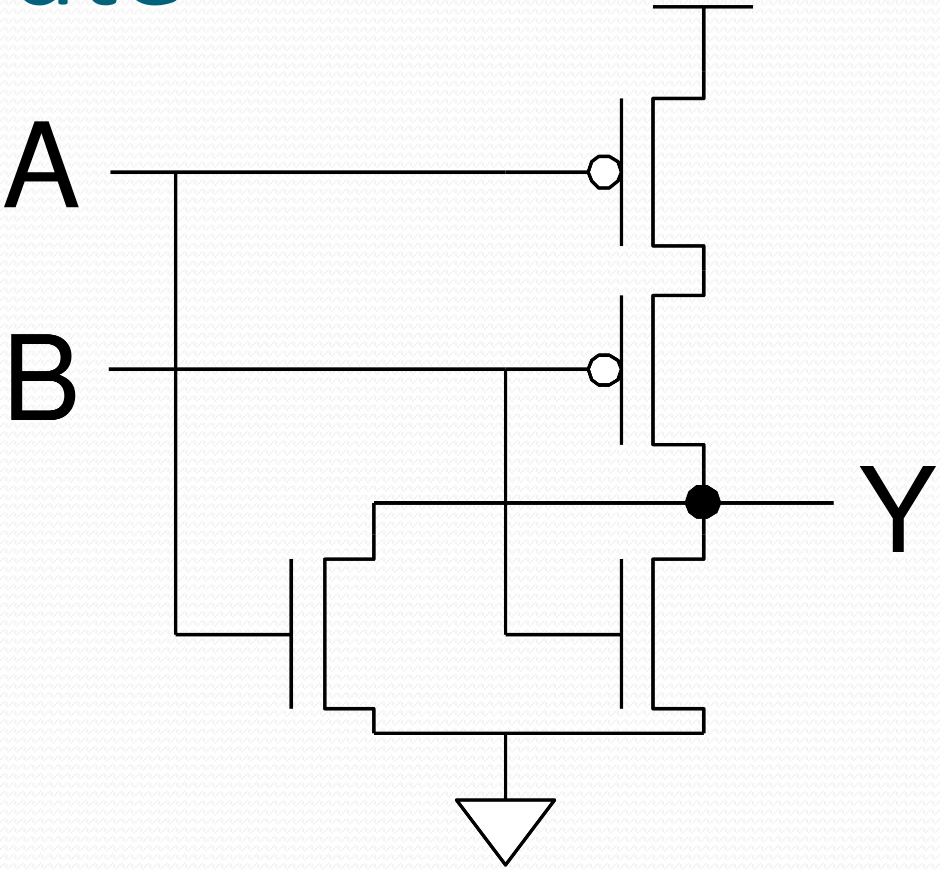




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



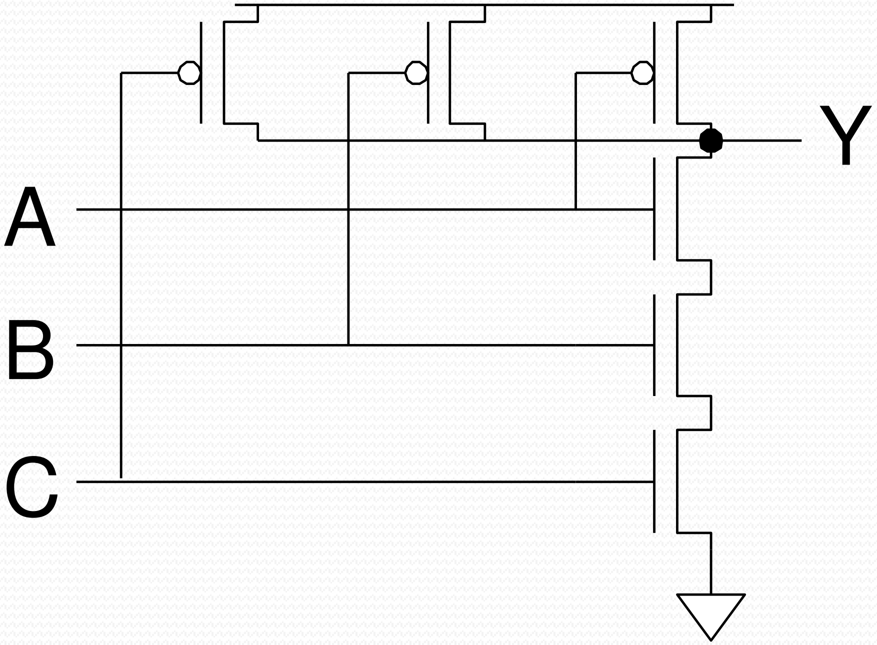


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

CMOS Fabrication Process

- The CMOS can be fabricated using different processes such as:
  1) N-well process for CMOS fabrication
  2) P-well process
  3) Twin tub-CMOS-fabrication process

- CMOS can be obtained by integrating both the NMOS and PMOS transistors on the same chip substrate.

- For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs are required in which semiconductor type and substrate type are opposite to each other.

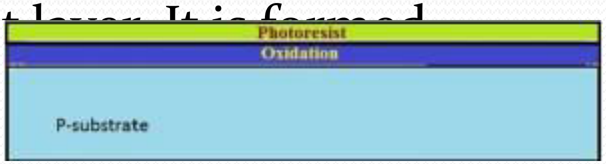
CMOS Fabrication Process (Contd.)

- **Step1: Substrate**
- Start the process with a P-substrate.

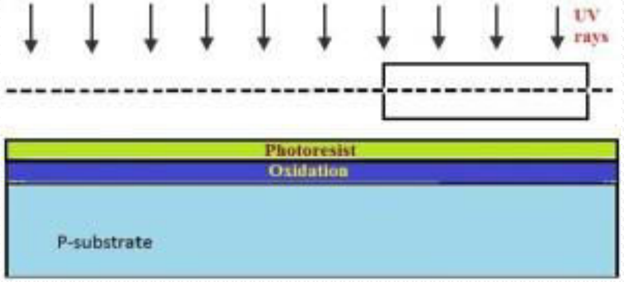
- **Step2: Oxidation**
- The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigra

CMOS Fabrication Process (Contd.)

- **Step3: Photoresist**
- A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.



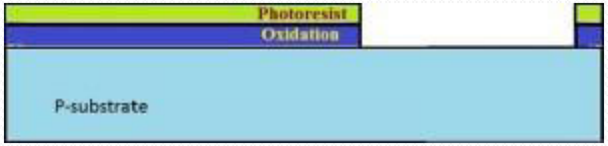
- **Step4: Masking**
- The photoresist is exposed to UV rays through the N-well mask.



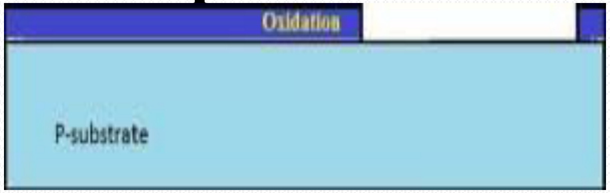
CMOS Fabrication Process (Contd.)

- **Step5: Photoresist removal**
- A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.

- **Step6: Removal of SiO2 using acid etching**
- The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.

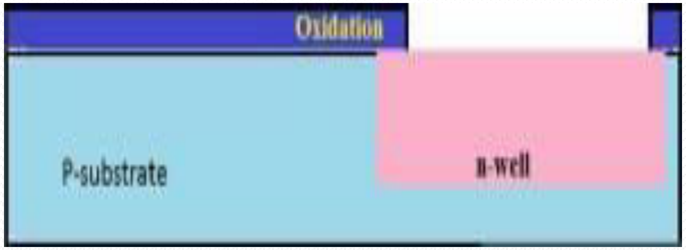


- **Step7: Removal of photoresist**

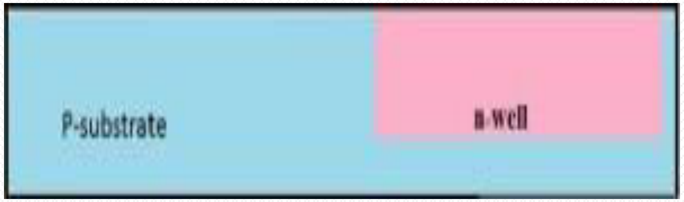


- **Step8: Formation of the N-well**

  By using ion implantation or diffusion process N-well is formed.

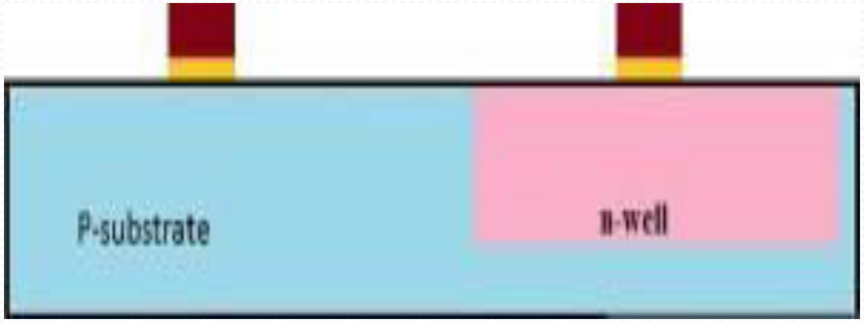


- **Step9: Removal of SiO2**
- Using the hydrofluoric acid, the remaining SiO2 is removed.

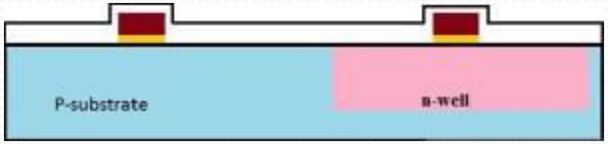


- **Step10: Deposition of polysilicon**
- Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.

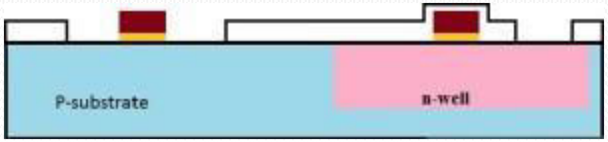
- **Step11: Removing the layer barring a small area for the Gates**
- Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



- **Step12: Oxidation process**
- Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.

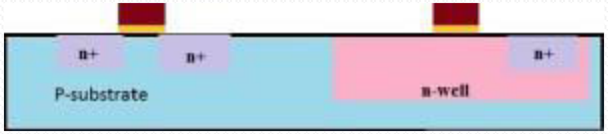


- **Step13: Masking and N-diffusion**
- By using the masking process small gaps are made for the purpose of N-diffusion



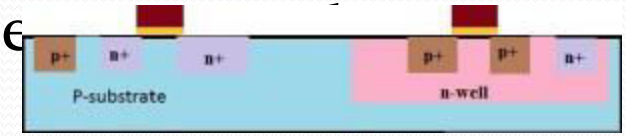
- The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.

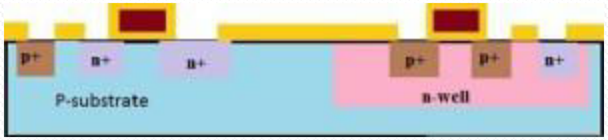
- **Step14: Oxide stripping**
- The remaining oxidation layer is stripped off.



- **Step15: P-diffusion**
- Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.

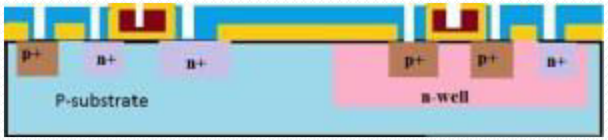
- **Step16: Thick field oxide**
- A thick-field oxide is formed in all regions except the terminals of the



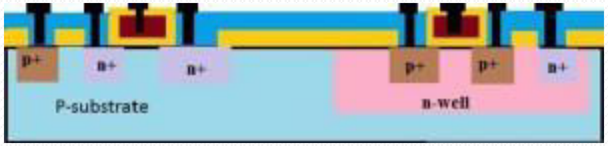


- **Step17: Metallization**
- Aluminum is sputtered on the whole wafer.

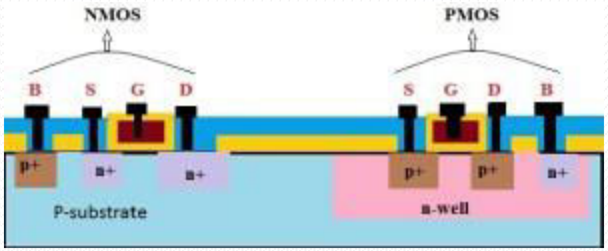
- **Step18: Removal of excess metal**
- The excess metal is removed from the wafer layer.



- **Step19: Terminals**
- The terminals of the PMOS and NMOS are made from respective gaps.



- **Step20: Assigning the names of the terminals of the NMOS and PMOS**

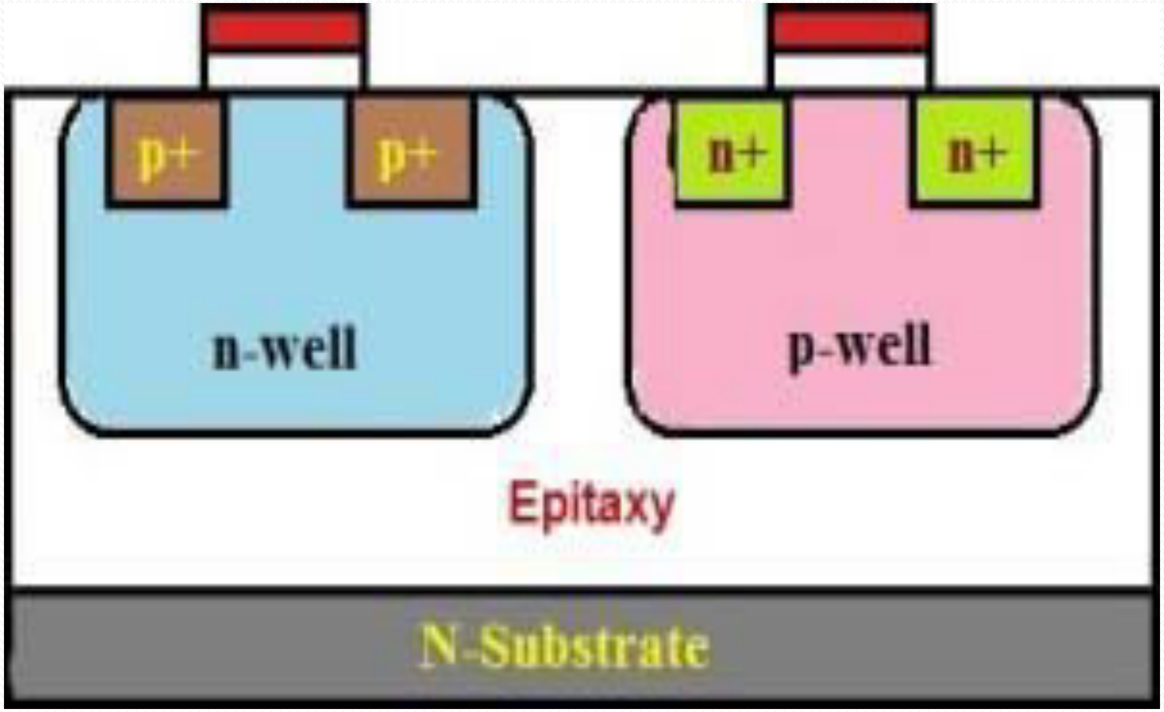


Fabrication of CMOS using P-well Process

- P-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices.
- Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS.

Twin tub-CMOS Fabrication Process

- In this process, separate optimization of the n-type and p-type transistors will be provided. The independent optimization of Vt, body effect and gain of the P-devices, N-devices can be made possible with this process.
- Different steps of the fabrication of the CMOS using the twintub process are as follows:
- Lightly doped n+ or p+ substrate is taken and, to protect the latch up, epitaxial layer is used.
- The high-purity controlled thickness of the layers of silicon are grown with exact dopant concentrations.
- The dopant and its concentration in Silicon are used to determine electrical properties.
- Formation of the tub
- Thin oxide construction
- Implantation of the source and drain
- Cuts for making contacts
- Metallization
- By using the above steps we can fabricate CMOS using twintub process method.


p+
p+
n+
n+
n-well
p-well
Epitaxy
N-Substrate