Unit 1
Design Rules and Stick Diagrams

Stick Diagrams

- VLSI design aims to translate circuit concepts onto silicon
- stick diagrams are a means of capturing topography and layer information - simple diagrams
- Stick diagrams convey layer information through colour codes (or monochrome encoding
- Used by CAD packages, including Microwind

Design Rules

- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducable

Lambda Based Design Rules

- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Design Rules - The Reality

- Manufacturing processes have inherent limitations in accuracy and repeatability
- Design rules specify geometry of masks that provide reasonable yield
- Design rules are determined by experience

Problems - Manufacturing

- Photoresist shrinking / tearing
- Variations in material deposition
- Variations in temperature
- Variations in oxide thickness
- Impurities
- Variations between lots
- Variations across the wafer

Problems - Manufacturing

- Variations in threshold voltage
  - oxide thickness
  - ion implantation
  - poly variations
- Diffusion - changes in doping (variation in R, C)
- Poly, metal variations in height and width -> variation in R, C
- Shorts and opens
- Via may not be cut all the way through
- Undersize via has too much resistance
- Oversize via may short

Meta Design Rules

- Basic reasons for design rules
- Rules that generate design rules
- Under worst case misalignment and maximum edge movement of any feature, no serious performance degradation should occur

VLSI DESIGN RULES

$\lambda = 1\mu m$

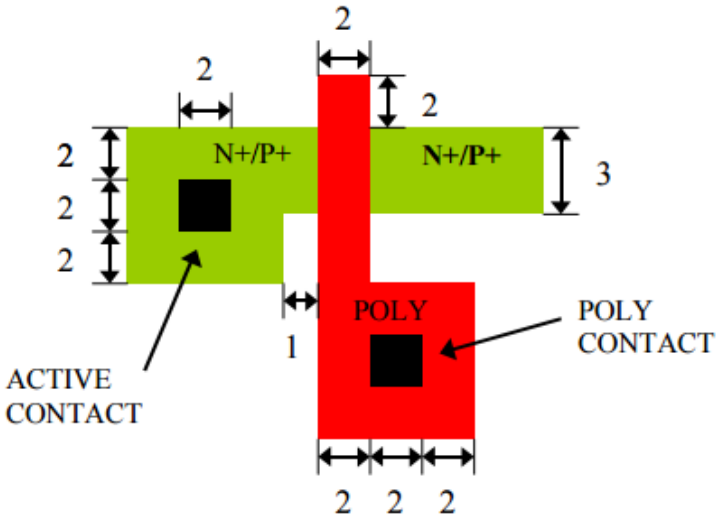
MINIMUM WIDTH AND SPACING RULES

LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
ACTIVE	Minimum Width Minimum Spacing	3λ 3λ
NSELECT	Minimum Width Minimum Spacing	3λ 3λ
PSELECT	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

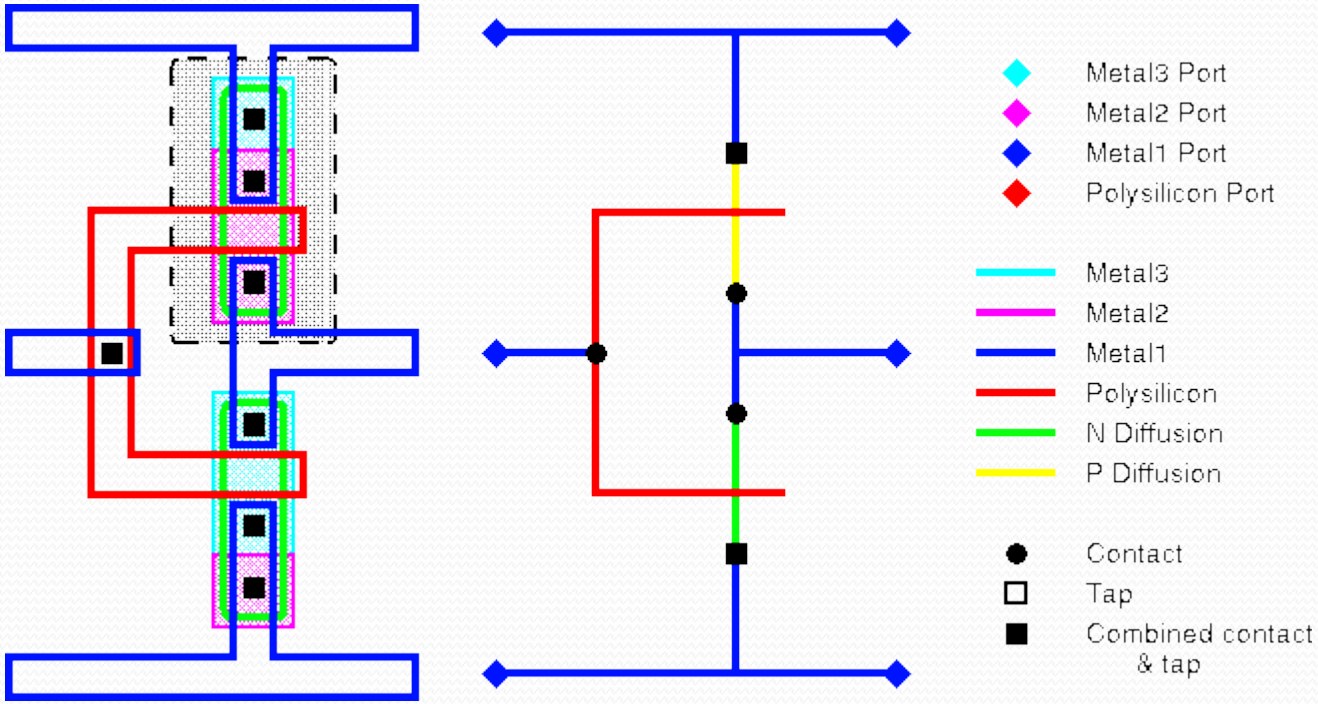
VLSI DESIGN RULES (Contd.)

MOSFET LAYOUT RULES

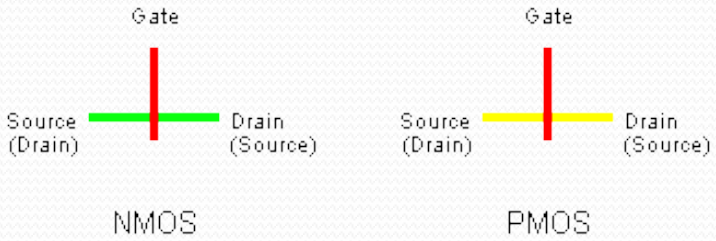
RULE	MEANING	VALUE
POLY Overlap	Minimum extension over ACTIVE	2λ
POLY-ACTIVE	Minimum Spacing	1λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
ACTIVE CONTACT	Exact Size Minimum Space to ACTIVE Edge	2λ x 2λ 2λ
POLY CONTACT	Exact Size Minimum Space to POLY Edge	2λ x 2λ 2λ



Stick Diagram and Mask Layout Design of CMOS Inverter

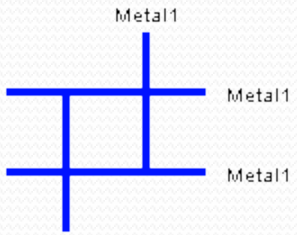


- **Transistors**
- A transistor exists where a polysilicon stick crosses either an N diffusion stick (NMOS transistor) or a P diffusion stick (PMOS transistor).

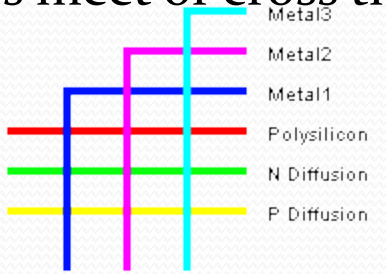


- There is no difference in the construction of a transistor source and a transistor drain. The source is determined as the source of conductors (electrons for NMOS / holes for PMOS) when current flows through the channel. In some pass transistor circuits, the source and drain may swap over during use.

- **Implied Connections and Crossovers:**
- Where two sticks of the same colour meet or cross there is always a connection.
- Where two sticks of different colours meet or cross there is no implied connection.



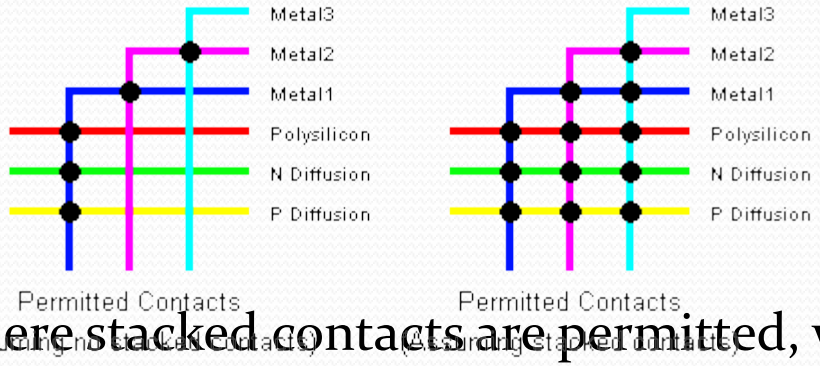
Conductors Join



Conductors Cross
(No Connection)

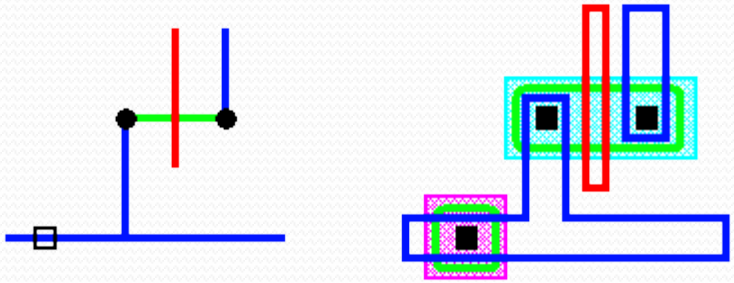
- N and P diffusions may not cross each other. Where poly crosses diffusion we have a transistor.

- **Contacts**
- A connection may be explicitly defined using a filled black circle. In the general case a connection is permitted where the mask layers will be separated by just one layer of insulator (through which a "contact cut" may be defined). Thus P diffusion may connect to Metal1 but not directly to Metal2.



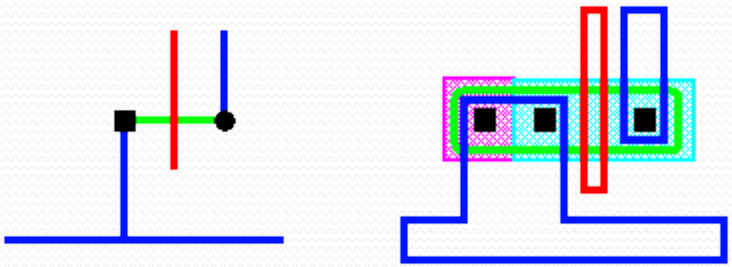
- In a process where stacked contacts are permitted, we may draw a contact between non-adjacent conductors; e.g. between Poly and Metal3, in which case the connection to intermediate layers (Metal1 and Metal2) is implied.

- **Taps**
- The tap represents a connection to something we can't see; either the N-Well (not shown on our stick diagram) or the wafer substrate. A tap is defined using an unfilled black square. Here there will be only one conductor crossing the square (Metalı power or ground rail).



- An N-Well Tap is inferred where the connection is from a power rail while a Substrate Tap is inferred where the connection is from a ground rail.

- **Combined Contacts & Taps**
- We can often save space by using a combined contact and tap. Here the tap shares the same Active Area as the contact. A combined contact and tap is defined using a filled black square in place of the source contact (filled black circle).



- A combined contact and tap can only be used where the end of a diffusion stick coincides with a contact to the power or ground rail.

- **Stick Diagram Colour Code**

P diffusion	**:**	**Yellow/Brown**		**Metal1**	**:**	**Blue**
N diffusion	:	Green		Metal2	:	Magenta/Purple
Polysilicon	:	Red		Metal3	:	Cyan/L.Blue
Contacts & Taps	:	Black				

- In case of deviation from these colours, there is a need to include a key with your stick diagram.

Advantages of Generalised Design Rules

- Ease of learning because they are scalable, portable, durable
- Longlevity of designs that are simple, abstract and minimal clutter
- Increased designer efficiency
- Automatic translation to final layout