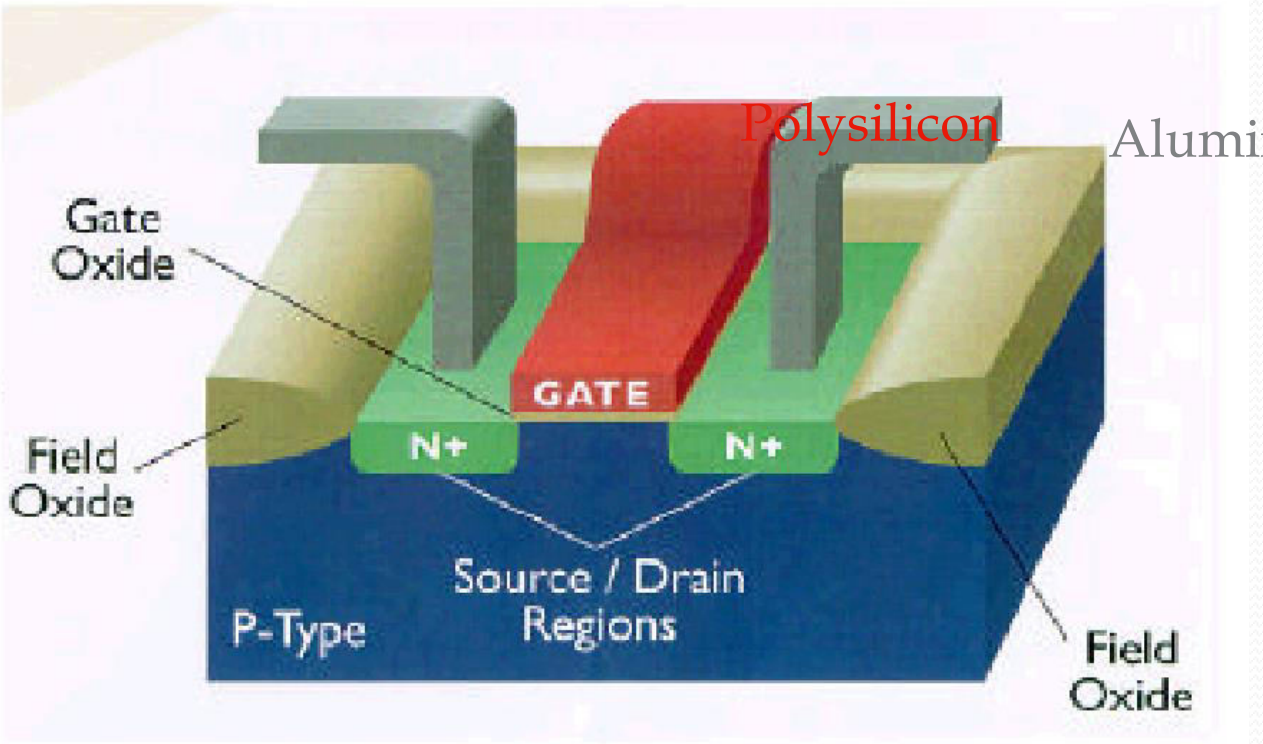
Unit 1
The MOS Transistor

The MOS Transistor

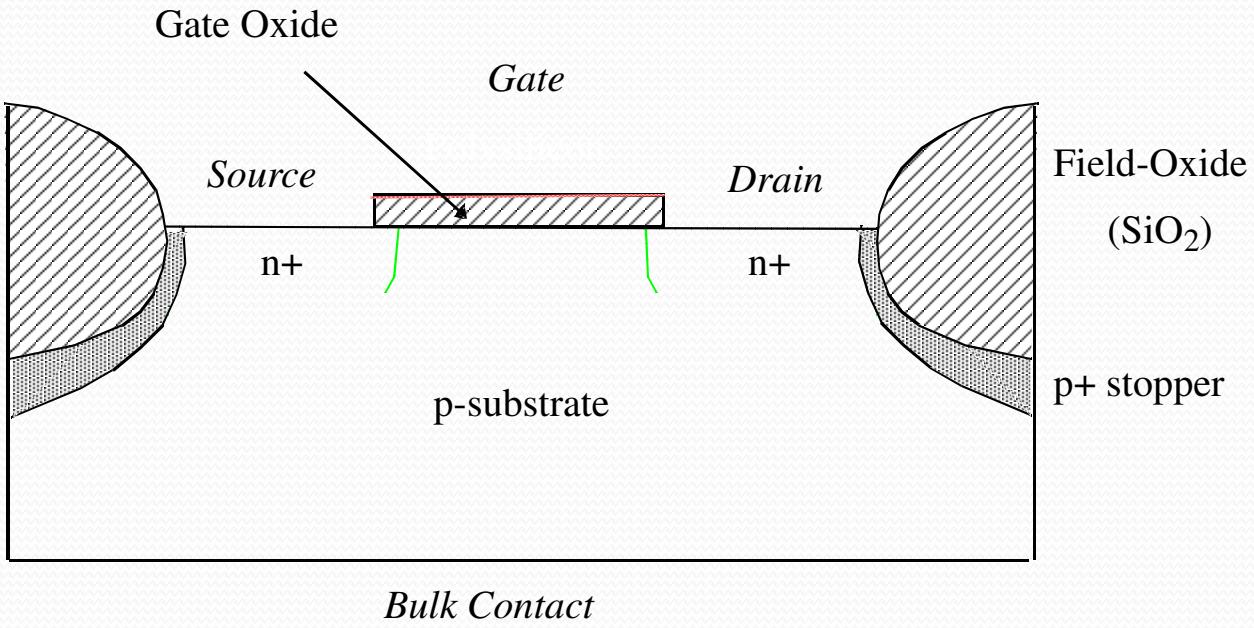


JFET – Junction Field Effect Transistor

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

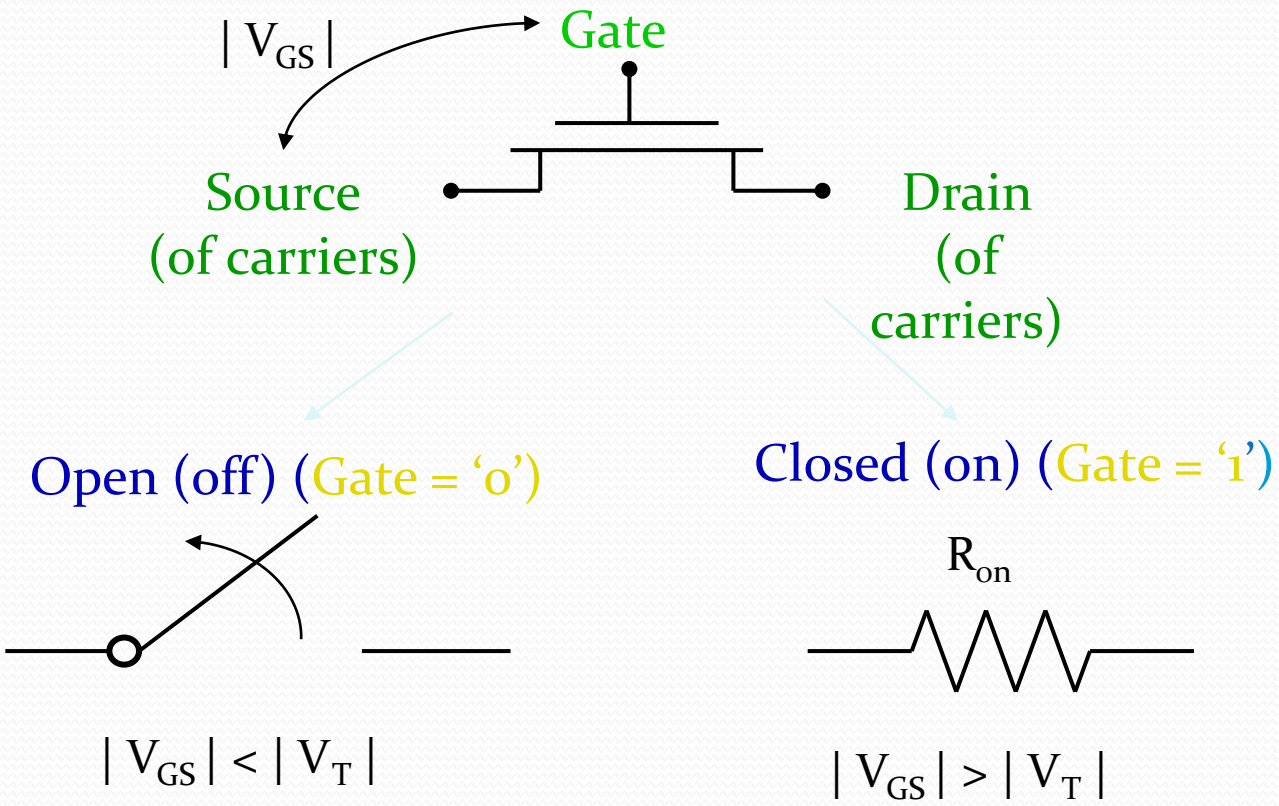
n-channel MOSFET (nMOS) & p-channel MOSFET (pMOS)

The MOS Transistor

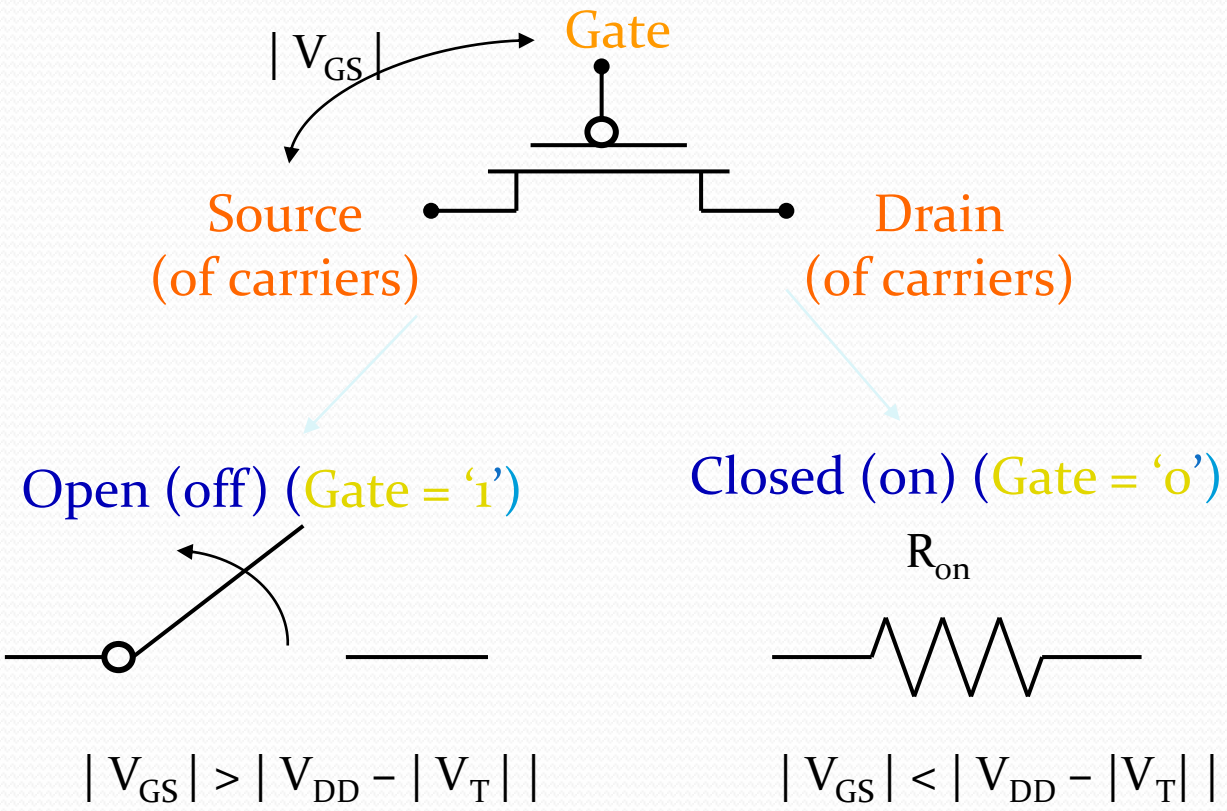


CROSS-SECTION of NMOS Transistor

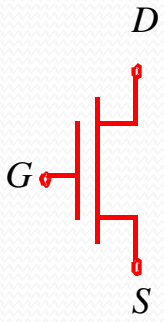
Switch Model of NMOS Transistor



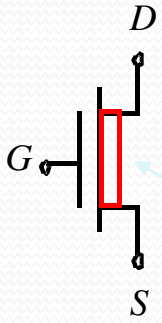
Switch Model of PMOS Transistor



MOS transistors Symbols

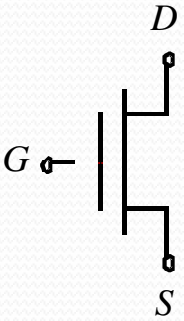


NMOS Enhancement

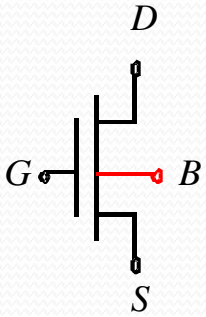


NMOS Depletion

Channel

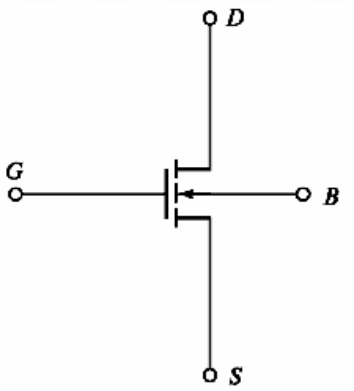


PMOS Enhancement



NMOS with Bulk Contact

JFET and MOSFET Transistorsor



Symbol

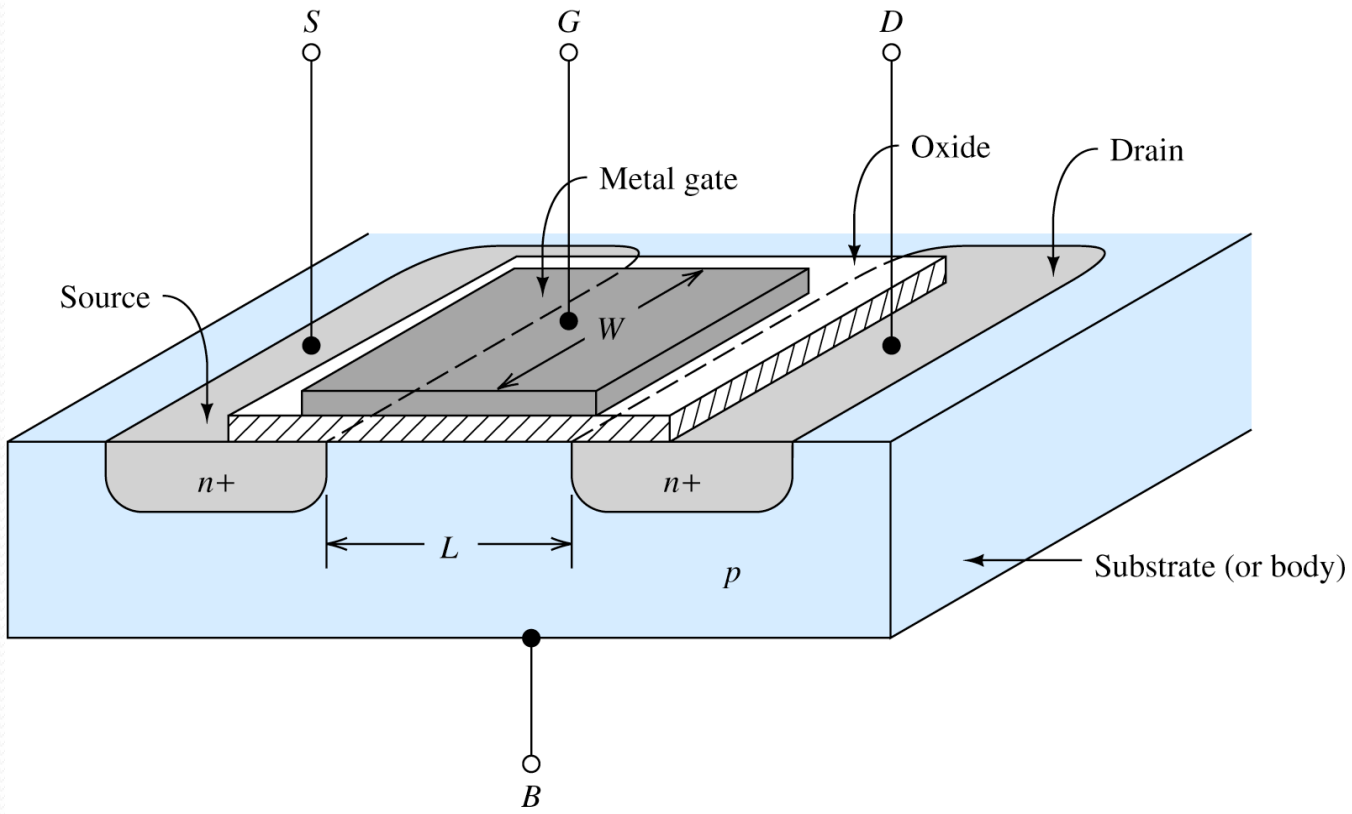


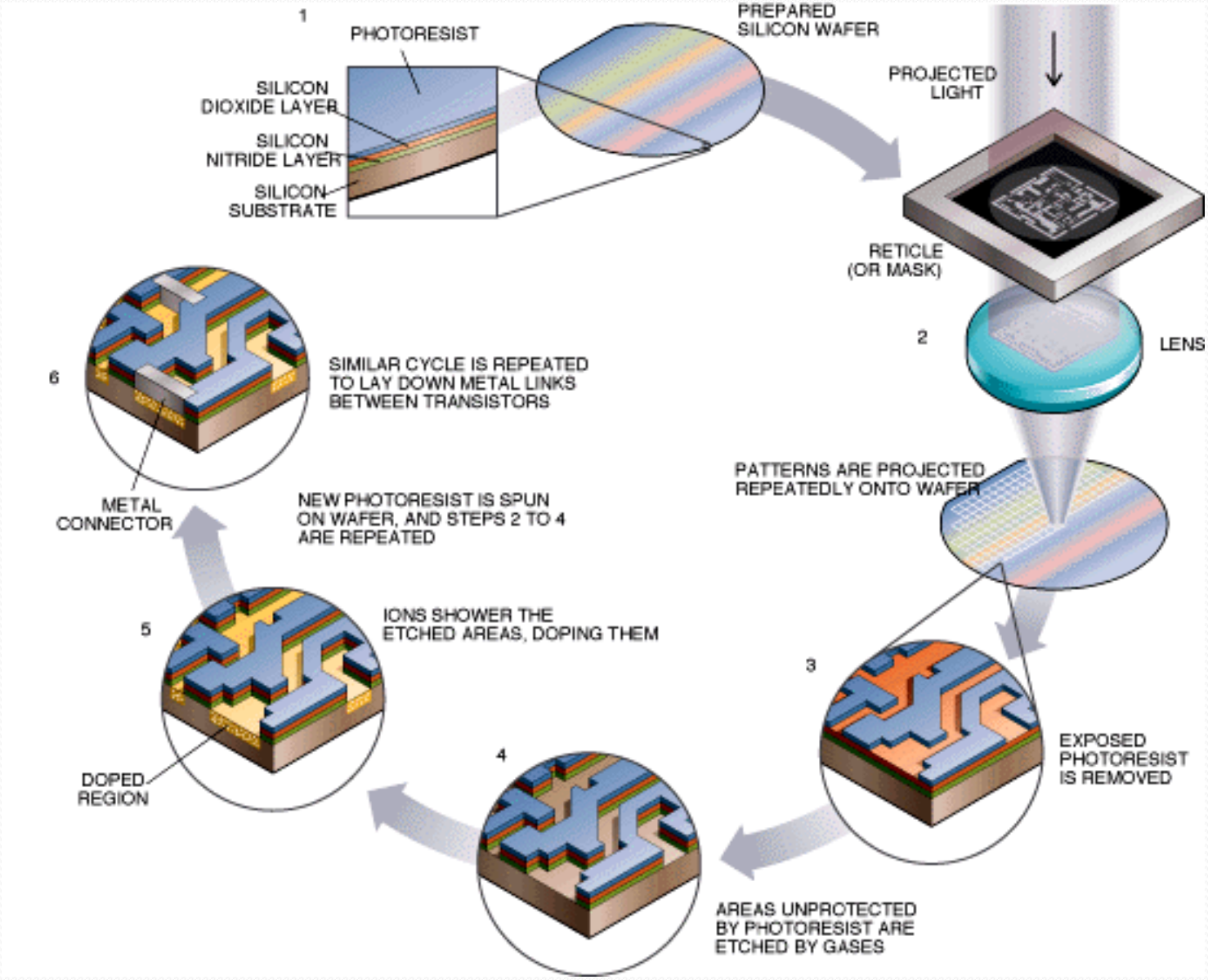
Figure 12.1 n-channel enhancement MOSFET showing channel length L and channel width W.

L = 0.5-10 μm
W = 0.5-500 μm

SiO_2 Thickness = 0.02-0.1 μm

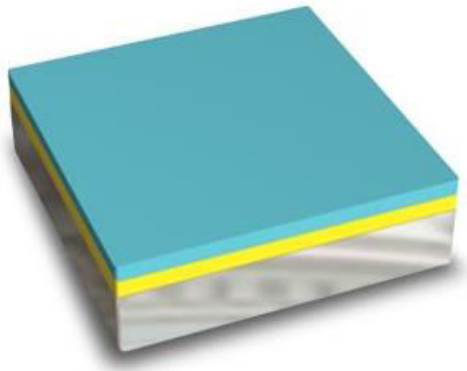
Device characteristics depend on L,W, Thickness, doping levels

MOSFET Transistor Fabrication Steps

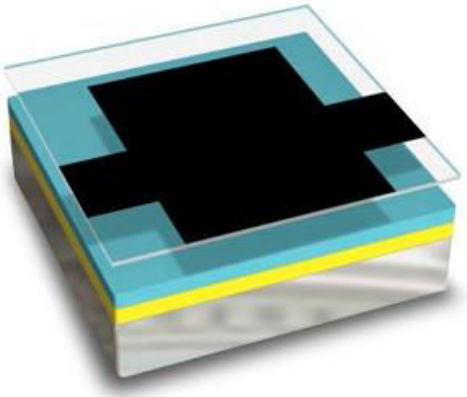


Building A MOSFET Transistor Using Silicon

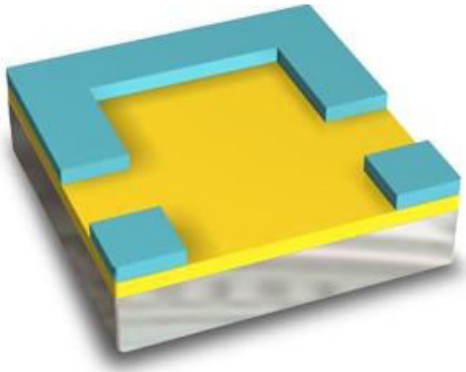
The positively doped silicon wafer is first coated with an insulating layer of silicon dioxide (yellow) through chemical vapor deposition.



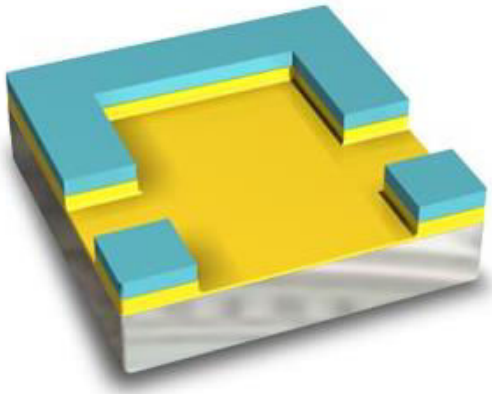
An ultraviolet light-sensitive thin layer of photoresist (blue) is applied to the silicon dioxide surface and evenly spread across the wafer.



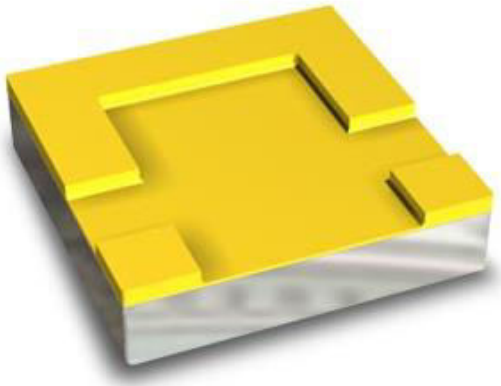
The first mask is placed over the wafer and ultraviolet light is projected onto the mask. Areas of photoresist exposed to the light are hardened and those shielded remain soft.



The unexposed (and soft) photoresist is removed by washing with a solvent, leaving the hardened resist and underlying silicon dioxide layer intact.

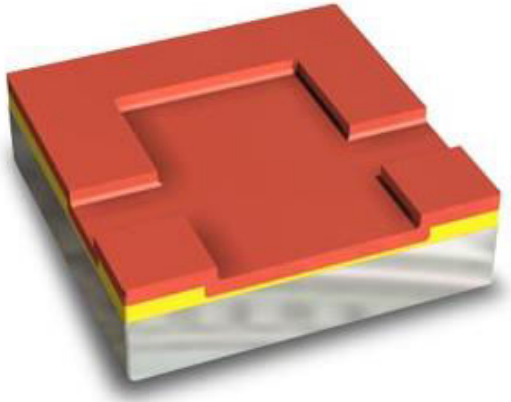


The upper layer of the silicon dioxide is removed by etching with hot gasses, leaving only a very thin layer for insulation.

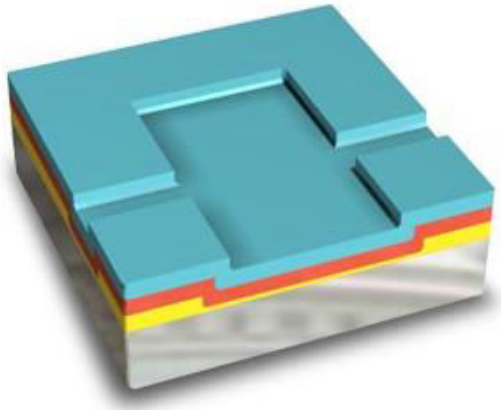


The hardened photoresist is removed with a chemical solvent leaving an uneven silicon dioxide surface over the entire wafer.

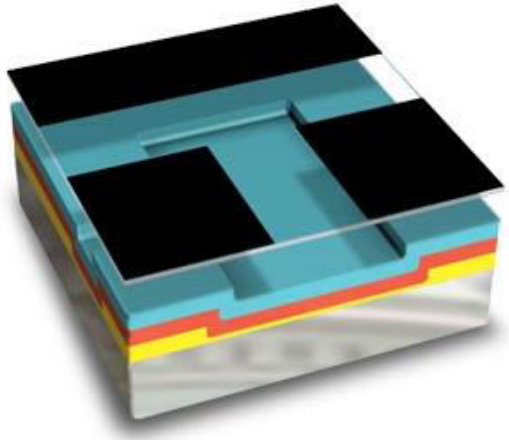
http://micro.magnet.fsu.edu/electromag/java/transistor/index.html



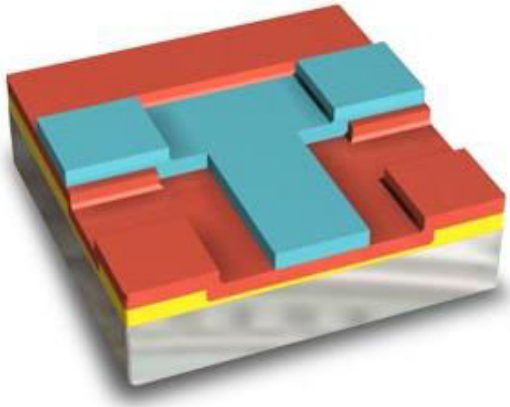
A layer of polysilicon is then deposited onto the silicon dioxide surface using chemical vapor deposition. This material will serve as the transistor's gate.



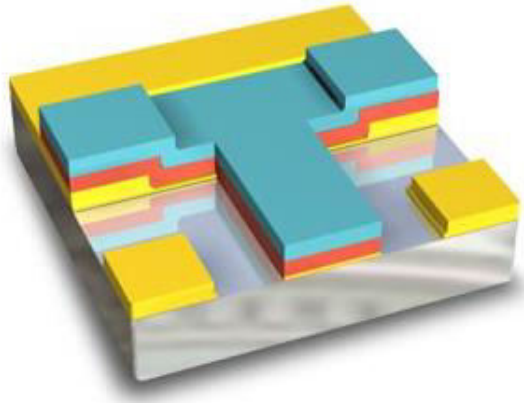
A second layer of photoresist is applied over the polysilicon to prepare the wafer's surface for a second photomask.



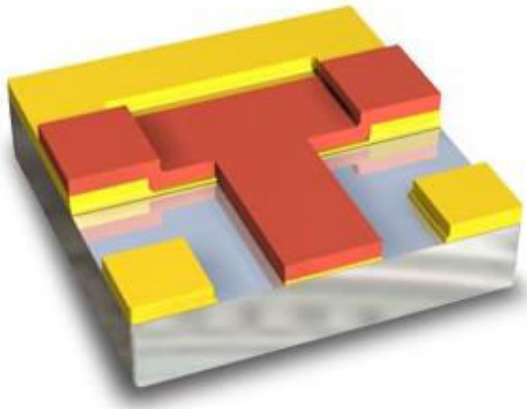
The second mask is placed over the wafer and ultraviolet light is again projected onto the mask. The areas exposed to the light are hardened.



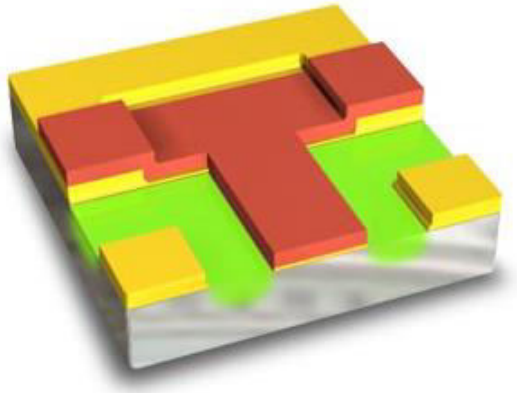
The unexposed photoresist is washed away with a solvent, leaving only the L-shaped hardened resist on the wafer.



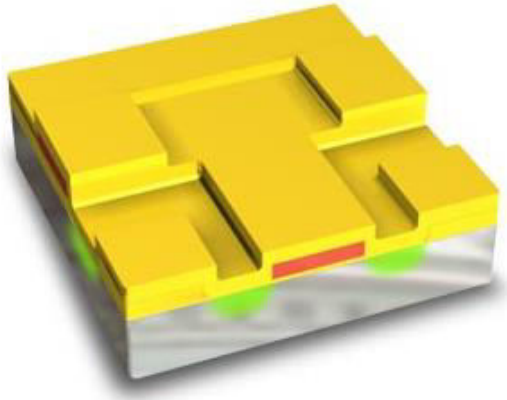
The next step is ion-beam milling (etching) to remove the excess polysilicon and another thin layer of silicon dioxide exposing the silicon wafer's surface.



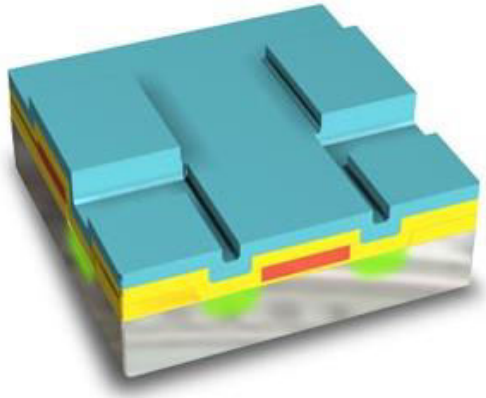
The photoresist is removed with solvent leaving a ridge of polysilicon (the transistor's gate), which rises above the silicon wells.



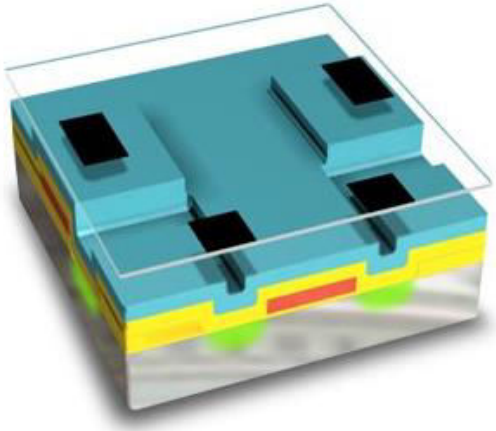
Chemical doping implants phosphorous (green) deep within the silicon wells surrounded by the silicon dioxide and polysilicon layers to produce positively doped silicon.



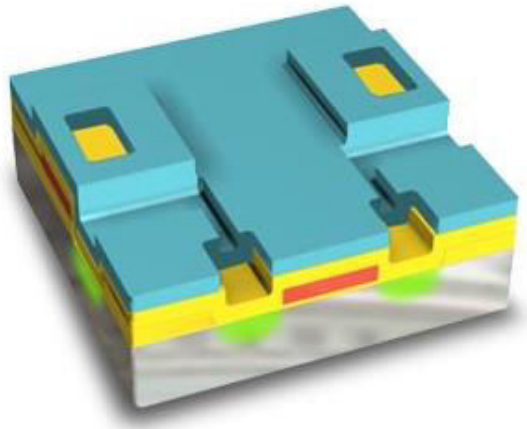
a second layer of silicon dioxide is applied to provide insulation of the basic transistor structure from metal contacts to be applied later.



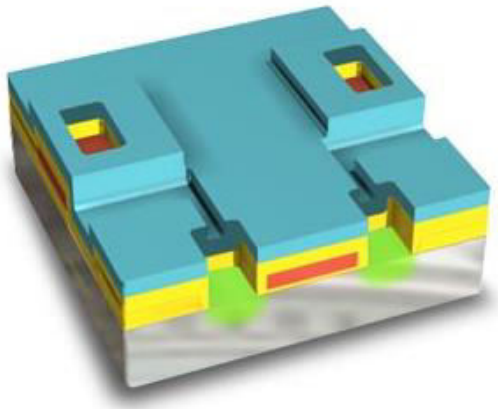
A third film of photoresist is added to prepare the formation of vertical shafts (vias) that will contain metal contacts for the polysilicon and the wells.



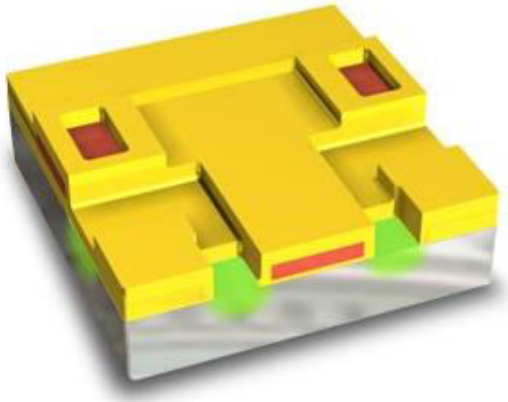
The third mask is illuminated with ultraviolet light, hardening the photoresist everywhere with the exception of small black rectangles that will become shafts.



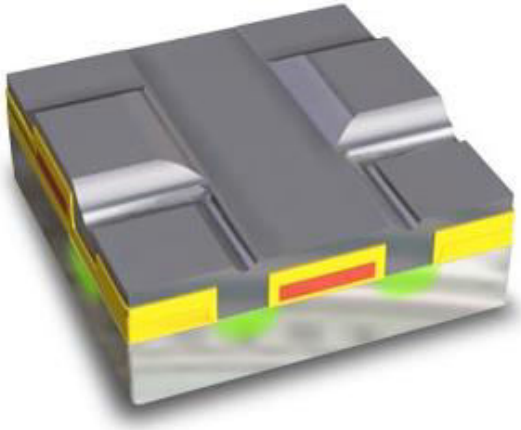
Removal of the soft photoresist with solvent exposes three areas of exposed silicon dioxide that mark the planned shafts.



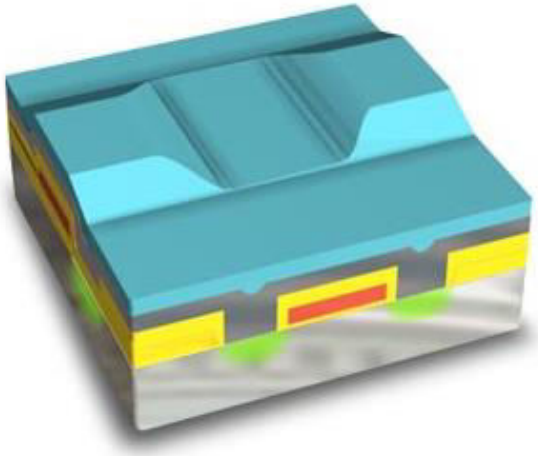
The wafer is next etched again to remove silicon dioxide and exposing the positively doped silicon and the polysilicon gate.



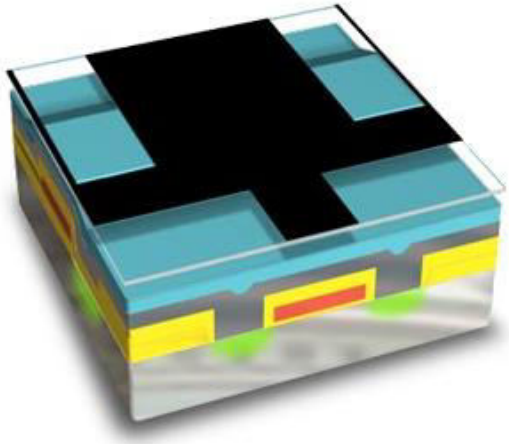
The remaining photoresist is then washed away with solvent. The positively doped silicon areas (green) will serve as the source and the drain.



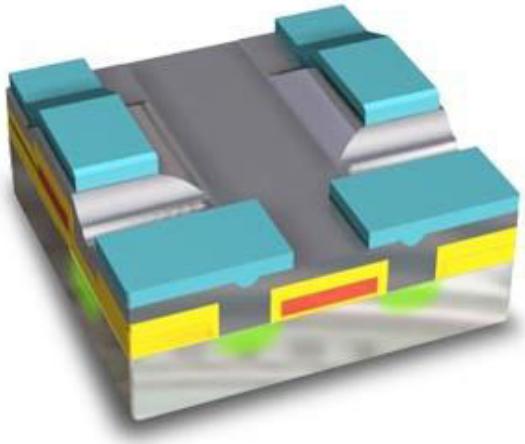
The wafer is then sputter-coated with aluminum that fills the shafts and evenly coats the wafer's surface to provide electrical contacts.



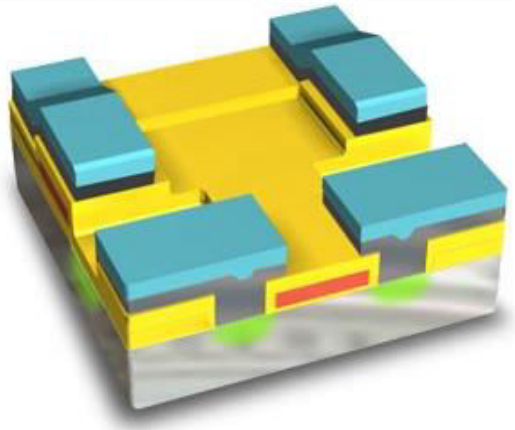
A fourth layer of photoresist is applied to the wafer to prepare the transistor for its final mask, which will produce the pattern for the aluminum "wiring".



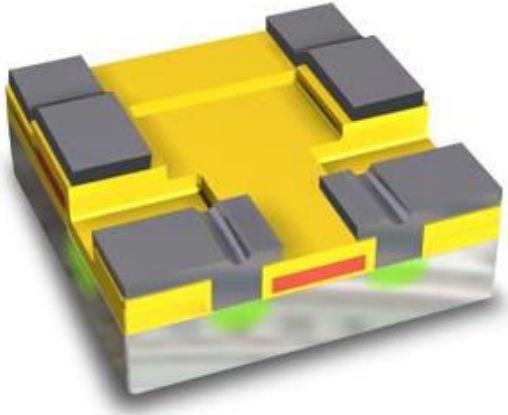
Ultraviolet light shining through the metallization mask hardens the photoresist covering the aluminum, which will carry current to and from the transistor.



The unexposed photomask is removed with solvent, exposing many bare regions of aluminum that will be removed next.

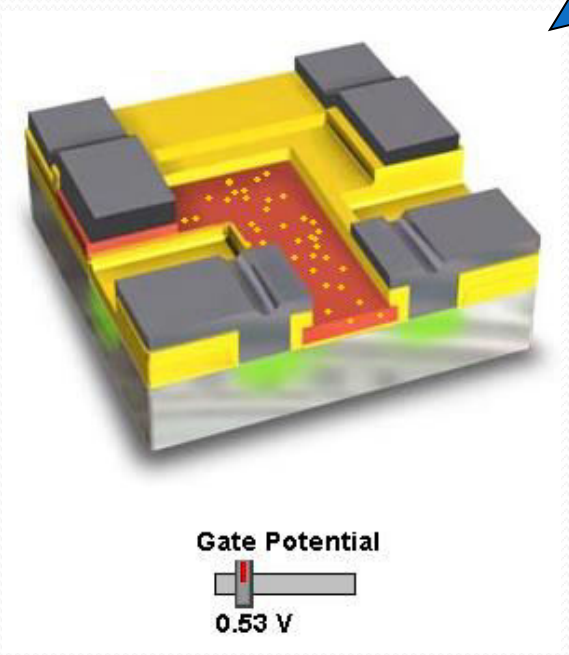


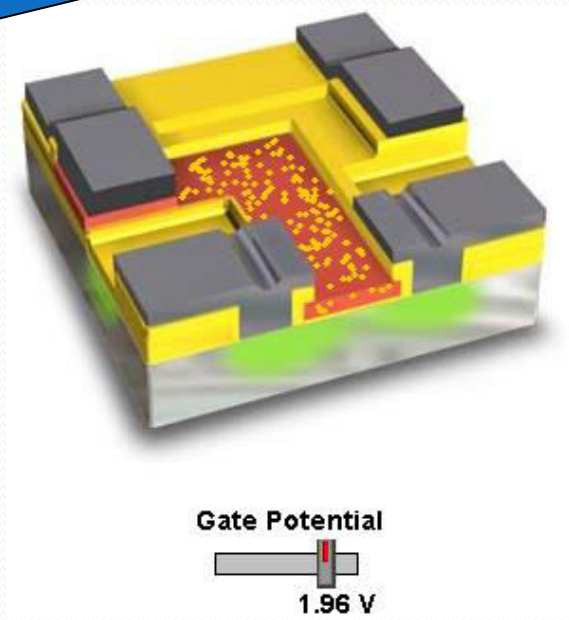
A final etching step removes exposed aluminum leaving only the metal necessary to make contacts in the shafts and connectors on the surface.

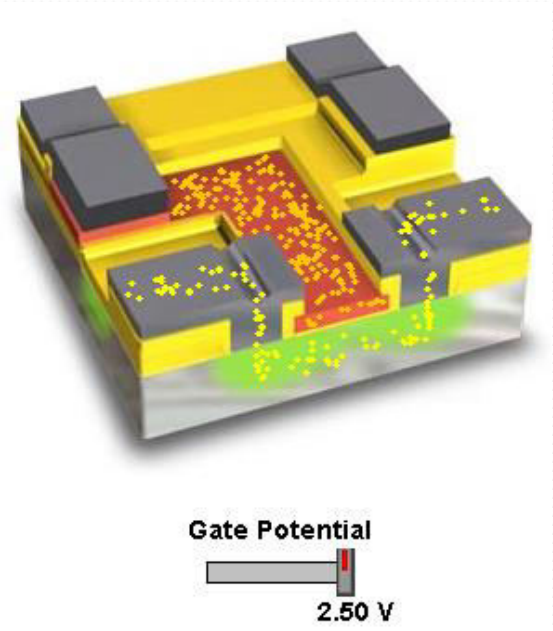


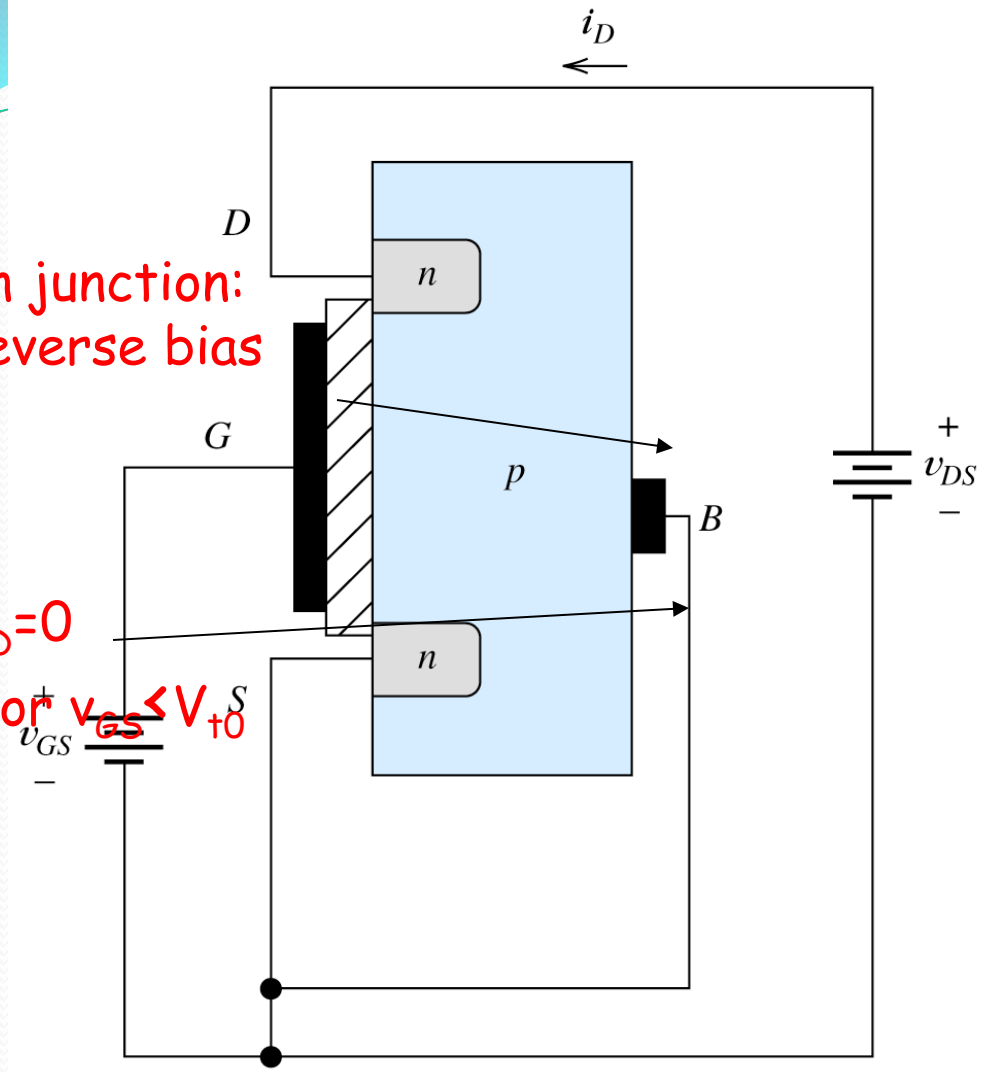
The last resist is washed away with solvent and the transistor is finished, along with millions of its neighbors on the wafer.

It is done. Now, how does it work?



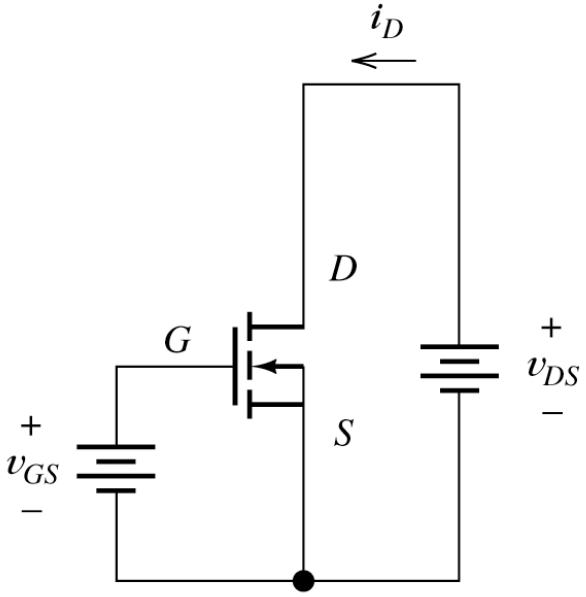






pn junction:
reverse bias

i_D=0
for $v_{GS} < V_{t0}$



Schematic

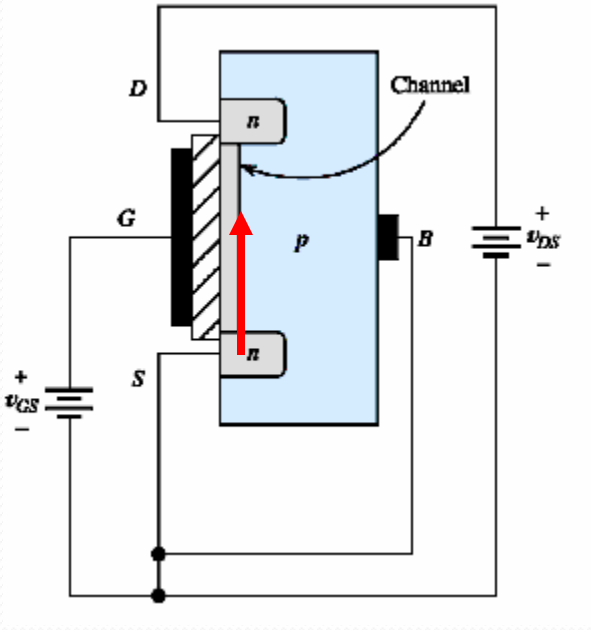
Figure 12.3 For $v_{GS} < V_{to}$, the pn junction between drain and body is reverse biased and $i_D = 0$.

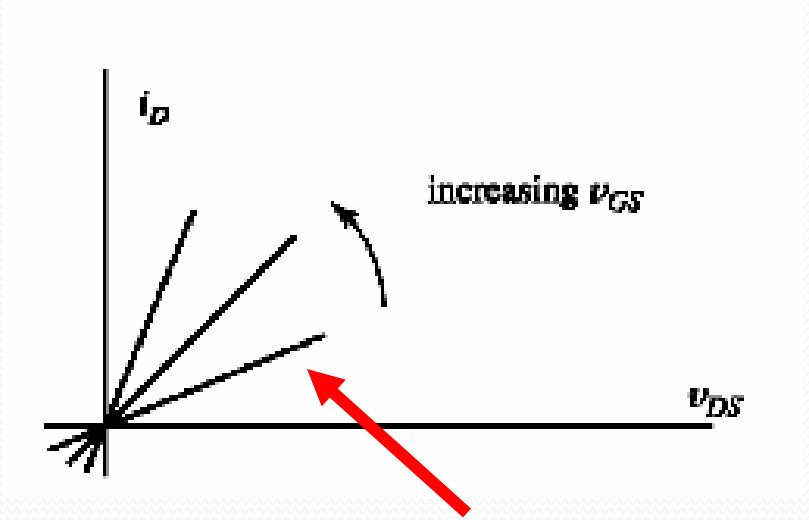
When v_{GS}=0 then i_D=0 until v_{GS}>V_{t0} (V_{t0} -threshold voltage)

n-channel MOSFET Basic Operation

Operation in the Triode Region

For $v_{DS} < v_{GS} - V_{t0}$ and $v_{GS} > V_{t0}$ the NMOS is operating in the triode region



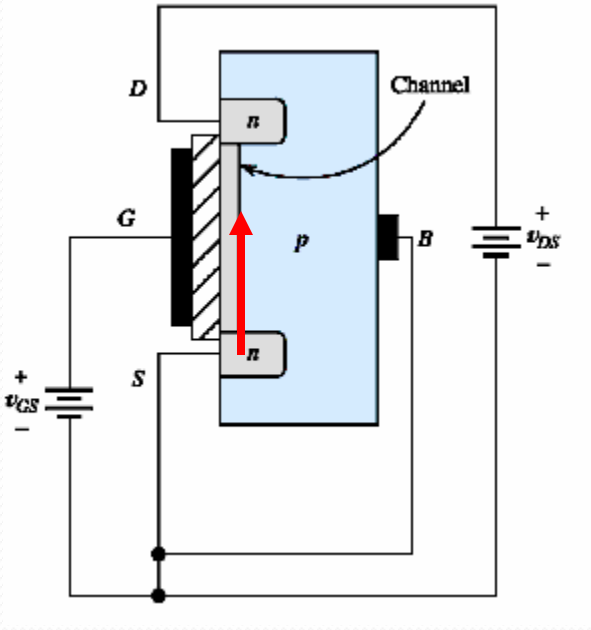


Resistor like characteristic
(R between S & D,
Used as voltage controlled R)

For small v_{DS}, i_D is proportional to the excess voltage $v_{GS} - V_{t0}$

n-channel MOSFET Basic Operation

Operation in the Triode Region



$$i_D = K\left[2\left(v_{GS} - V_{t0}\right)v_{DS} - v_{DS}^2\right]$$

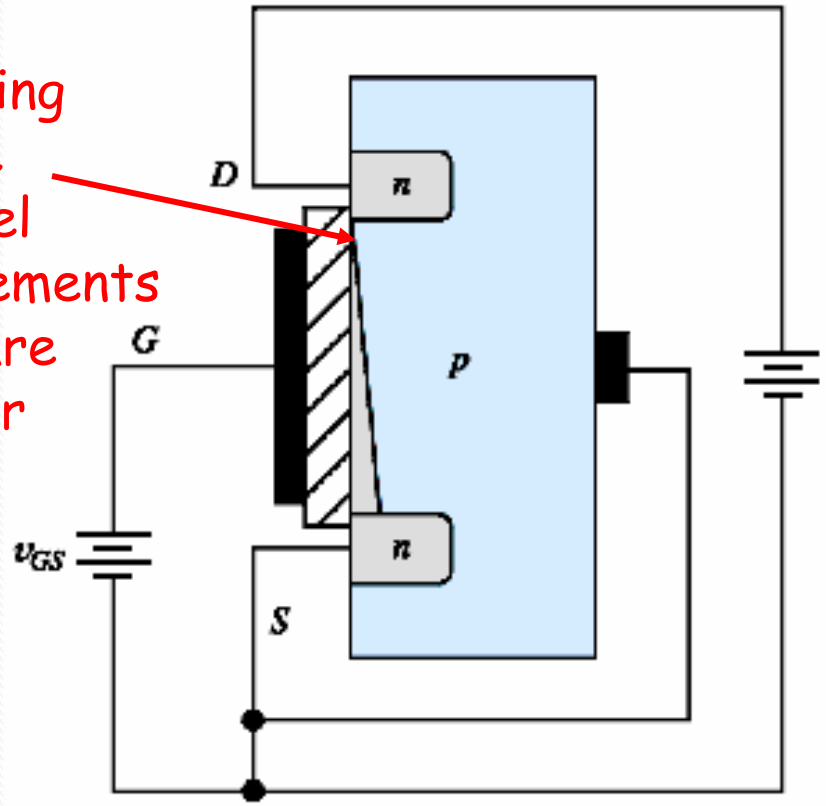
$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

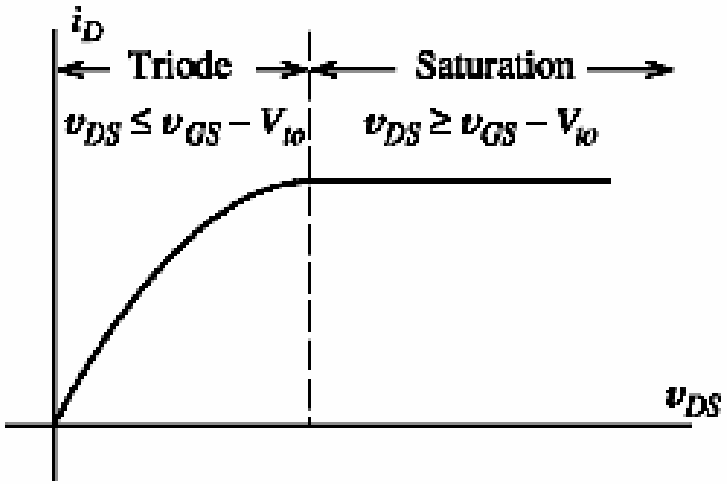
Device parameter KP for NMOSFET is 50 $\mu A/V^2$

n-channel MOSFET Basic Operation

Operation in the Saturation Region (v_{DS} is increased)

Tapering of the channel - increments of i_D are smaller when v_{DS} is larger





When $v_{GD}=V_{t0}$ then the channel thickness is 0 and

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

n-channel MOSFET Basic Operation

Example 12.1

An nMOS has W=160 μm, L=2 μm, KP= 50 μA/V² and V_{to}=2 V.

Plot the drain current characteristic vs drain to source voltage for v_{GS}=3 V.

$$i_D = K\left[2\left(v_{GS} - V_{t0}\right)v_{DS} - v_{DS}^2\right]$$

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

n-channel MOSFET Basic Operation

Example 12.1

Channel length modulation

i_d depends on v_{DS} in saturation region

(approx: i_D =const in saturation region)

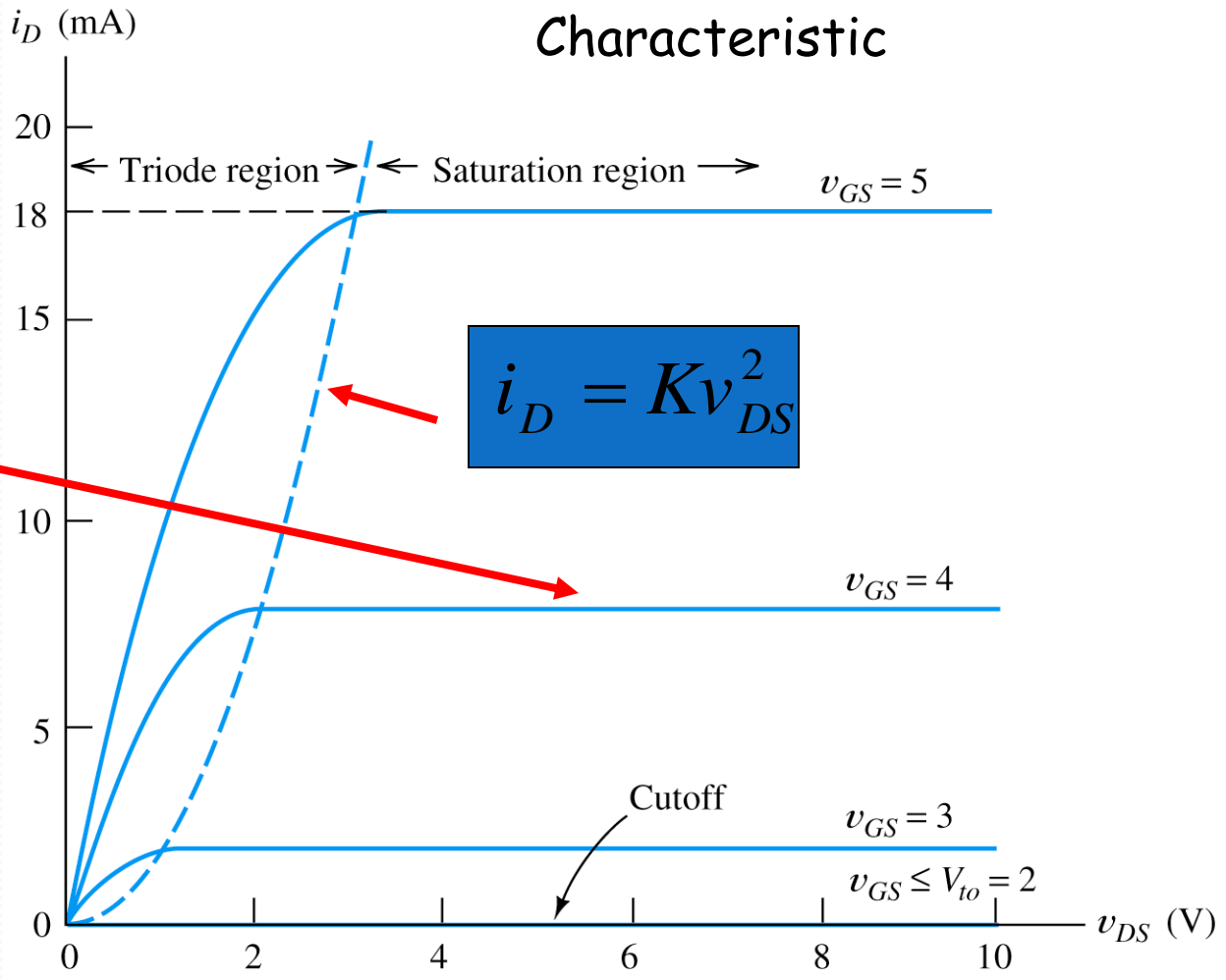


Figure 12.6 Characteristic curves for an NMOS transistor.

p-channel MOSFET Basic Operation

It is constructed by interchanging the *n* and *p* regions of n-channel MOSFET.

Symbol

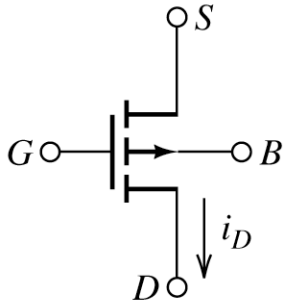


Figure 12.8 Circuit symbol for PMOS transistor.

Characteristic

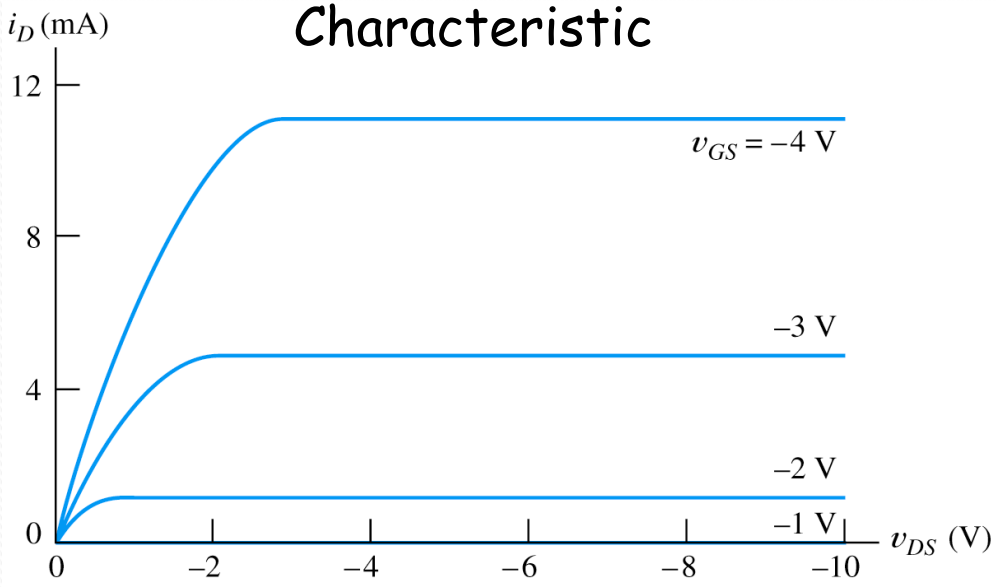
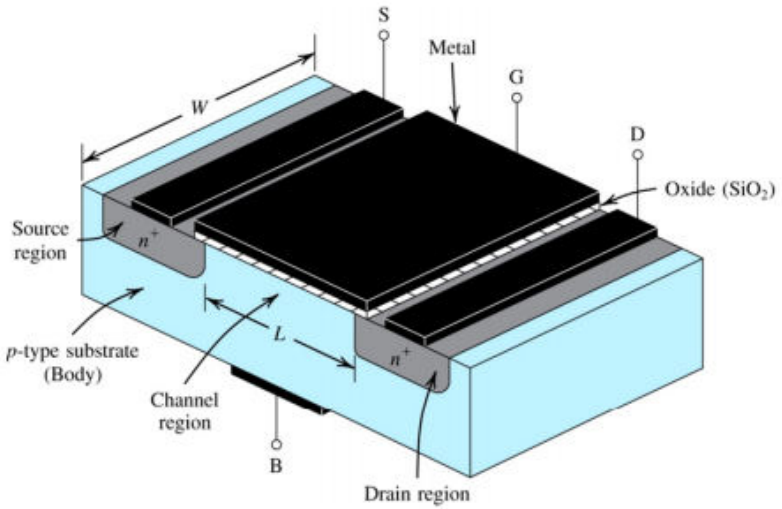


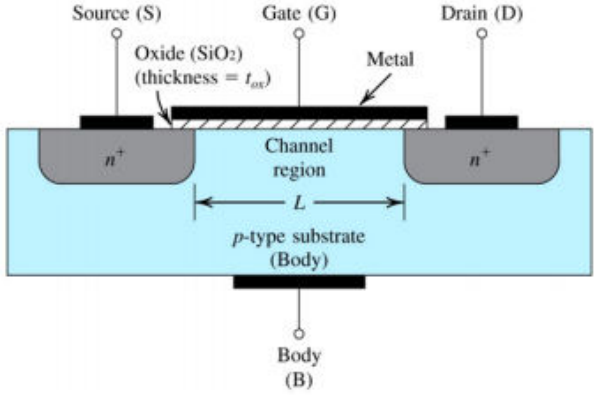
Figure 12.9 Answer for Exercise 12.3.

How does p-channel MOSFET operate?
-voltage polarities
-i_D current
-schematic

MOS FIELD-EFFECT TRANSISTORS (MOSFETs)

Device structure of MOSFET





- "MOS" ≡ metal-oxide-semiconductor structure.
- MOSFET is a four-terminal device: gate (G), source (S), drain (D) and body (B).
- The device size (channel region) is specified by channel width (W) and channel length (L).
- Two kinds of MOSFETs: n-channel (NMOS) and p-channel (PMOS) devices
- The device structure is basically symmetric in terms of drain and source.
- Source and drain terminals are specified by the operation voltage.

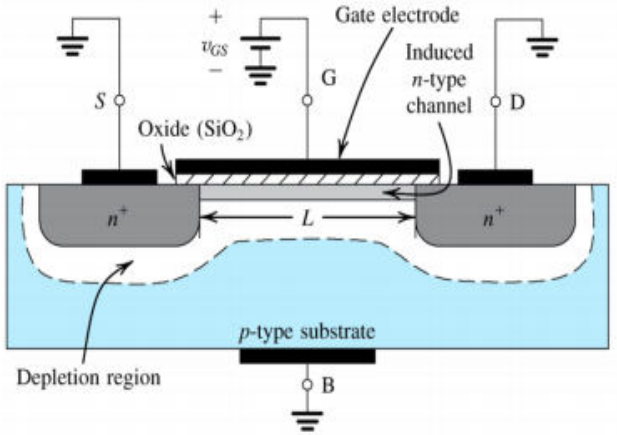
M

Operation with zero gate voltage

- The MOS structure form a parallel-plate plate capacitor with gate oxide layer in the middle.
- Two *pn* junctions (S-B and D-B) are connected as back to back diodes.
- The source and drain terminals are isolated by two depletion regions without conducting current.
- The operating principles will be introduced by using the *n*-channel MOSFET as an example.

Creating a channel for current flow

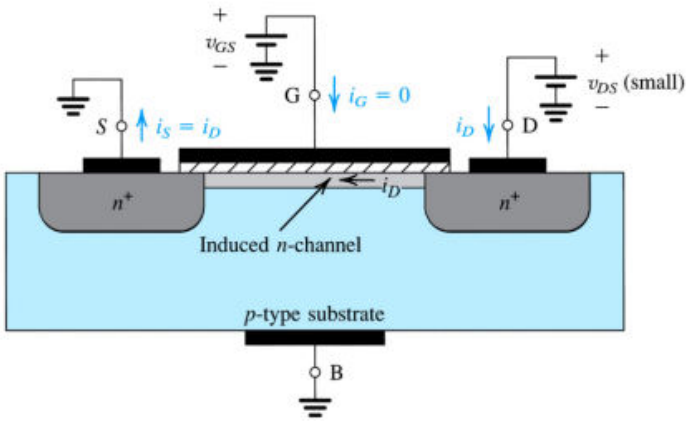
- Positive charges accumulate in gate as a positive voltage applies to gate electrode.
- The electric field forms a depletion region by pushing holes in *p*-type substrate away from the surface.
- Electrons start to accumulate on the substrate surface as gate voltage exceeds a **threshold voltage** V_t.
- The induced *n* region thus forms a **channel** for current flow from drain to source.
- The channel is created by inverting the substrate surface from *p*-type to *n*-type → **inversion layer**.
- The field controls the amount of charge in the channel and determines the channel conductivity.

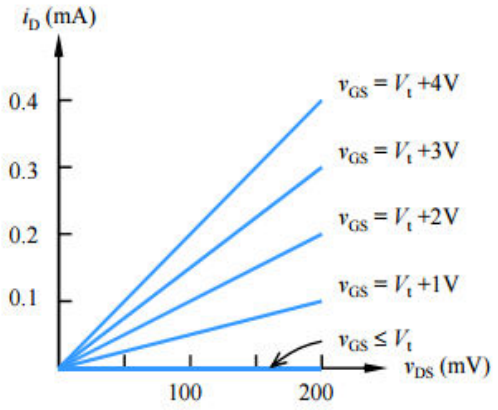


The MOS System under external b

Applying a small drain voltage

- A positive $v_{GS} > V_t$ is used to induce the channel and it is called *n*-channel **enhancement-type** MOSFET.
- Free electrons travel from source to drain through the induced *n*-channel due to a small v_{DS}.
- The resulting current i_D flows from drain to source (opposite to the direction of the flow of negative charge).
- The current is proportional to the number of carriers in the induced channel.
- The channel is controlled by the **effective voltage** or **overdrive voltage**: $v_{OV} \equiv v_{GS} - V_t$
- The electron charge in the channel due to the overdrive voltage: $|Q| = C_{ox}WLv_{OV}$
- **Gate oxide capacitance** C_{ox} is defined as capacitance per unit area.
- MOSFET can be approximated as a linear resistor in this region with a resistance value inversely proportional to the excess gate voltage.





Operation as increasing drain voltage

- As v_{DS} increases, the voltage along the channel increases from 0 to v_{DS}, and the voltage between the gate and the points along the channel decreases from v_{GS} at the source end to $(v_{GS} - v_{DS})$ at the drain end.
- Since the inversion layer depends on the voltage difference across the MOS structure, increasing v_{DS} will result in a tapered channel.
- The resistance increases due to tapered channel and the i_D-v_{DS} curve does not continue as a straight line.
- At the point $v_{DSsat} = v_{GS} - V_t$, the channel is **pinched off** at the drain side.
- Increasing v_{DS} beyond this value has little effect on the channel shape and i_D saturates at this value.
- **Triode region**: $v_{DS} < v_{DSsat}$
- **Saturation region**: $v_{DS} \geq v_{DSsat}$