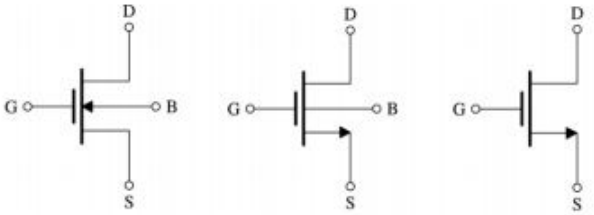
Unit 1
Current-Voltage Characteristics

Current-Voltage Characteristics

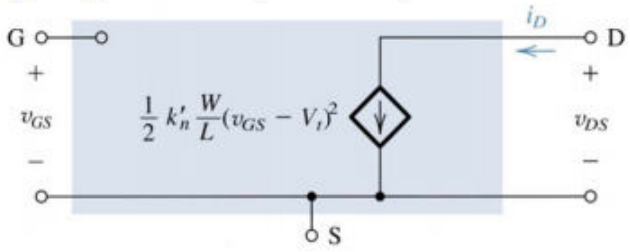
Circuit symbol

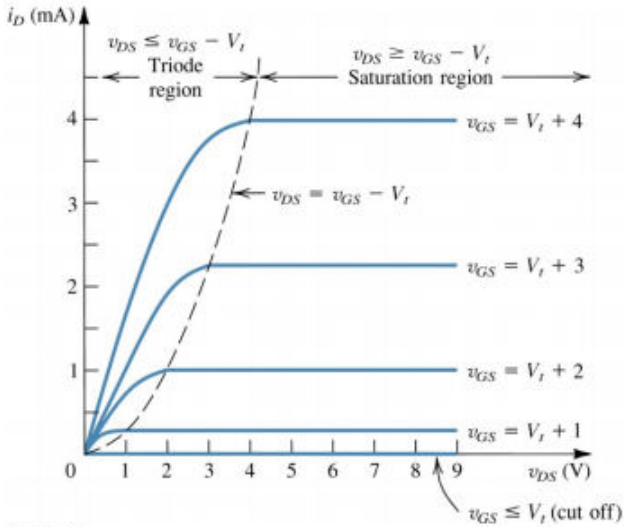
- *n*-channel enhancement-mode MOSFET

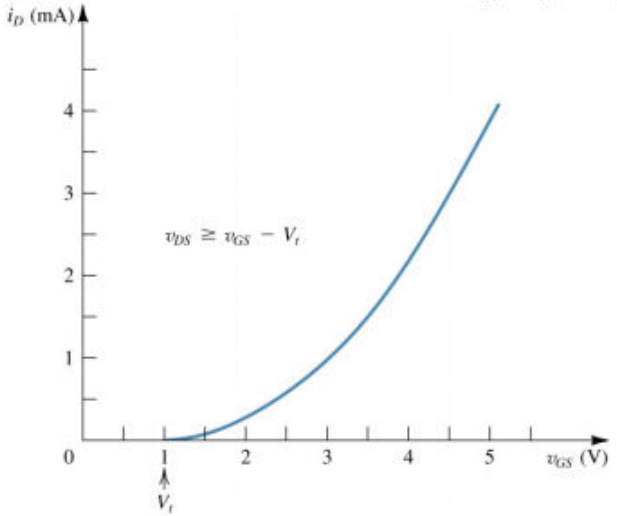


The current-voltage characteristics

- Cut-off region: $(v_{GS} \le V_t)$
  - ➔ $i_D = 0$
- Triode region: $(v_{GS} > V_t \text{ and } v_{DS} < v_{GS} - V_t)$
  - ➔ $i_D = \mu_n C_{ox} \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$
- Saturation: $(v_{GS} > V_t \text{ and } v_{DS} \ge v_{GS} - V_t)$
  - ➔ $i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)^2$
- large-signal model (saturation)







Derivation of the I-V relationship

- Induced charge in the channel due to MOS capacitor:

$$Q_I(x) = -C_{ox}[v_{GS} - V_t - v(x)]$$

- Equivalent resistance dR along the channel:

$$dR = \frac{dx}{qn(x)\mu_n h(x)W} = \frac{dx}{\mu_n W Q_I(x)}$$

- I-V derivations:

$$dv = i_D dR = \frac{i_D dx}{\mu_n W Q_I(x)} = \frac{i_D dx}{\mu_n C_{ox} W[v_{GS} - V_t - v(x)]}$$

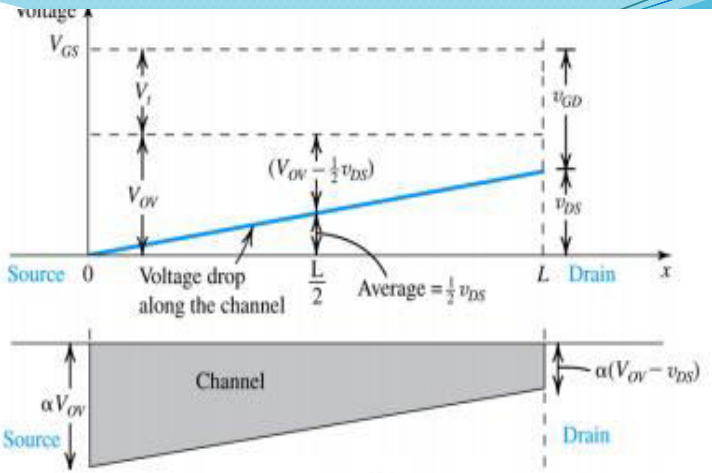
$$\int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]dv = \int_0^L i_D dx$$

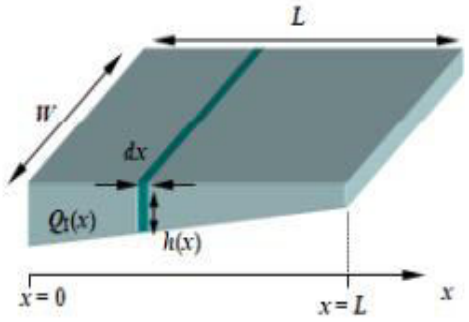
$$i_D = \mu_n C_{ox} \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

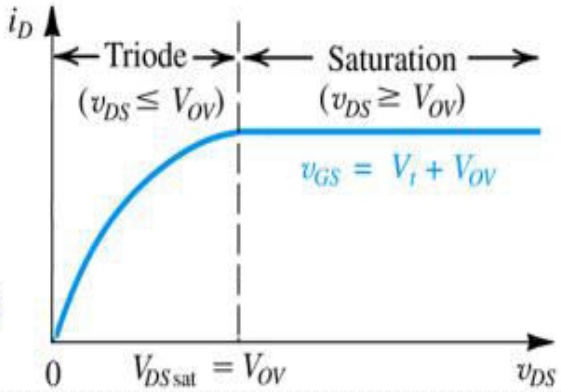
  - **Process transconductance parameter** (μA/V^2): $k'_n = \mu_n C_{ox}$
  - **Aspect ratio**: W/L
  - **Transconductance parameter** (μA/V^2): $k_n = \mu_n C_{ox}(W/L)$

- Drain current of MOSFETs:
  - Triode region: $i_D = k_n[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$
  - Saturation region: $i_{Dsat} = \frac{1}{2}k_n(v_{GS} - V_t)^2$

- On-resistance (channel resistance for small v_{DS}): $r_{DS} = 1/k_n(v_{GS} - V_t)$





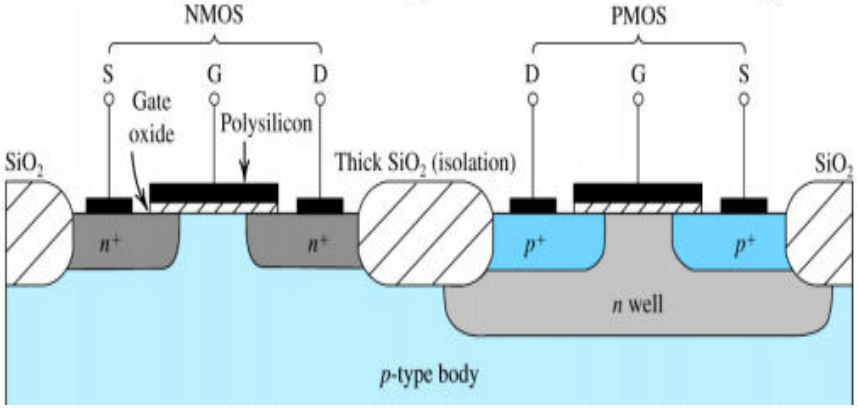


The *p*-channel enhancement-type MOSFET

- *p*-channel enhanced-type MOSFETs are fabricated on *n*-type substrate with p^+ source and p^+ drain.
- Normally, source is connected to high voltage and drain is connected to low voltage.
- As a negative voltage applies to gate electrode, negative charges accumulate in gate and the resulting field pushes electrons in *n*-type substrate away from the surface, leaving behind a carrier-depletion region.
- As gate voltage exceeds a negative **threshold voltage** V_t, holes start to accumulate on the substrate surface.
- The induced *p* region (**inversion layer**) thus forms a *p*-type channel for current flow from source to drain.
- Negative gate voltage is required to induce the channel → **enhancement-type** MOSFET.

Complementary MOS (CMOS)

- CMOS technology employs both PMOS and NMOS devices.
- If substrate is *p*-type, PMOS transistors are formed in *n* well (*n*-type body needed).
- If substrate is *n*-type, NMOS transistors are formed in *p* well (*p*-type body needed).
- The substrate and the well are connected to voltages which reverse bias the junctions for device isolation.



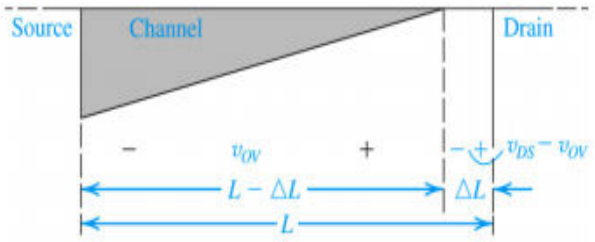
Channel length modulation

- Channel length modulation: the channel pinch-off point moves slightly away from drain as $v_{DS} > v_{DSsat}$.
- The effective channel length (L_{eff}) reduces with v_{DS}.
- Electrons travel to pinch-off point will be swept to drain by electric field.
- The length accounted for conductance in the channel is replaced by L_{eff}:

$$\int_0^{v_{GS}-V_t} k_n' W[v_{GS} - V_t - v(x)]dv = \int_0^{L_{eff}} i_D dx$$

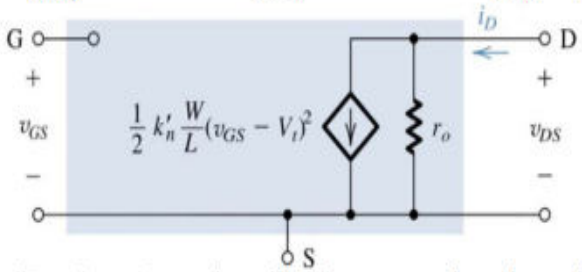
$$i_D = \frac{1}{2}k_n'\frac{W}{L_{eff}}(v_{GS}-V_t)^2 = \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2 \approx \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2\left(1+\frac{\Delta L}{L}\right)$$

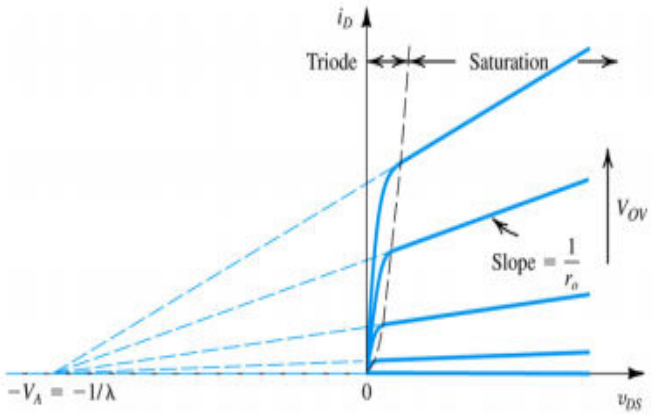
assuming that $\frac{\Delta L}{L} \propto v_{DS} \rightarrow i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS})$



Finite output resistance

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=constant} = \left[\lambda\frac{k_n'}{2}\frac{W}{L}(v_{GS}-V_t)^2\right]^{-1} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$





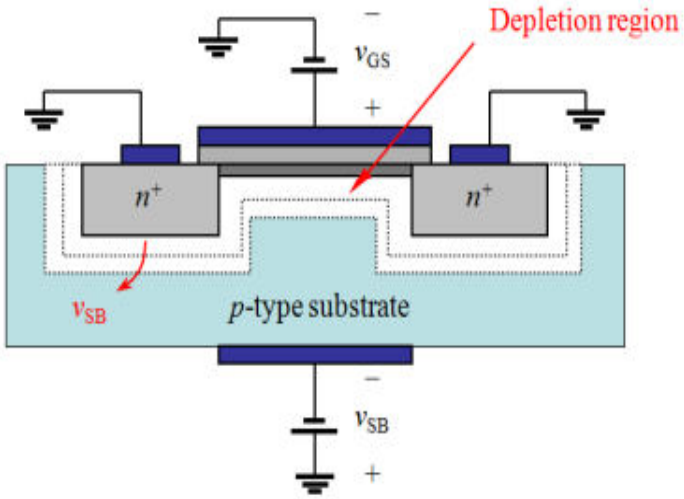
- V_A (**Early voltage**) $= 1/\lambda$ is proportional to channel length: $V_A = V'_A L$
- V'_A is process-technology dependent with a typical value from 5 ~ 50 V/μm.
- Due to the dependence of i_D on v_{DS}, MOSFET shows **finite output resistance** in saturation region.

The body effect

- The BS and BD junction should be reverse biased for the device to function properly.
- Normally, the body of a *n*-channel MOSFET is connected to the most negative voltage.
- The depletion region widens in BS and BD junctions and under the channel as V_{SB} increases.
- **Body effect**: V_t increases due to the excess charge in the depletion region under the channel.
- The body effect can cause considerable degradation in circuit performance.
- Threshold voltage:

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

$$\text{where } \gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \text{ and } \phi_f = \frac{kT}{q}\ln(\frac{N_A}{n_i})$$



- Current equations:

$$i_D = \mu_n C_{ox}\frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

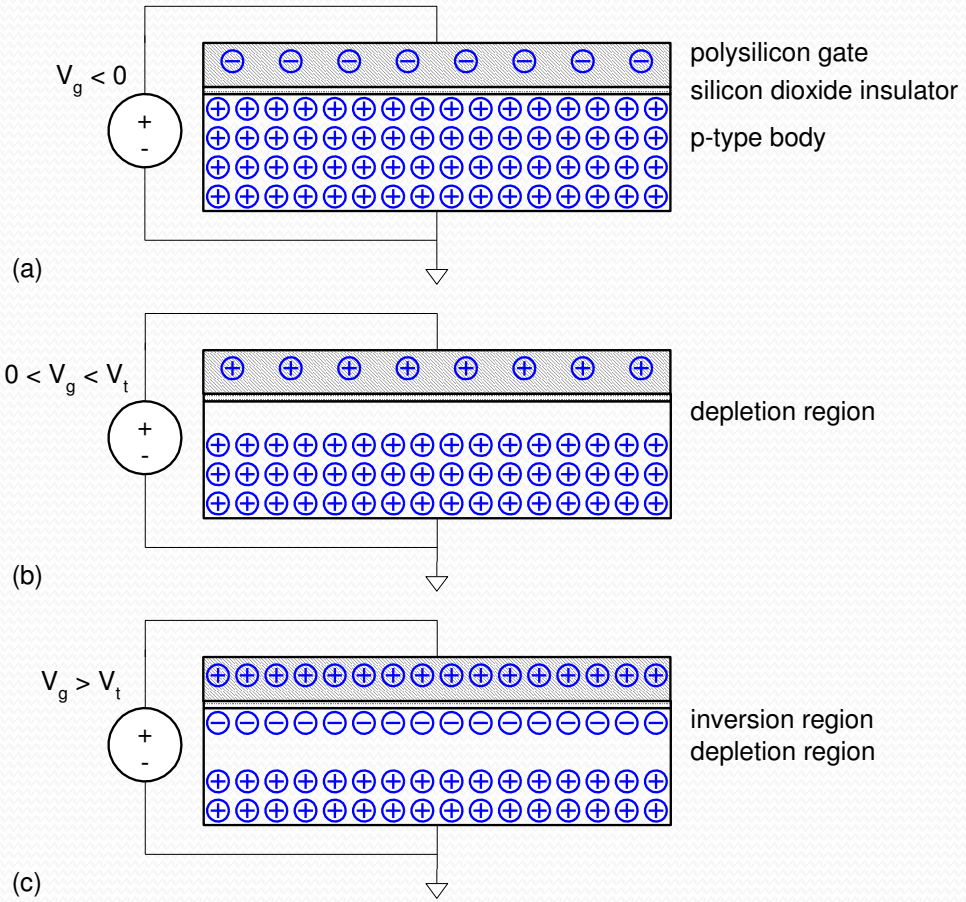
$$i_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2$$

Temperature effect

- V_t decreases by ~2mV for every 1°C rise → i_D increases with temperature.
- k'_n decreases with temperature → i_D decreases with increasing temperature.
- For a given bias voltage, the overall observed effect of a temperature increase is a decrease in i_D.

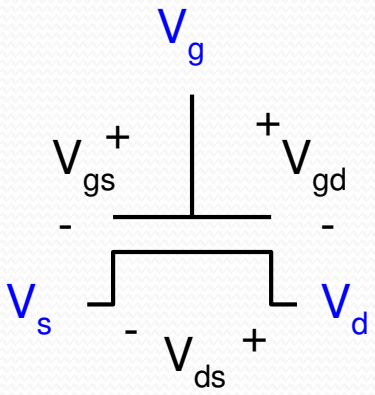
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



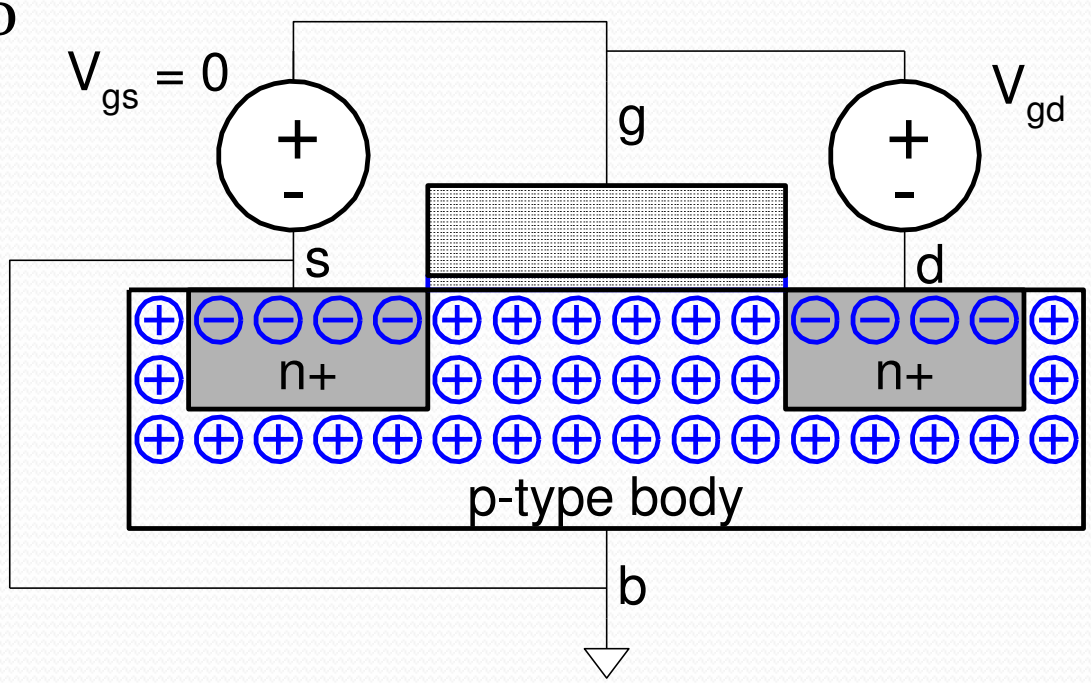
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- NMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



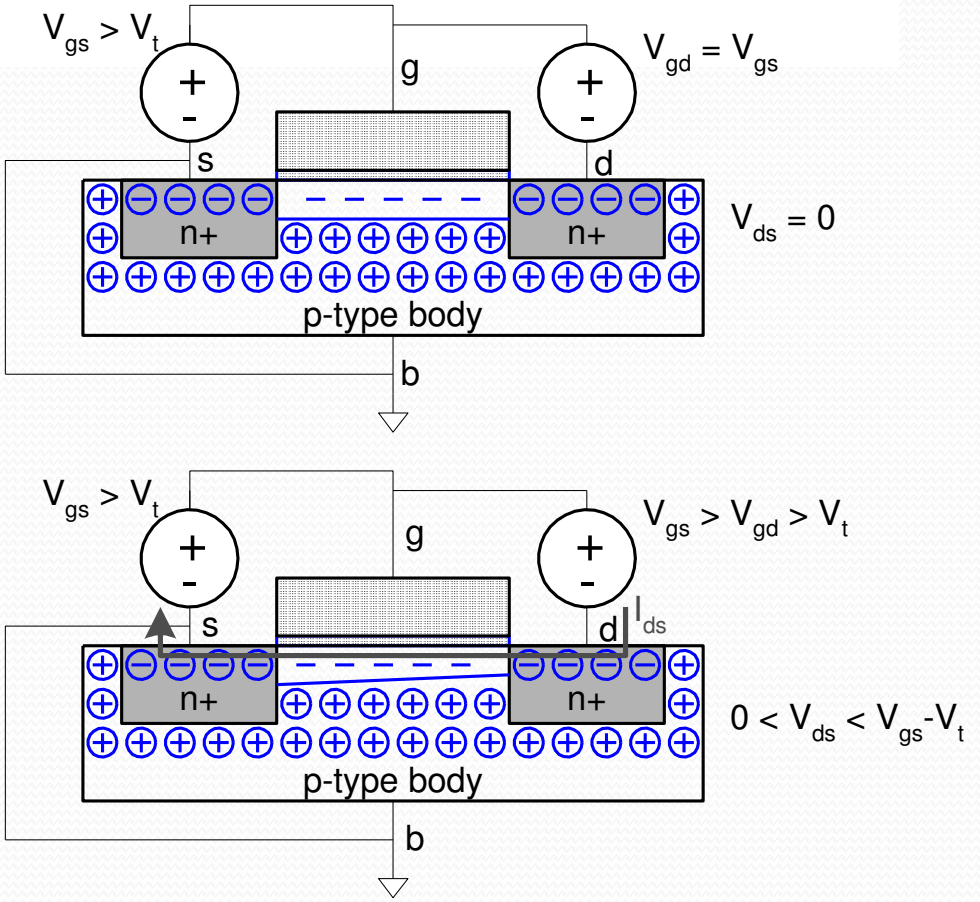
NMOS Cutoff

- No channel
- $I_{ds} = o$



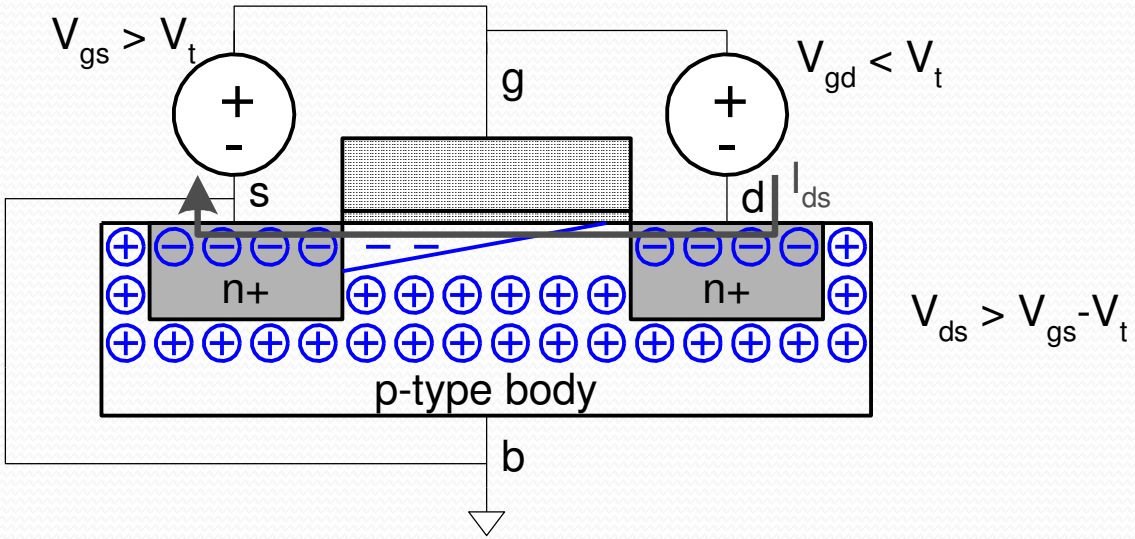
NMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



NMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source

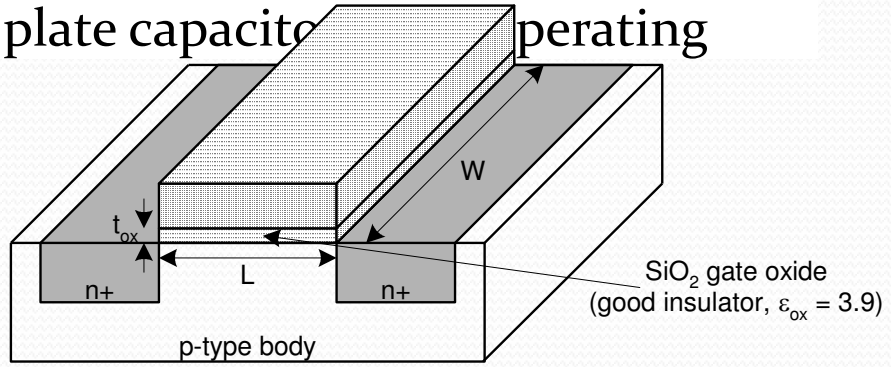


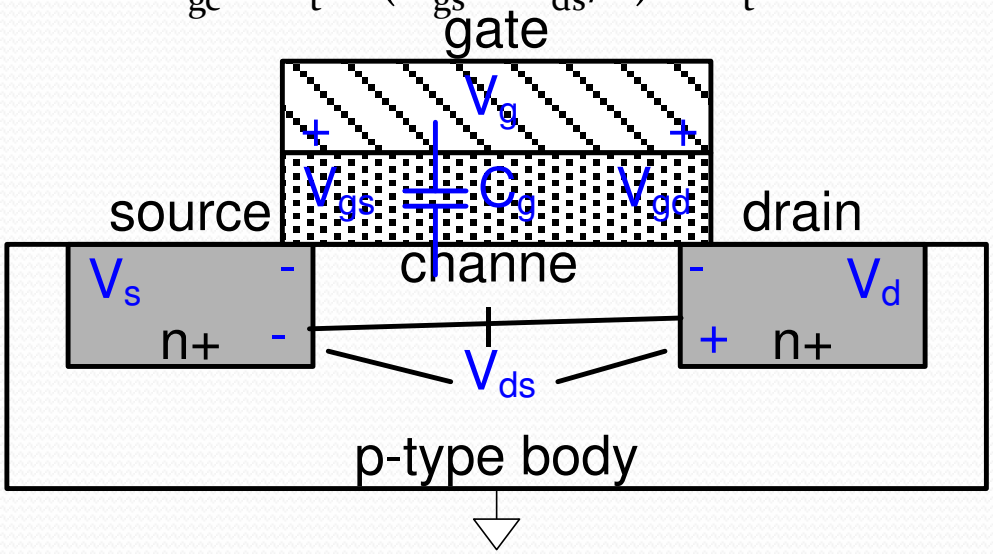
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





$C_{ox} = \varepsilon_{ox} / t_{ox}$

$V_{gc}=(V_{gs}+V_{gd})/2$
$=V_{gs}-V_{ds}/2$

Carrier velocity

- Charge is carried by e-
- Carrier velocity v proportional to lateral E-field between source and drain
- $v = \mu E$ (μ is called mobility)
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

NMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \qquad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

NMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

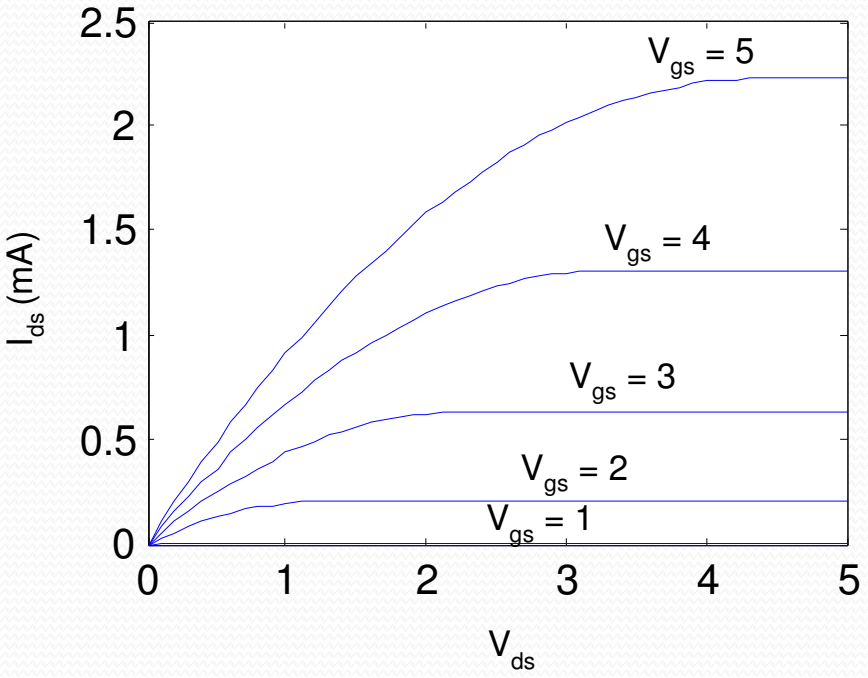
NMOS I-V Summary

- *Shockley* 1st order transistor models (long-channel)

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Example

- We consider a 0.6 μm process
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - μ = 350 cm²/V*s
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\,\mu A/V^2$$

PMOS I-V

- All dopings and voltages are inverted for PMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V*s$ in AMI 0.6 μm process
- Thus PMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$