Unit 2
MOS Inverters

MOS Inverter: Static Characteristics

- The inverter is the most fundamental logic gate that performs a Boolean operation on a single input variable.
- Many basic principles employed in the design and analysis of MOS inverters can be directly applied to more complex circuits such as NAND, NOR and XOR, XNOR gates.
- The inverter operation is such that, for very low input voltage levels the output voltage V_{out} is equal to a high value V_{OH} (output high voltage).

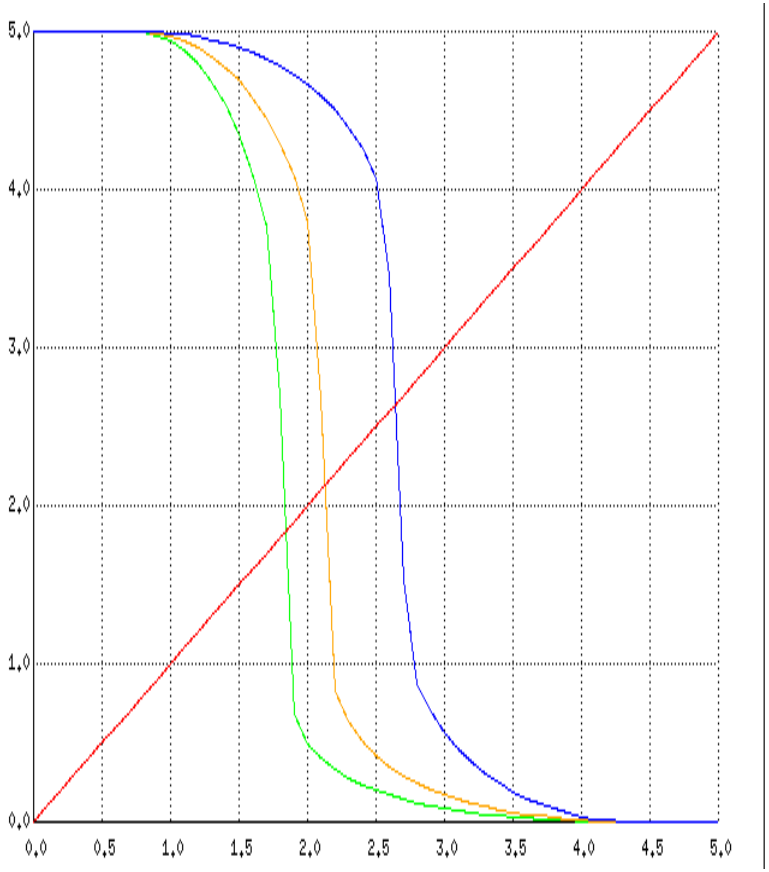
MOS INVERTER

- The smaller input voltage satisfying dVout/dVin=-1 is called the input low voltage VIL and the larger input voltage satisfying this condition is called the input high voltage VIH.
- Both these voltages play significant roles in determining the Noise Margins of inverter circuits.
- As the input voltage is further increased, the output voltage continues to drop and reaches a value of VOL (output low voltage) when the input voltage is equal to VOH.

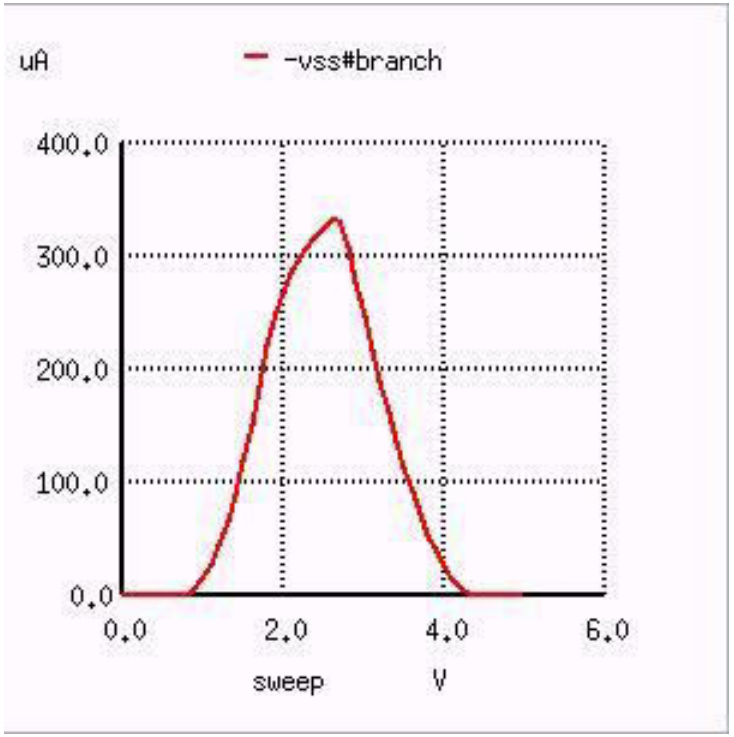
- We can now define the inverter threshold voltage as the point where Vin=Vout on the voltage transfer characteristic (VTC) curve.
- From this analysis of inverter operation we come up with five critical voltages, which characterize the behavior of the inverter circuit. These are VOL, VOH, VIL, VIH and Vth and are defined as follows:
- VOH: maximum output voltage; “1”.
- VOL: Minimum output voltage; “0”.
- VIL: Maximum input voltage which can be interpreted as a logic 0.
- VIH: Minimum input voltage which can be interpreted as a logic 1.

- In this case the nMOS device is in Cut-off and hence conducts no current.
- The pMOS is in linear region and acts as a resistor, the voltage drop across this resistor is very small in magnitude and the output voltage level is high.
- As Vin is increased the fall in the output voltage is not abrupt but gradual (refer to the inverter VTC curve) and has a finite slope.
- The two critical voltage points on the VTC are when the slope of the Vout(Vin) charateristic becomes –1.

MOS INVERTER VTC & I_{ds}



- I_{ds} Vs Time



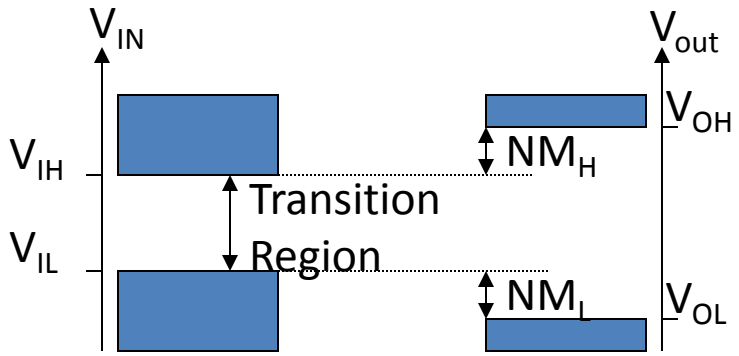
NOISE MARGIN

- Noise Margin is a parameter closely related to the input-output voltage characteristics.
- Noise Margin allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected.
- Noise Margin is usually defined in terms of Low Noise Margin (NML) and High Noise Margin (NMH).
- NML is the difference in magnitude between the maximum low output voltage of the driving gate and the maximum input low voltage recognized by the driven gate.

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$

- NMH is the difference in magnitude between the minimum high output voltage of the driving gate and the minimum input high voltage recognized by the receiving gate.
- The ideal operating point with regard to NOISE MARGIN is to have the minimum High input voltage (VIH) be equal to the maximum Low input voltage (VIL).

NOISE MARGINS HIGH & LOW DEFINITIONS



- Shaded areas represent valid regions of the input and output voltages.
- With $I_{dsn} = I_{dsp} = 0$, implying that n-type device is in saturation while p-device is in linear region we have that:

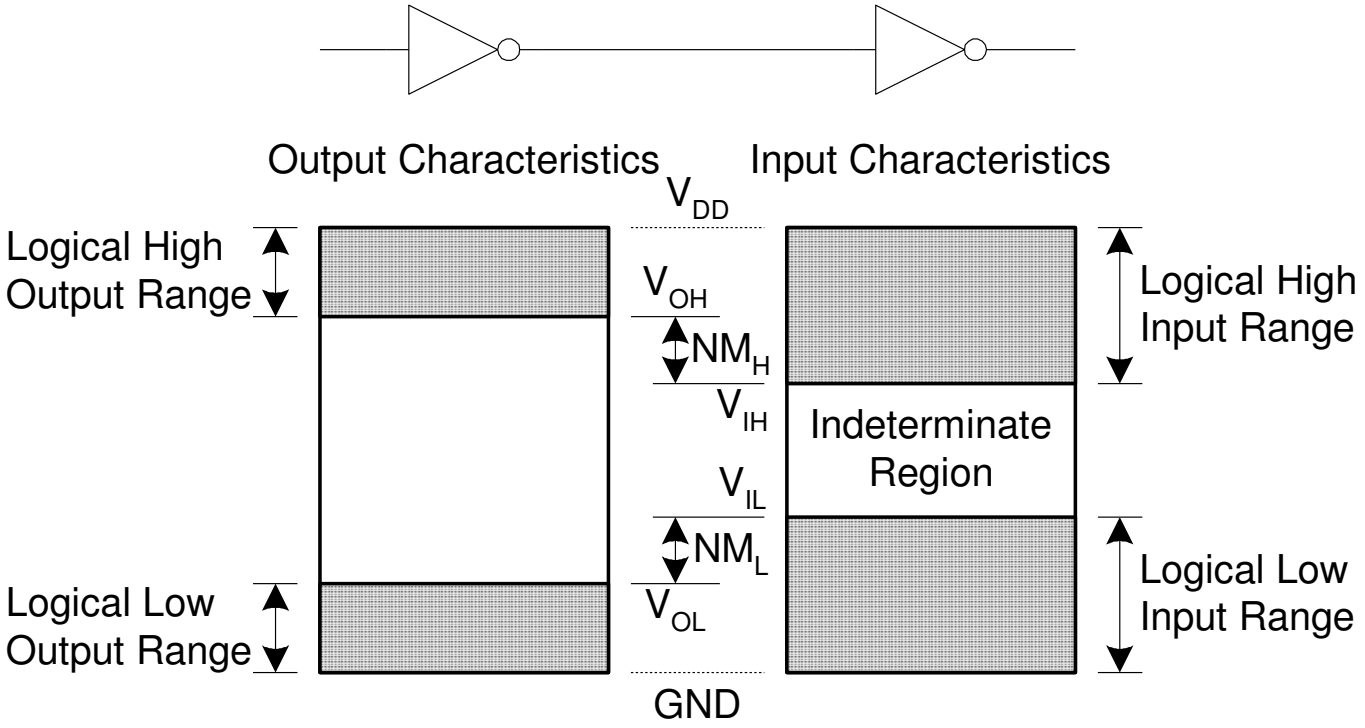
$$V_{out} = V_{OH} = V_{DD}$$

- If the pMOS transistor is turned off that is, the input voltage exceeds $V_{DD} + V_{tp}$, with the nMOS device operating in linear region, but with Idsn=Idsp=0 then we have that:

$$V_{out} = V_{OL} = 0$$

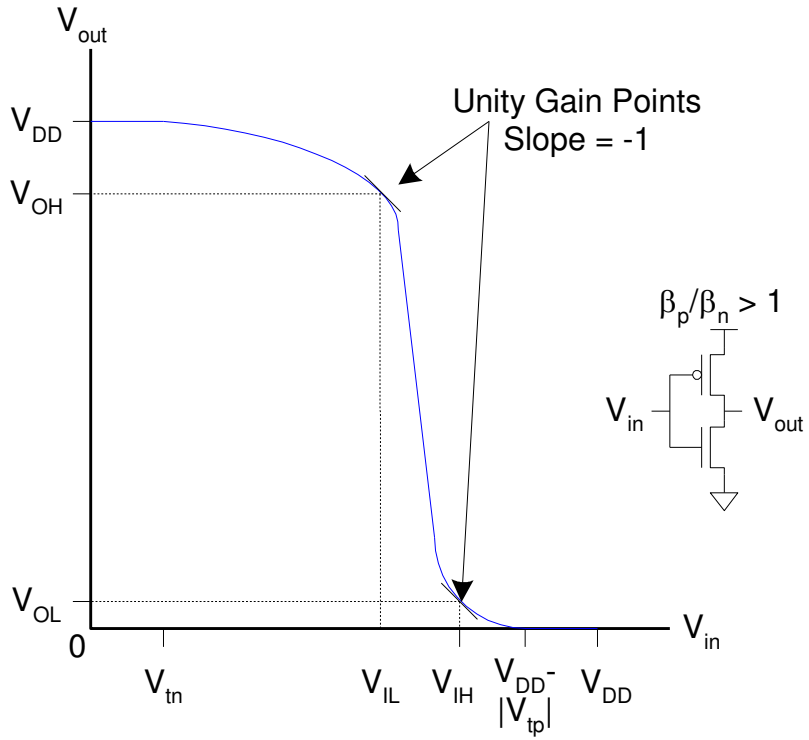
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



Transient Response

- *DC analysis* tells us V_{out} if V_{in} is constant
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to V_{DD} or vice versa

Inverter Step Response

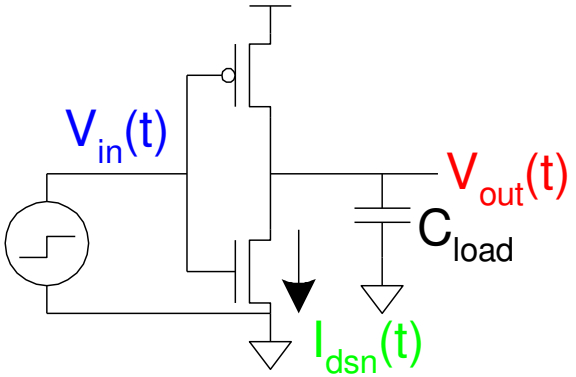
- Ex: find step response of inverter driving load cap

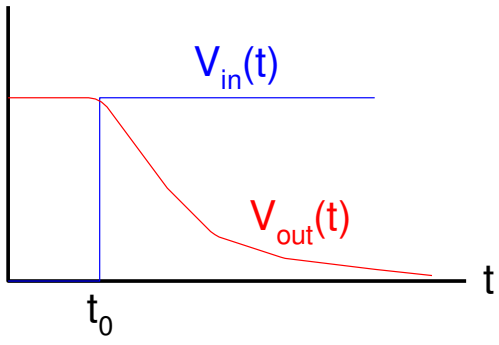
$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - V_{out}(t)/2\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$





Delay Definitions

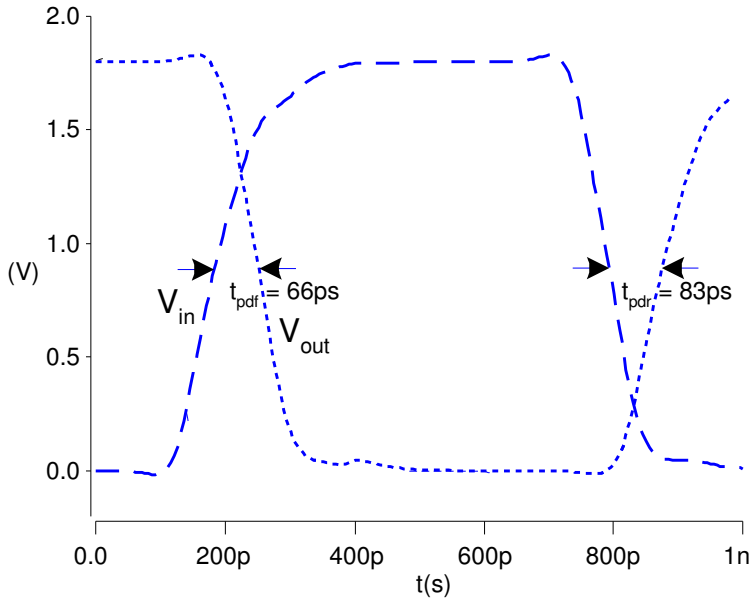
- $\mathbf{t_{pdr}}$: *rising propagation delay*
  - From input to rising output crossing $V_{DD}/2$
- $\mathbf{t_{pdf}}$: *falling propagation delay*
  - From input to falling output crossing $V_{DD}/2$
- $\mathbf{t_{pd}}$: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- $\mathbf{t_r}$: *rise time*
  - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- $\mathbf{t_f}$: *fall time*
  - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

Delay Definitions

- **t_{cdr}**: *rising contamination delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{cdf}**: *falling contamination delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{cd}**: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$

Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write

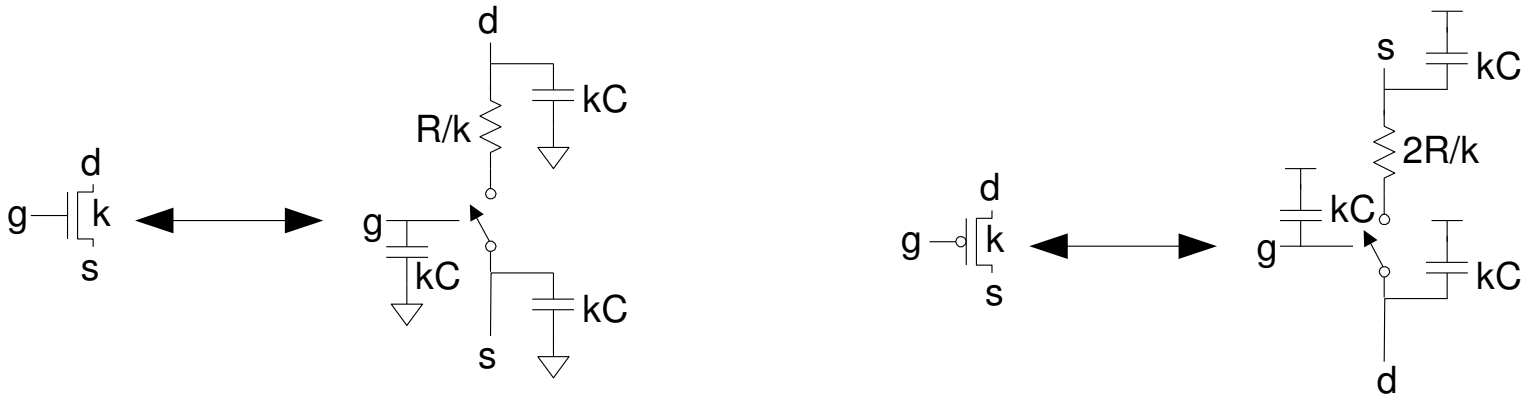


Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use *effective resistance* R
  - So that t_{pd} = RC
- Characterize transistors by finding their effective R
  - Depends on average current as gate switches

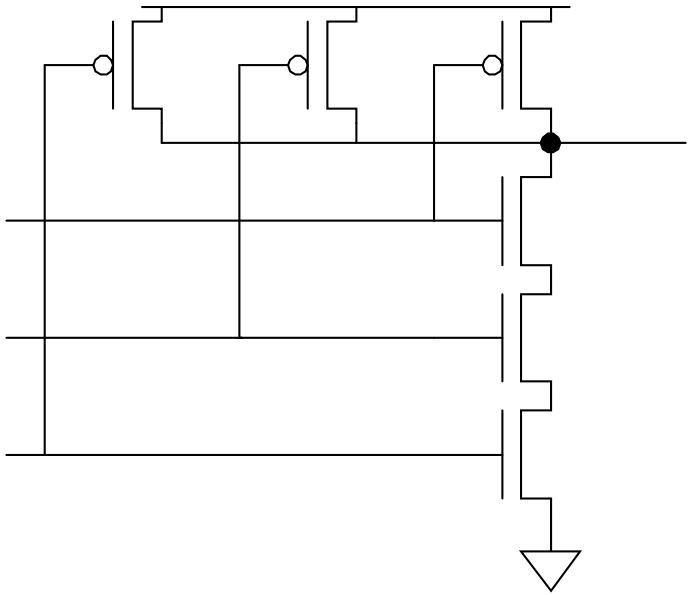
RC Delay Models

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



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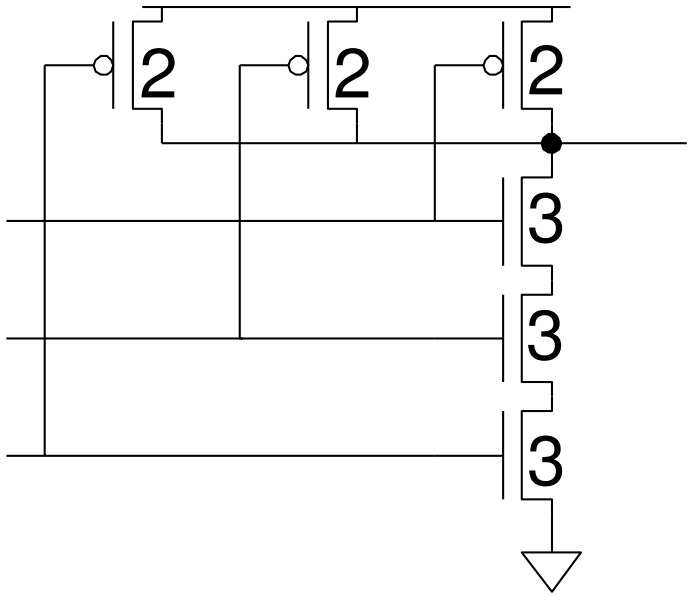
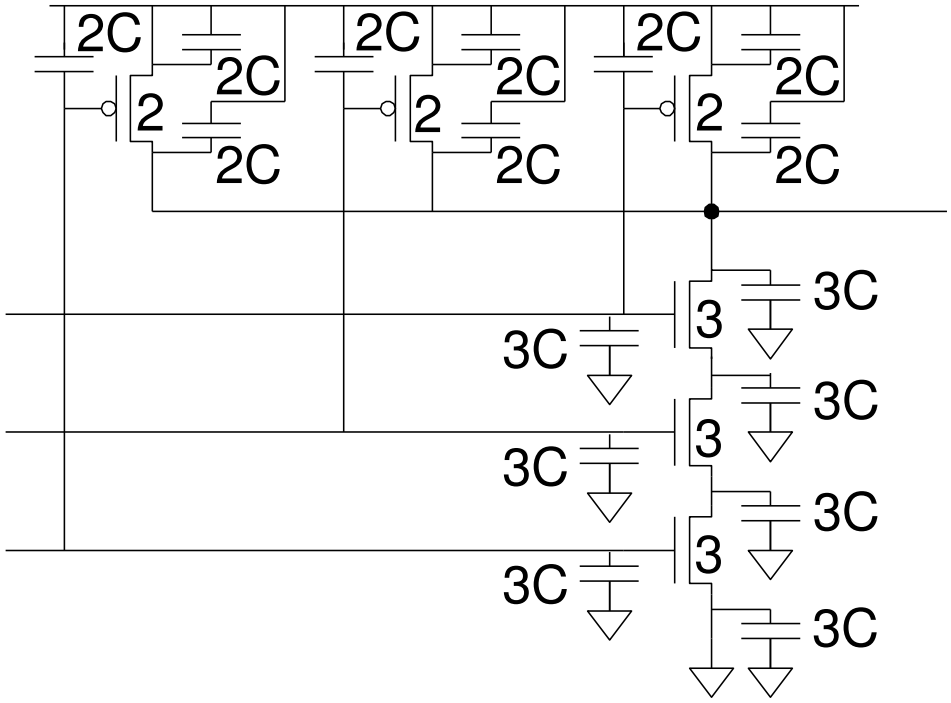


3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.



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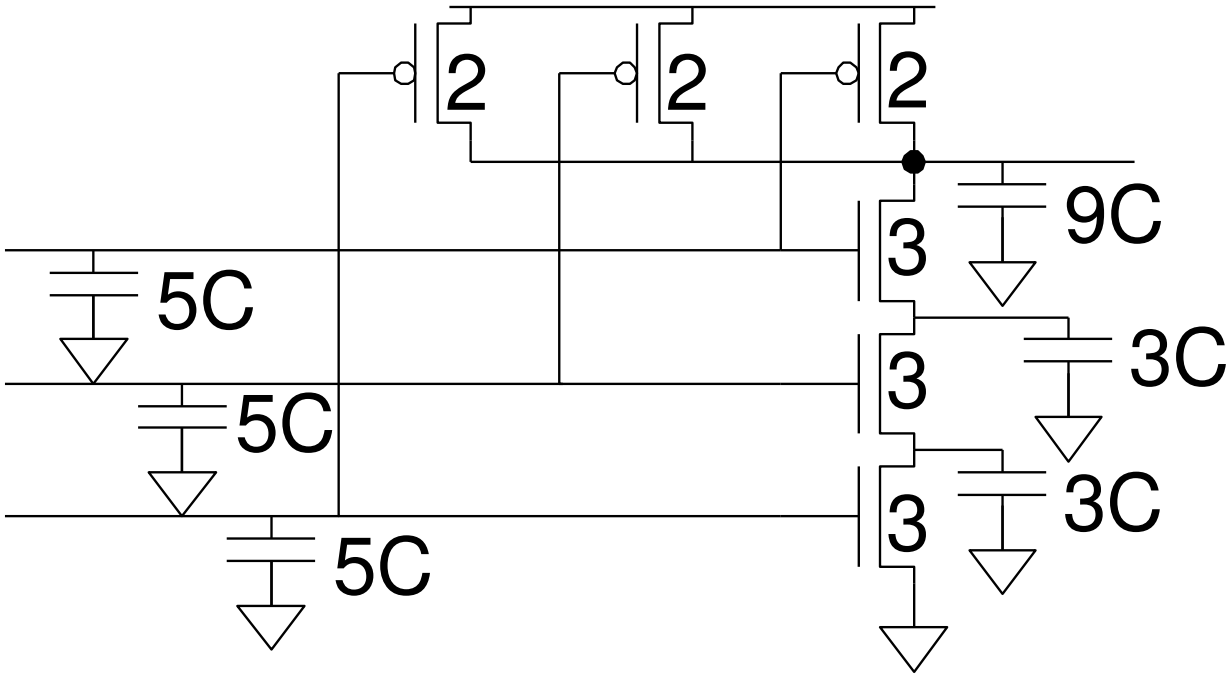
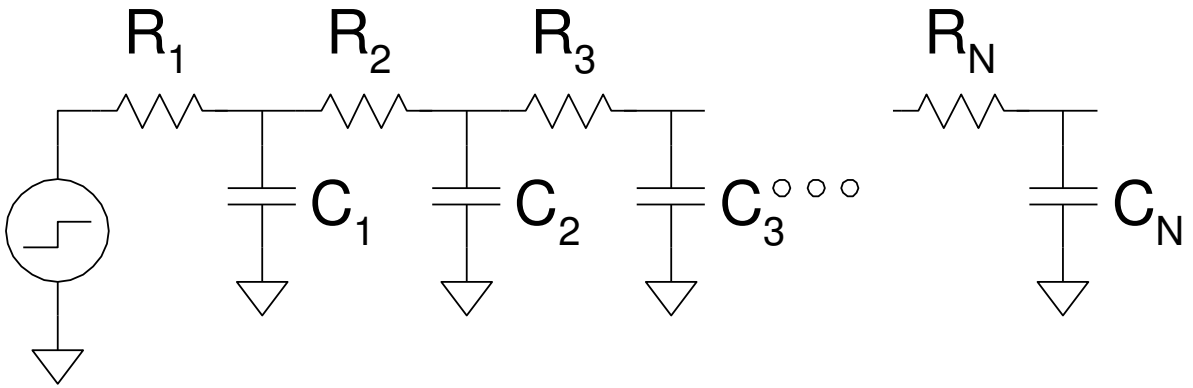


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

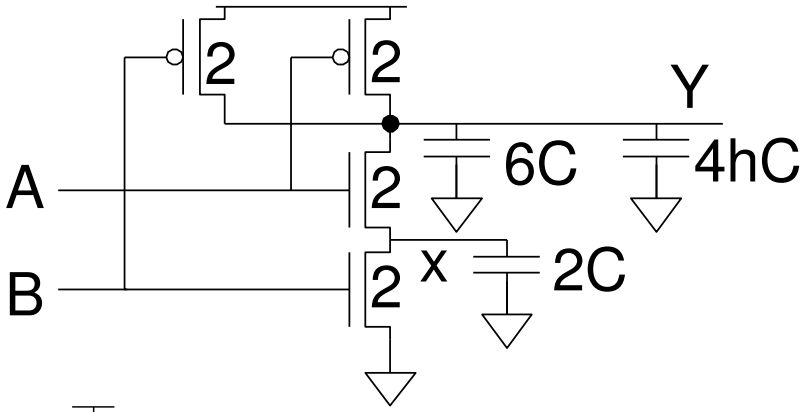
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

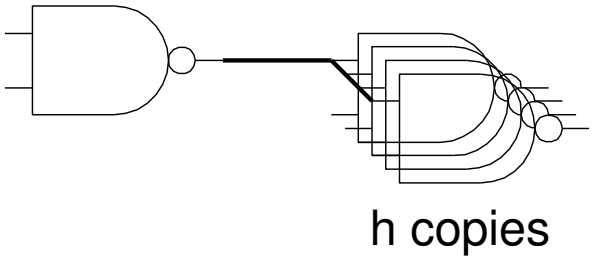
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$

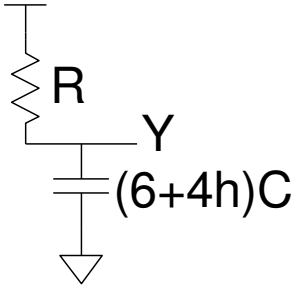


Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.







$$t_{pdr} = (6+4h)RC$$

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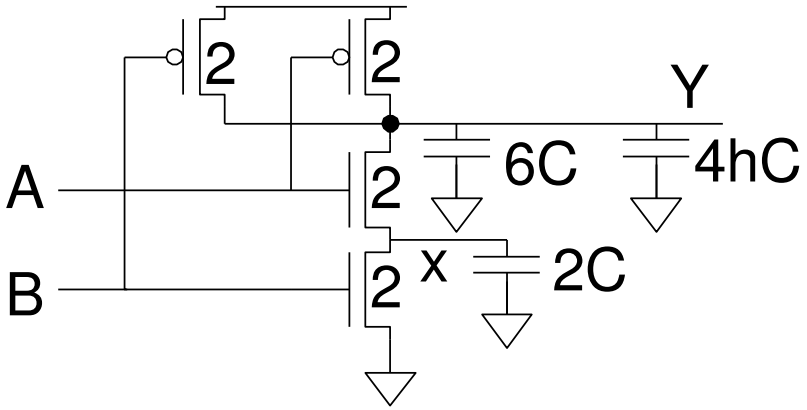

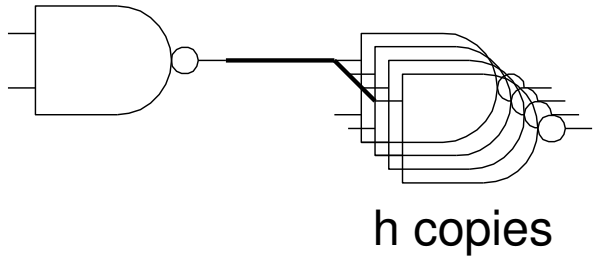

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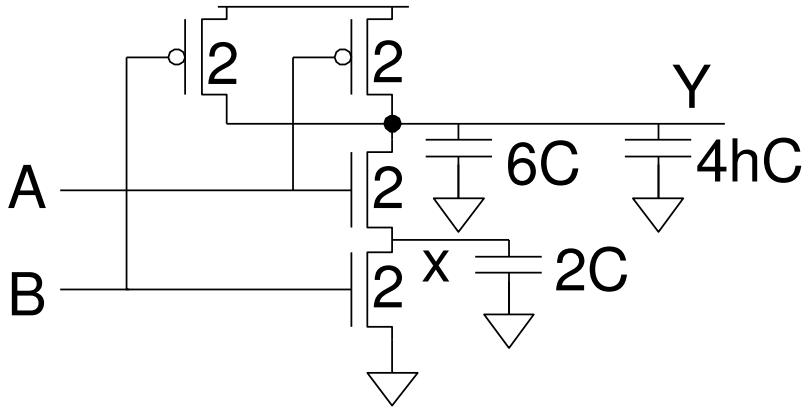
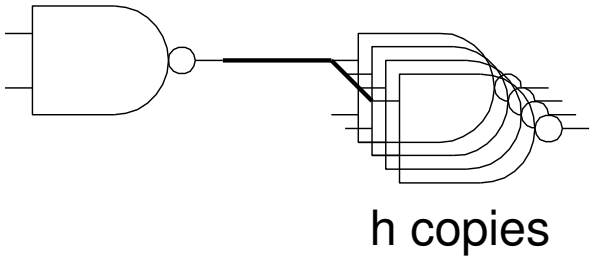
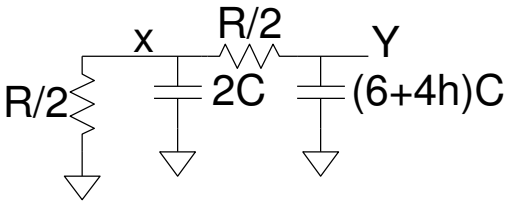






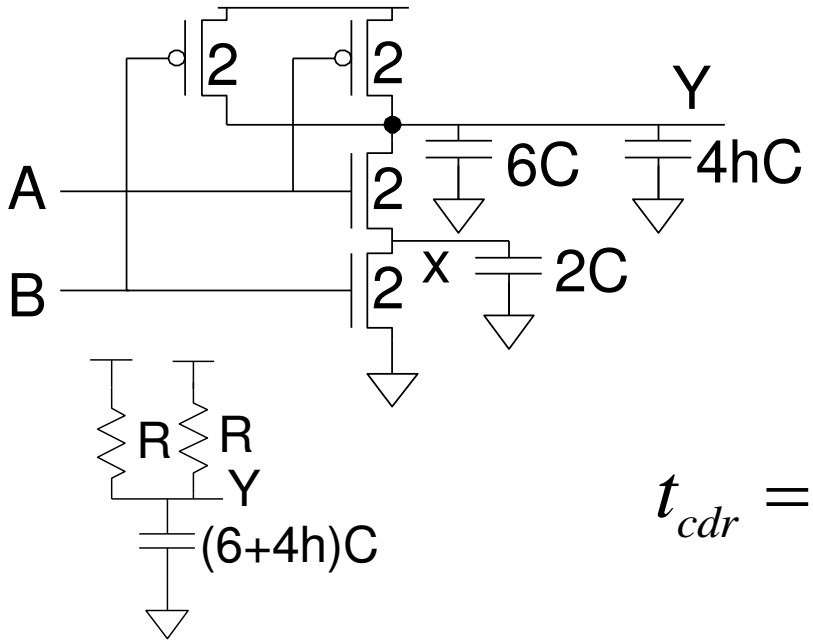
$$t_{pdf} = (2C)\left(\tfrac{R}{2}\right) + \left[(6+4h)C\right]\left(\tfrac{R}{2}+\tfrac{R}{2}\right)$$
$$= (7+4h)RC$$

Delay Components

- Delay has two parts
  - *Parasitic delay*
    - 6 or 7 RC
    - Independent of load
  - *Effort delay*
    - 4h RC
    - Proportional to load capacitance

Contamination Delay

- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If both inputs fall simultaneously



$$t_{cdr} = (3+2h)RC$$

Diffusion Capacitance

- we assumed contacted diffusion on every s / d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too