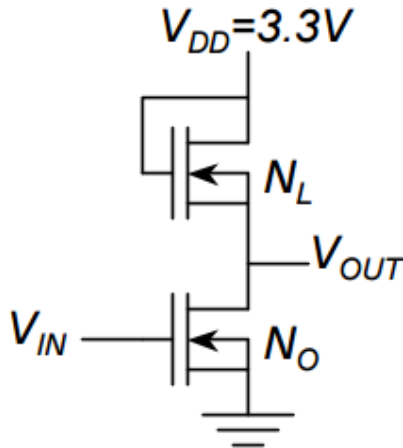# Unit 2
# MOS Inverters

NMOS Inverter w/ Saturated Enhancement Load

- A MOSFET replaces the resistive load, greatly improving the packing density.

- The two MOSFET's are fabricated with identical thresholds and process transconductance parameters, for simplicity and high circuit yield.

- The load has a positive threshold and has $V_{GS}=V_{DS}$; therefore it is always saturated.

- $V_{OH} = V_{DD} - V_T$.

NMOS Inverter w/ Depletion Type Load

- For the depletion type device,

$$V_{GSL} = 0$$

This necessitates $V_{TL} \leq 0$ for conduction in the load. Also, linear or saturated operation of the load is possible:
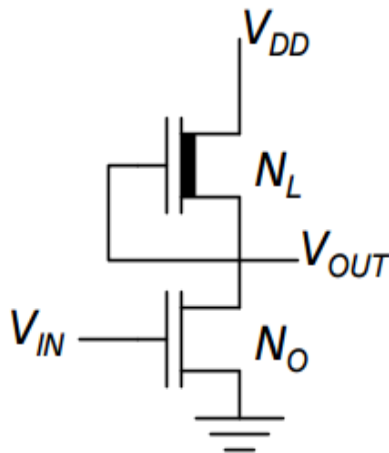
$$V_{DD} - V_{OUT} > -V_{TL} \Rightarrow \text{saturation}$$
$$V_{DD} - V_{OUT} < -V_{TL} \Rightarrow \text{linear operation}$$

- This circuit achieves $V_{OH} = V_{DD}$ without the need for two supply voltages.

- The disadvantage is fabrication complexity, because transistors with two different threshold voltages are required.

n-Channel MOSFET connected as saturated load device

- An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter.

- Since the gate and drain of the transistor are connected, we have

$$V_{GS} = V_{DS}$$

When $V_{GS} = V_{DS} > V_{TN}$, *a non zero drain current is induced in the transistor and thus the transistor operates in saturation only. And following condition is satisfied.*

$$V_{DS} > (V_{GS} - V_{TN})$$

$V_{DS}(sat) = (V_{DS} - V_{TN})$ because $V_{GS} = V_{DS}$ or $V_{DS}(sat) = (V_{GS} - V_{TN})$

In the saturation region the drain current is
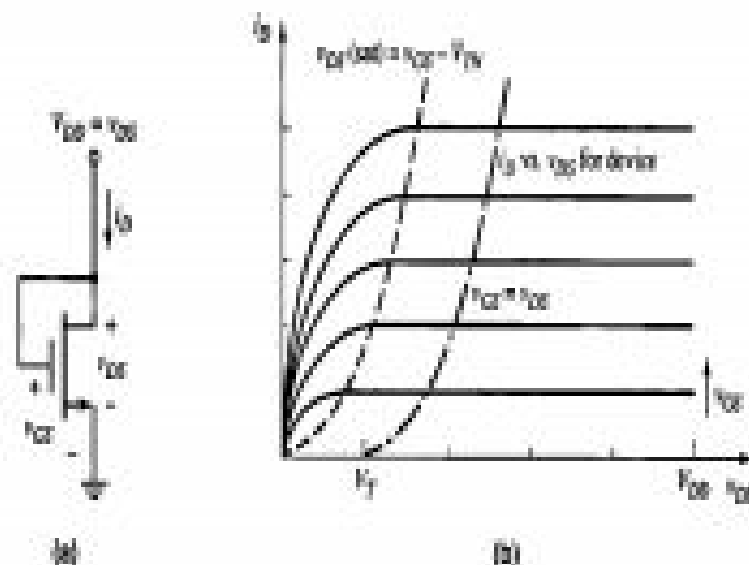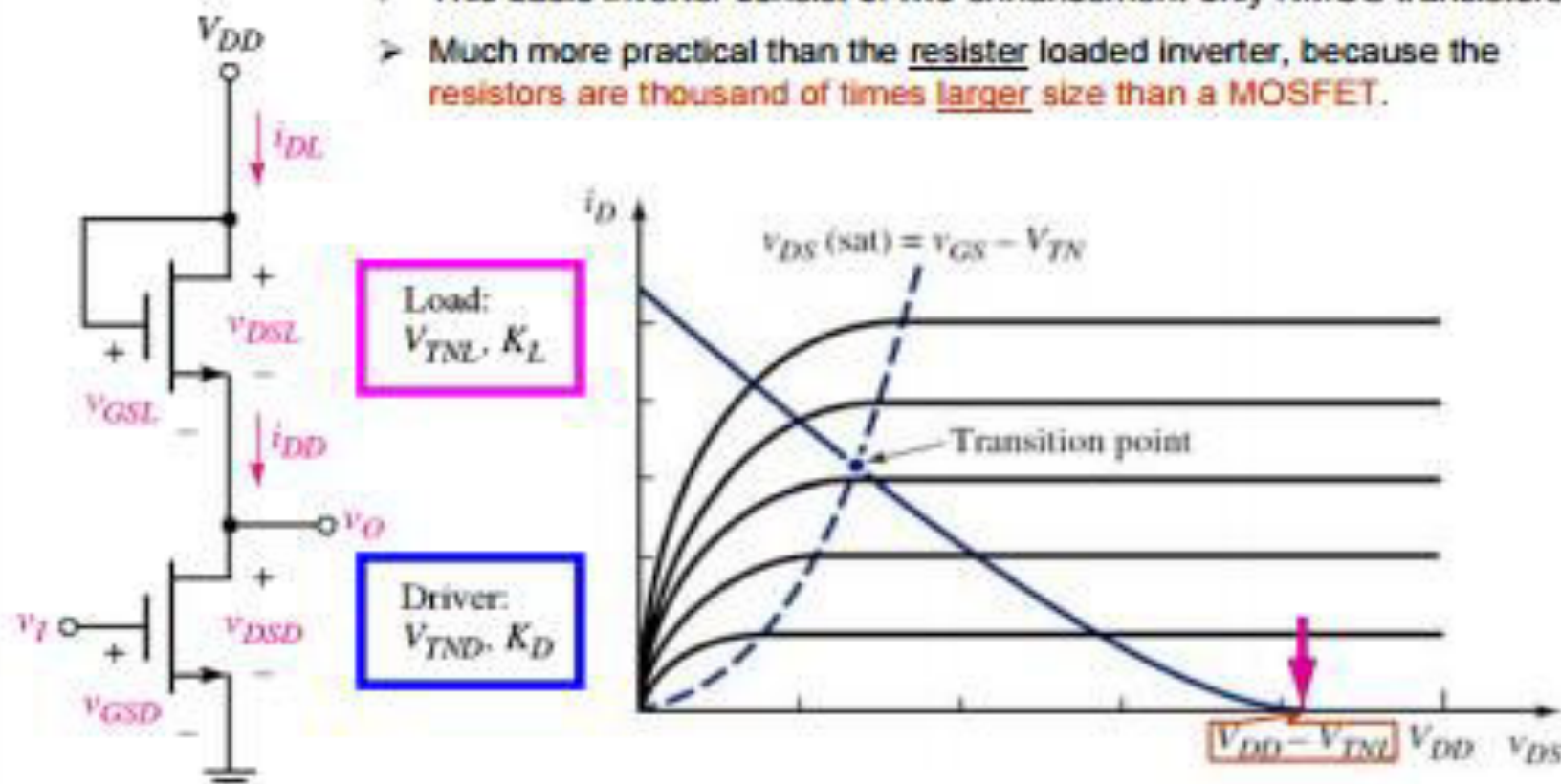$$i_D = K_n (V_{GS} - V_{TN})^2 = K_n (V_{DS} - V_{TN})^2$$

Figure 16.7 (a) n-channel MOSFET connected as saturated load device and (b) current-voltage characteristics of saturated load device

The i_D versus v_{DS} characteristics are shown in Figure 16.7(b), which indicates that this device acts as a nonlinear resistor.

NMOS Inverter with Enhancement Load

> ➤ This basic inverter consist of two enhancement-only NMOS transistors
> ➤ Much more practical than the resister loaded inverter, because the resistors are thousand of times larger size than a MOSFET.

Load:
V_{TNL}, K_L

Driver:
V_{TND}, K_D

v_{DS} (sat) $= v_{GS} - V_{TN}$

Transition point

$V_{DD} - V_{TNL}$ V_{DD} v_{DS}

NMOS Inverter with Enhancement Load

> An n-channel **enhancement-mode MOSFET** with gate connected to the drain can be used as a **load device**.

n-channel MOSFET connected as saturated load device

Device acts as a Nonlinear resistor !!!

i_D vs. v_{DS} for device
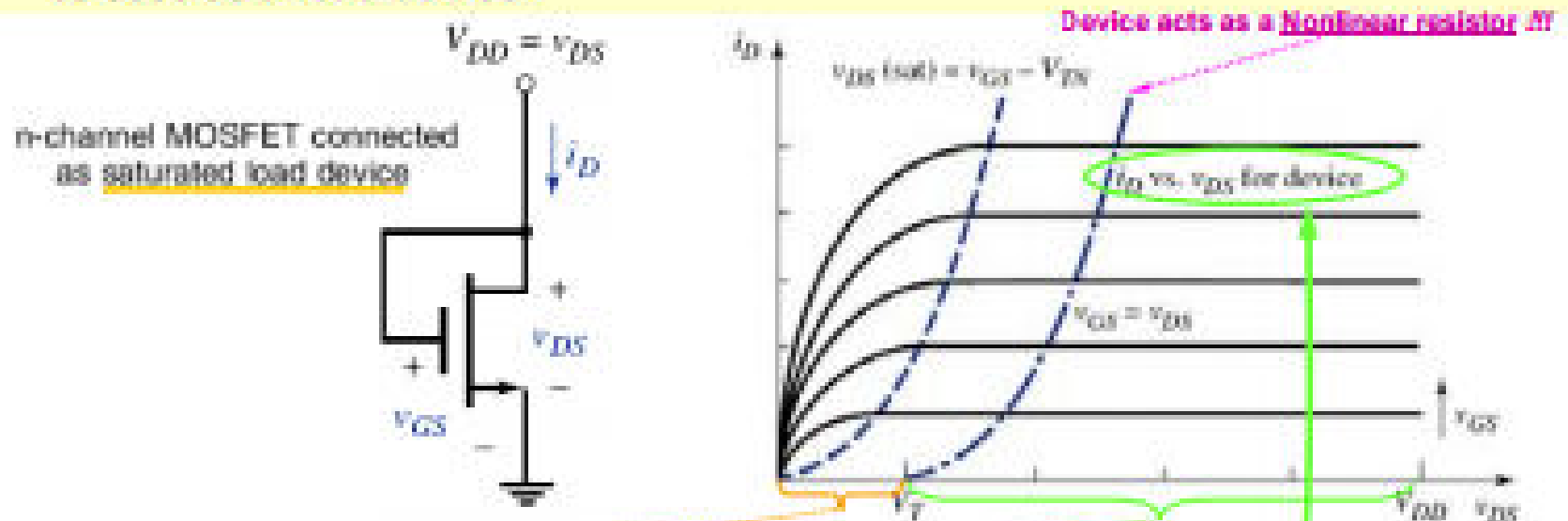
For $v_{GS} = v_{DS} \leq V_{TN}$, the drain current is zero.

$v_{GS} = v_{DS} > V_{TN}$, a nonzero drain current is induced in the device.

$$v_{DS} > (v_{GS} - V_{TN}) = (v_{DS} - V_{TN}) = v_{DS}(\text{sat})$$

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$$

Nonlinear resistor !!!

A transistor with this connection always operates in the **saturation** region when not in cutoff.

NMOS Inverter with Enhancement Load

When $v_I < V_{TND}$ driver is cut off and the drain currents are zero.

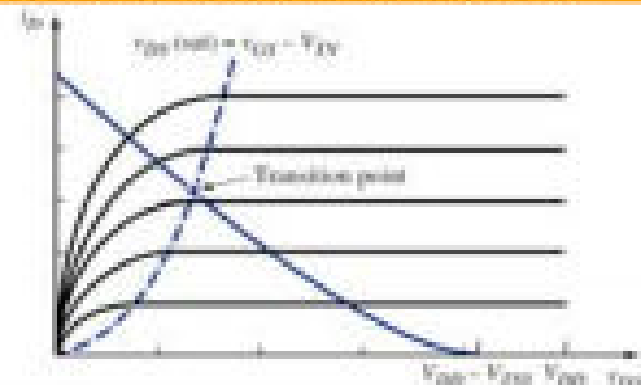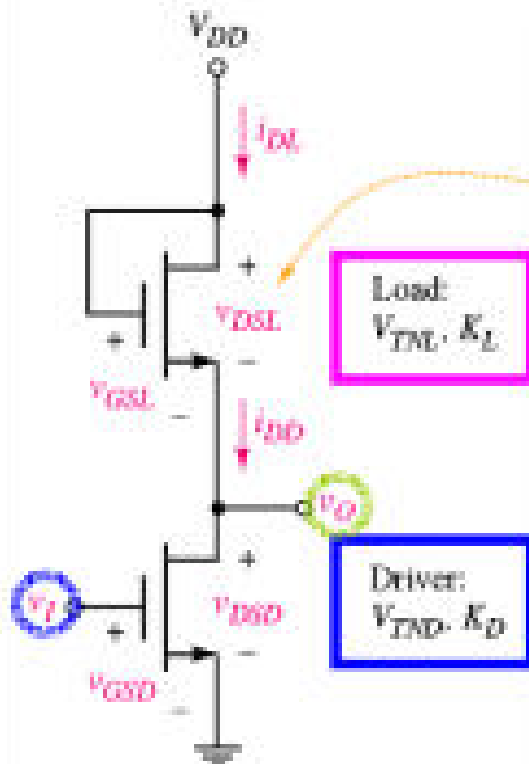$$i_{DL} = 0 = K_L(v_{DSL} - V_{TNL})^2$$

$$v_{DSL} = V_{DD} - v_O$$

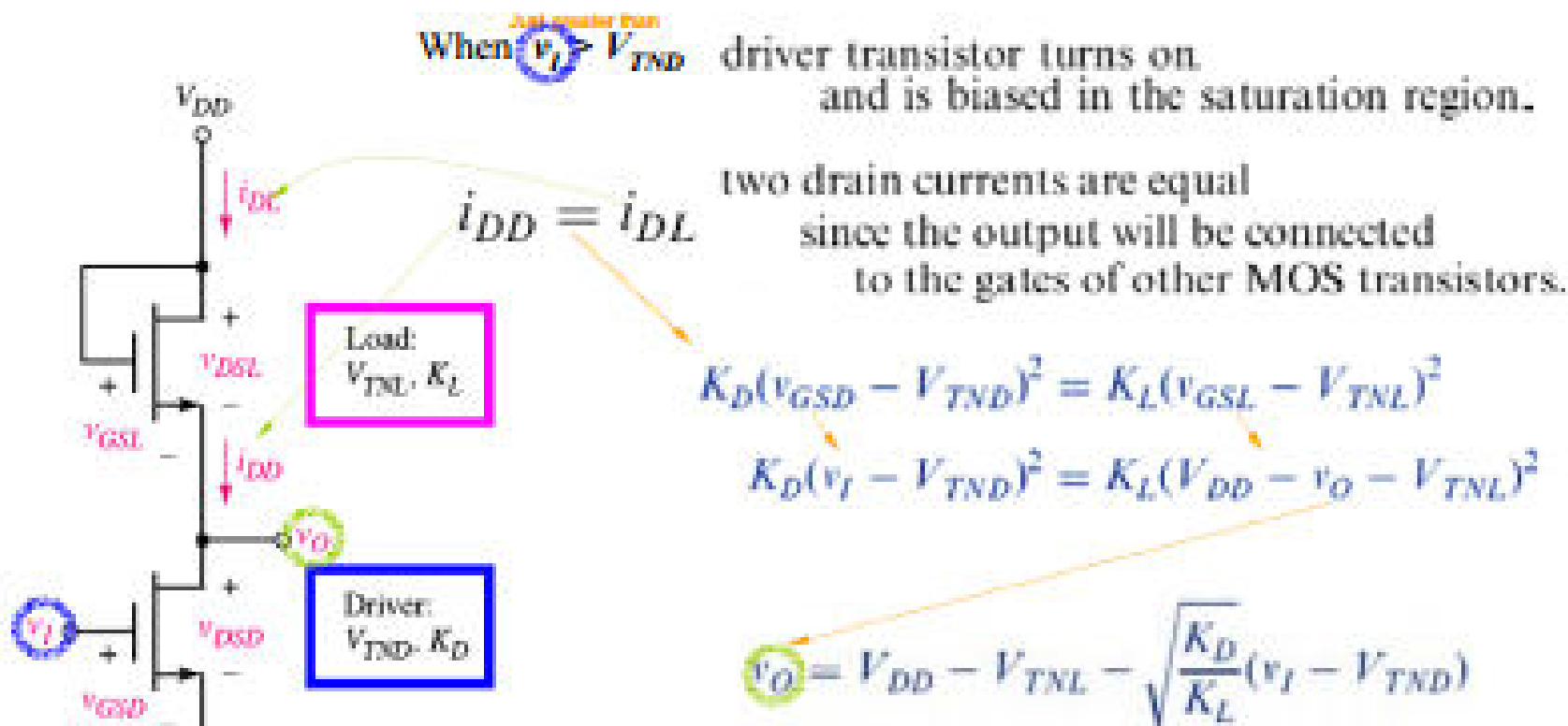$$\longrightarrow v_{DSL} - V_{TNL} = V_{DD} - v_O - V_{TNL} = 0$$

maximum output voltage

$$v_{O,max} \equiv V_{OH} = V_{DD} - V_{TNL}$$

For the enhancement-load NMOS inverter, the maximum output voltage, which is the logic 1 level, does not reach the full V_{DD} value.

NMOS Inverter with Enhancement Load

When $v_I > V_{TND}$ *Just master fun* driver transistor turns on
and is biased in the saturation region.

$$i_{DD} = i_{DL}$$

two drain currents are equal
since the output will be connected
to the gates of other MOS transistors.

Load: V_{TNL}, K_L

Driver: V_{TND}, K_D

$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$K_D(v_I - V_{TND})^2 = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

As the input voltage increases, the driver
Q-point moves up the load curve
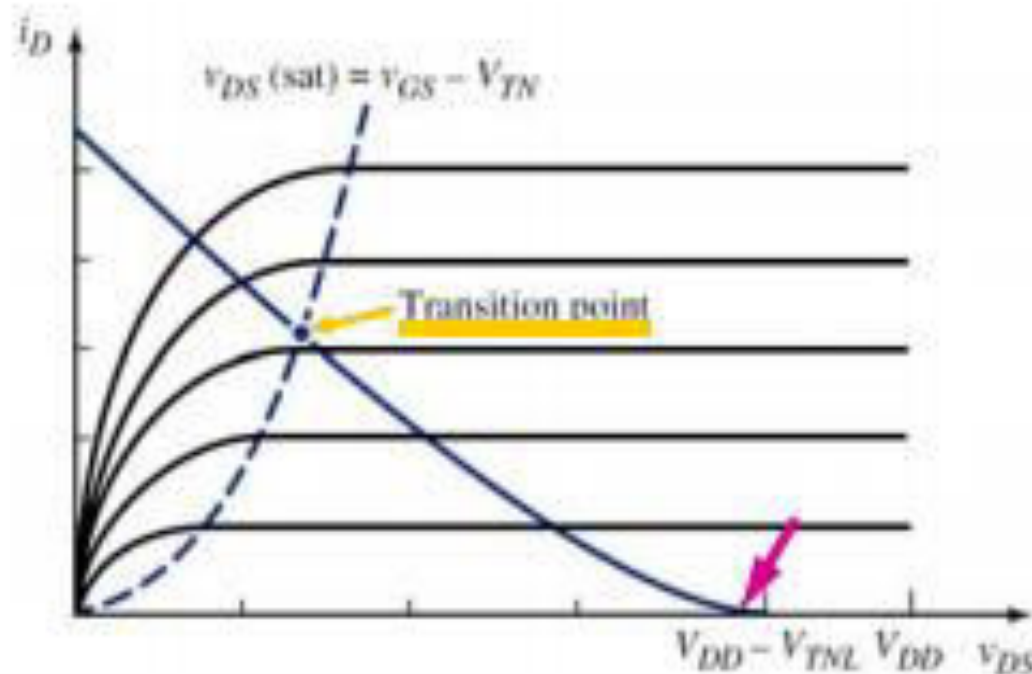and the output voltage decreases linearly with v_I.

NMOS Inverter with Enhancement Load

At the driver transition point,

$$v_{DSD}(\text{sat}) = v_{GSD} - V_{TND} \quad \text{or} \quad V_{Ot} = V_{It} - V_{TND}$$

$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}\left(1 + \sqrt{\dfrac{K_D}{K_L}}\right)}{1 + \sqrt{\dfrac{K_D}{K_L}}}$$

$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

Transition point

$V_{DD} - V_{TNL} \quad V_{DD} \quad v_{DS}$
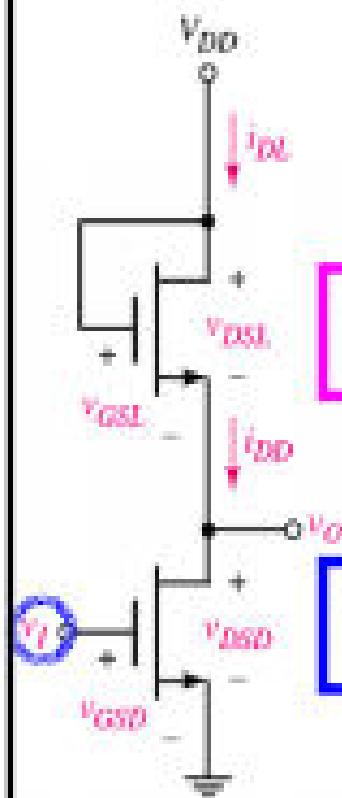
NMOS Inverter with Enhancement Load

When $v_I > V_{It}$ the driver transistor Q-point continues to move up the load curve and the driver becomes biased in the nonsaturation region.

Since $i_{DD} = i_{DL}$,

$$K_D\left[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2\right] = K_L(v_{DSL} - V_{TNL})^2$$

$$K_D\left[2(v_I - V_{TND})v_O - v_O^2\right] = K_L(V_{DD} - v_O - V_{TNL})^2$$

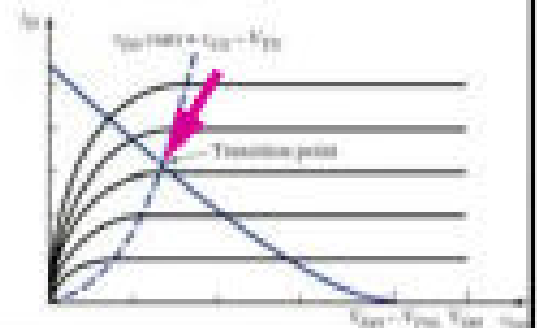the relationship between v_I and v_O in this region is not linear.
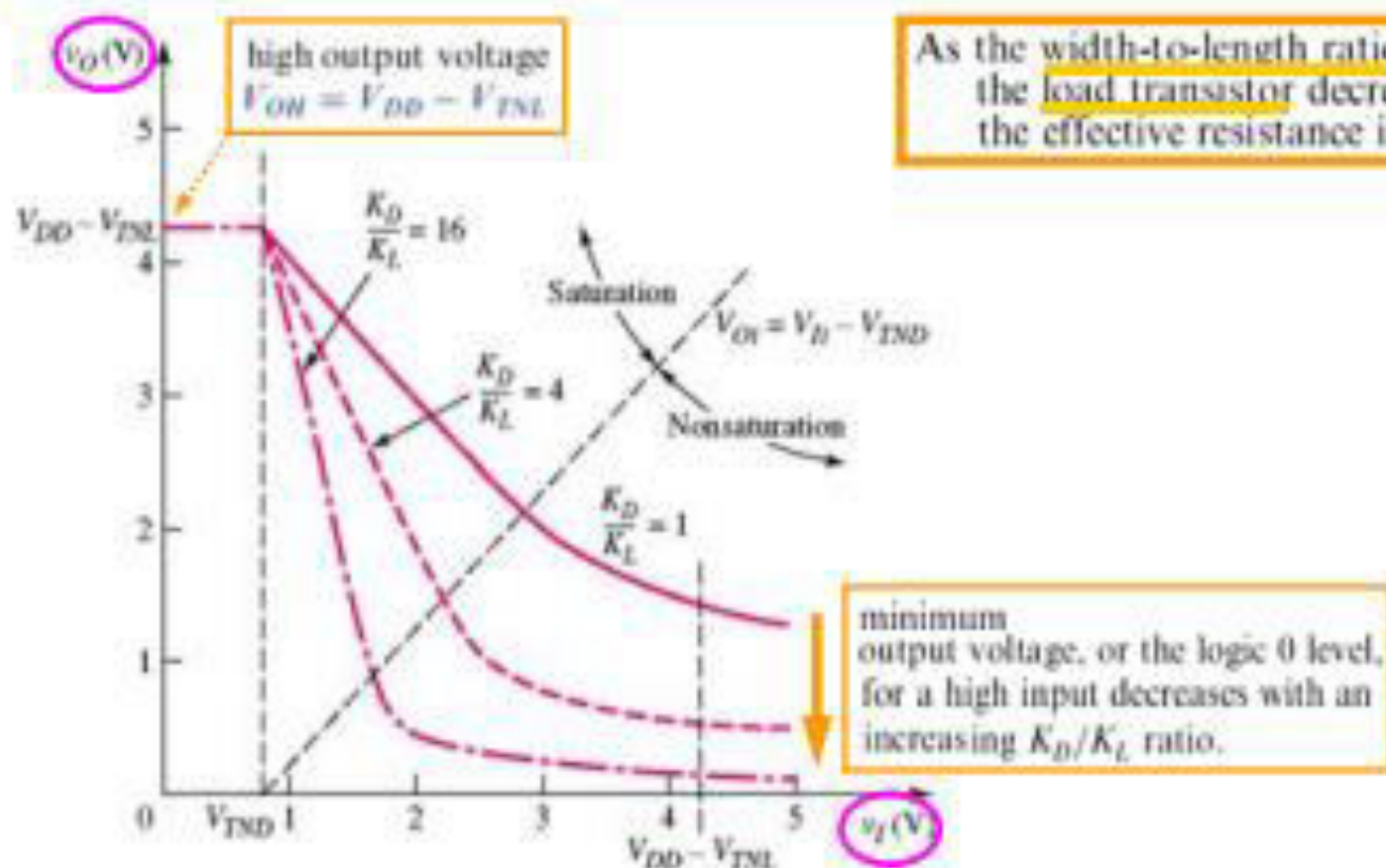
Load: V_{TNL}, K_L

Driver: V_{TND}, K_D

$$K_D/K_L$$

aspect ratio
width-to-length parameters
of the driver and load transistors.

NMOS Inverter with Enhancement Load

Voltage transfer characteristics, NMOS inverter with saturated load, for three aspect ratios

high output voltage $V_{OH} = V_{DD} - V_{TNL}$

As the width-to-length ratio of the load transistor decreases, the effective resistance increases.

minimum output voltage, or the logic 0 level, for a high input decreases with an increasing K_D/K_L ratio.

$\frac{K_D}{K_L} = 16$

$\frac{K_D}{K_L} = 4$

$\frac{K_D}{K_L} = 1$

Saturation

Nonsaturation

$V_{OH} = V_D - V_{TND}$

N-Channel Depletion-Mode MOSFET

- In n- channel depletion mode MOSFET, an n-channel region or inversion layer exists under the gate oxide layer even at zero gate voltage and hence term *depletion mode*.
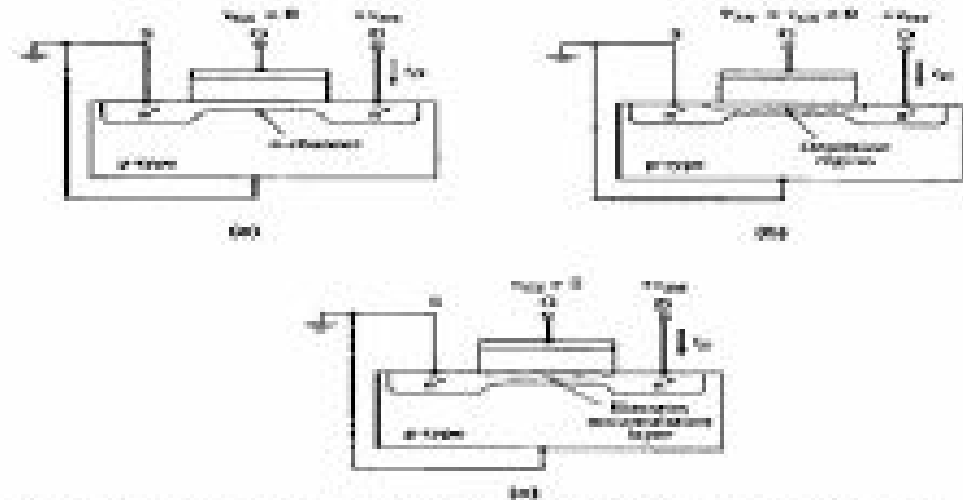
- A negative voltage must be applied to the gate to turn the *device off*.

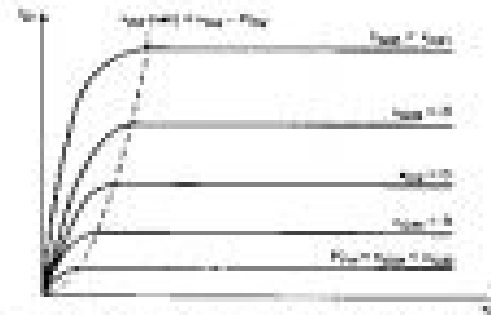- The *threshold voltage* is always *negative* for this kind of device.

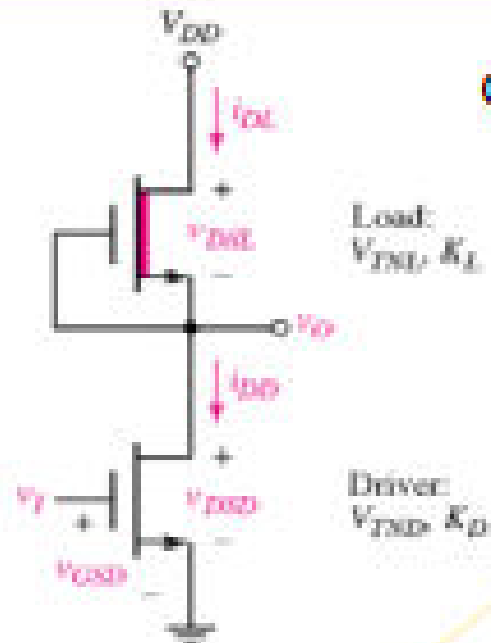Figure 5-13 Cross section of an n-channel depletion-mode MOSFET for (a) Vgs = 0, (b) Vgs > 0, and (c) Vgs < 0

Figure 5-14 Family of iD versus vDS curves for an n-channel depletion mode MOSFET

using a different circuit symbol for the depletion-mode device compared to the enhancement-mode device is simply for clarity in a circuit diagram.
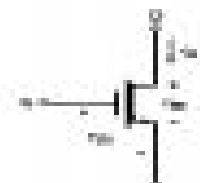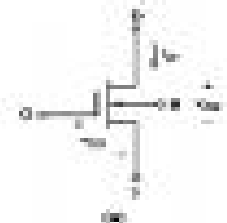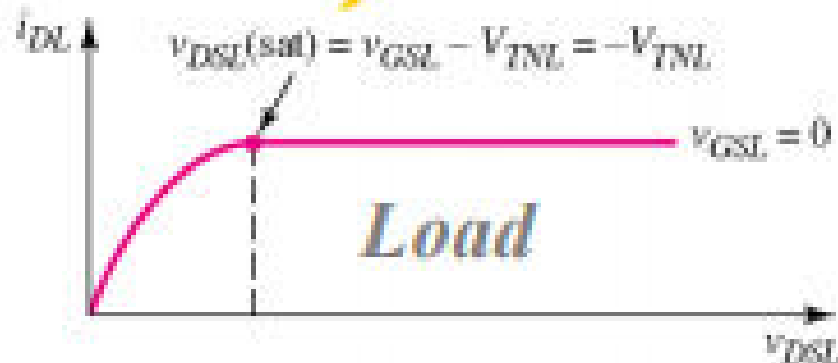
NMOS Inverter with Depletion Load

Gate and source are connected, $V_{GSL} = 0$

Load: V_{TNL}, K_L

Since the **threshold voltage** of load transistor is **negative**.

$$v_{DSL}(\text{sat}) = v_{GSL} - V_{TNL} = -V_{TNL}$$
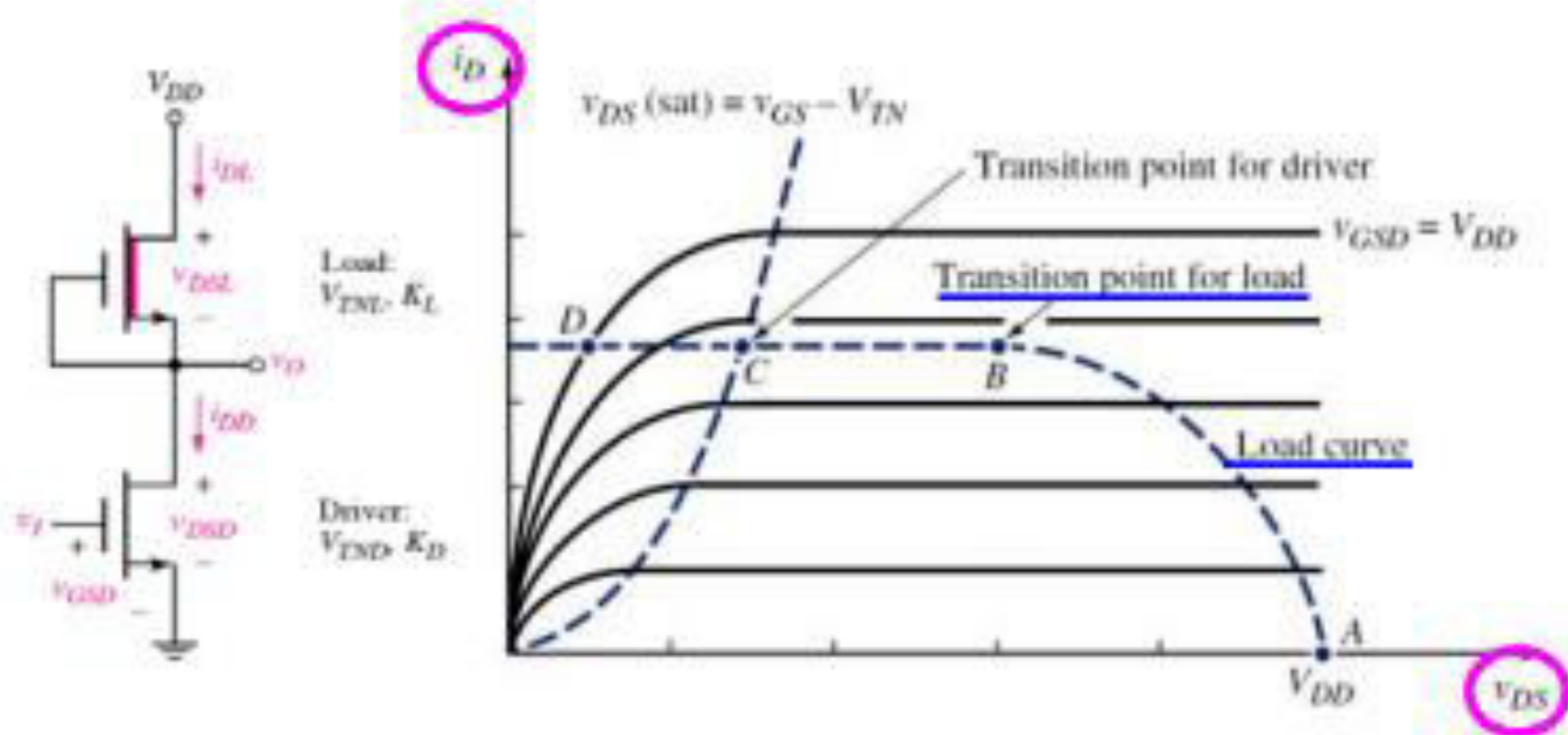$$v_{GSL} = 0$$

Driver: V_{TND}, K_D

$$v_{DSL}(\text{sat}) = v_{GSL} - V_{TNL} = -V_{TNL}$$

$v_{GSL} = 0$

Load

NMOS Inverter with Depletion Load

driver transistor characteristics and load curve

NMOS Inverter with Depletion Load (cont.)

Case 1: when $V_I < V_{TND}$ (drive is cutoff): No drain current conduct in either transistor. That means the load transistor must be in the linear region of the operation and the output current can be expressed as fellows

$$i_{DL}(linear) = K_L[2(V_{GSL} - V_{TNL})V_{DSL} - V_{DSL}^2]$$

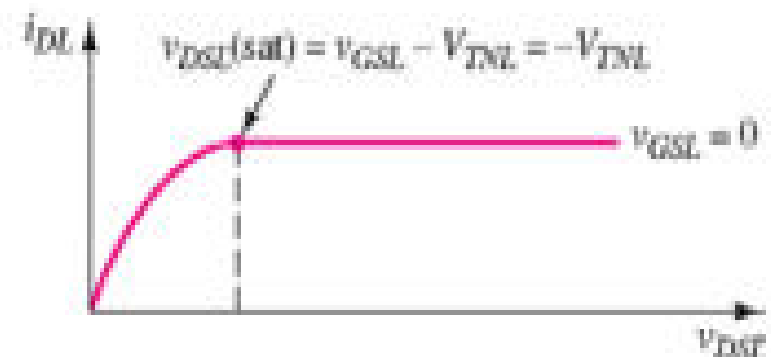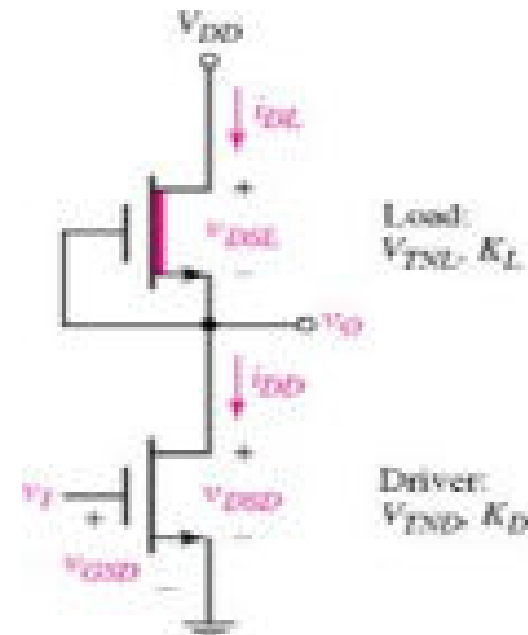Since $V_{GSL} = 0$, and $i_{DL=0}$

$$0 = -K_L[2V_{TNL}V_{DSL} + V_{DSL}^2]$$

Which gives $V_{DSL} = 0$ thus
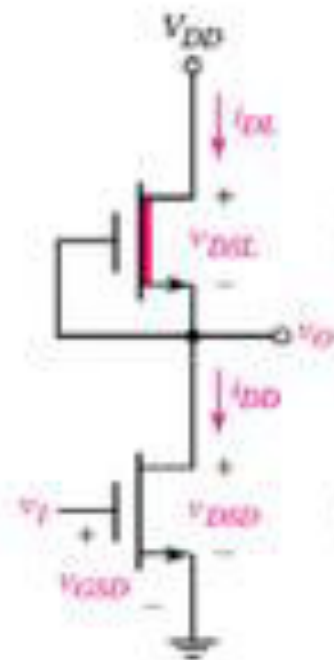
$$\mathbf{V_O = V_{DD}}$$

This is the advantage of the depletion load inverter over the enhancement load inverter.

Load:
V_{TNL}, K_L

Driver:
V_{TND}, K_D

$v_{DSL}(sat) = v_{GSL} - V_{TNL} = -V_{TNL}$

$v_{GSL} = 0$

NMOS Inverter with Depletion Load

When $v_I > V_{TND}$ driver turns on and in the saturation region; however, load is in the nonsaturation region. Q-point lies between points A and B

Load: V_{TNL}, K_L

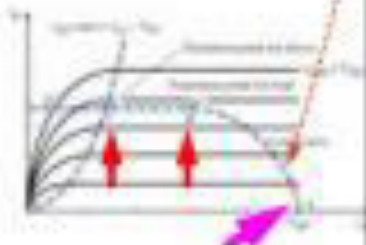two drain currents equal, $i_{DD} = i_{DL}$

$$K_D[v_{GSD} - V_{TND}]^2 = K_L[2(v_{GSL} - V_{TNL})v_{DSL} - v_{DSL}^2]$$

$v_{GSL} = 0$

$$K_D[v_I - V_{TND}]^2 = K_L[2(-V_{TNL})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

Driver: V_{TND}, K_D

There are two transition points
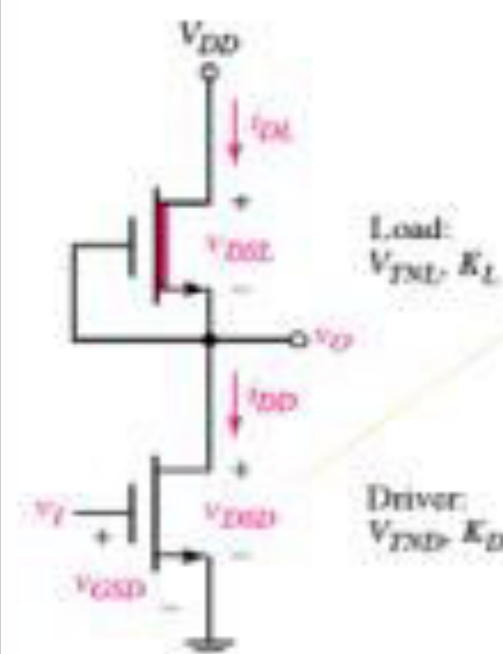one for the load and one for the driver.

B   C

transition point for the load

$$v_{DSL} = V_{DD} - V_{Ot} = v_{GSL} - V_{TNL} = -V_{TNL}$$

$V_{Ot} = V_{DD} + V_{TNL}$ Since V_{TNL} is negative, the output voltage at the transition point is less than V_{DD}.

NMOS Inverter with Depletion Load

transition point for the driver

$$v_{DSD} = v_{GSD} - V_{TND}, \qquad v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$V_{OT} = V_{It} - V_{TND}$$
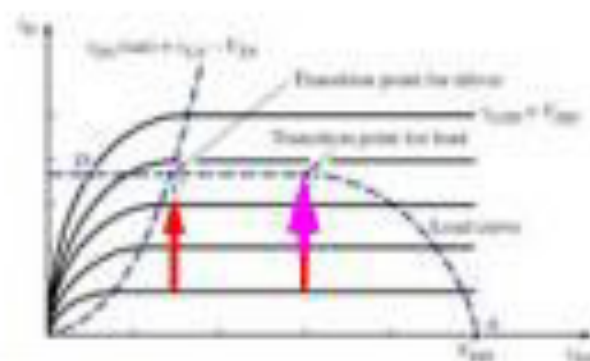
Load: V_{TNL}, K_L

Driver: V_{TND}, K_D

When the Q-point lies between points B and C both devices are in the saturation region,
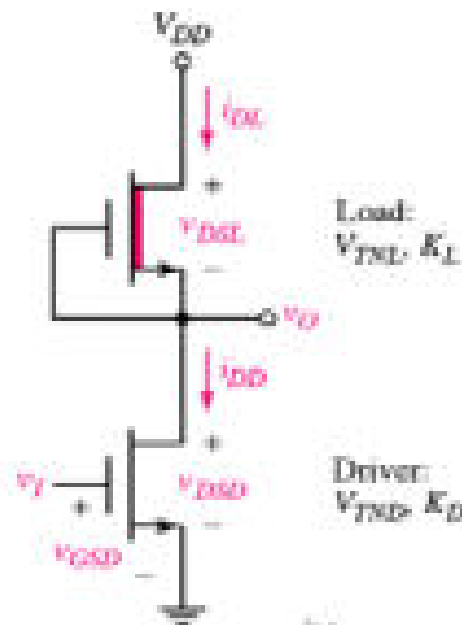
$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$\sqrt{\frac{K_D}{K_L}}(v_I - V_{TND}) = -V_{TNL}$$

This implies that input voltage is constant as the Q-point passes this region.
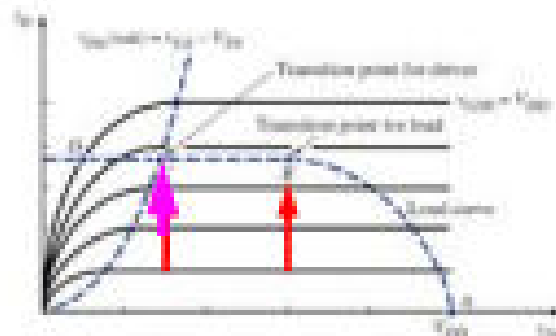
NMOS Inverter with Depletion Load

Load:
V_{TNL}, K_L

Driver:
V_{TND}, K_D

driver is biased in the nonsaturation region while the load is in the saturation region. Q-point is between points C and D

$$K_D\left[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2\right] = K_L(v_{GSL} - V_{TNL})^2$$

$$\frac{K_D}{K_L}\left[2(v_I - V_{TND})v_O - v_O^2\right] = (-V_{TNL})^2$$

This implies that input and output voltages are not linear in this region.

NMOS Inverter with Depletion Load

Voltage transfer characteristics,
NMOS inverter with depletion load,

I	Q_1	Cutoff
	Q_2	Triode (Nonsaturation)
II	Q_1	Saturation
	Q_2	Triode
III	Q_1	Saturation
	Q_2	Saturation
IV	Q_1	Triode
	Q_2	Saturation