Unit 2
MOS Inverters

# Propagation Delay, T_p
D(Dynamic Behavior)

Propagation Delay, T_p

- Defines how quickly output is affected by input
- Measured between 50% transition from input to output
- t_{pLH} defines delay for output going from low to high
- t_{pHL} defines delay for output going from high to low
- Overall delay, t_p, defined as the ***average*** of t_{pLH} and t_{pHL}

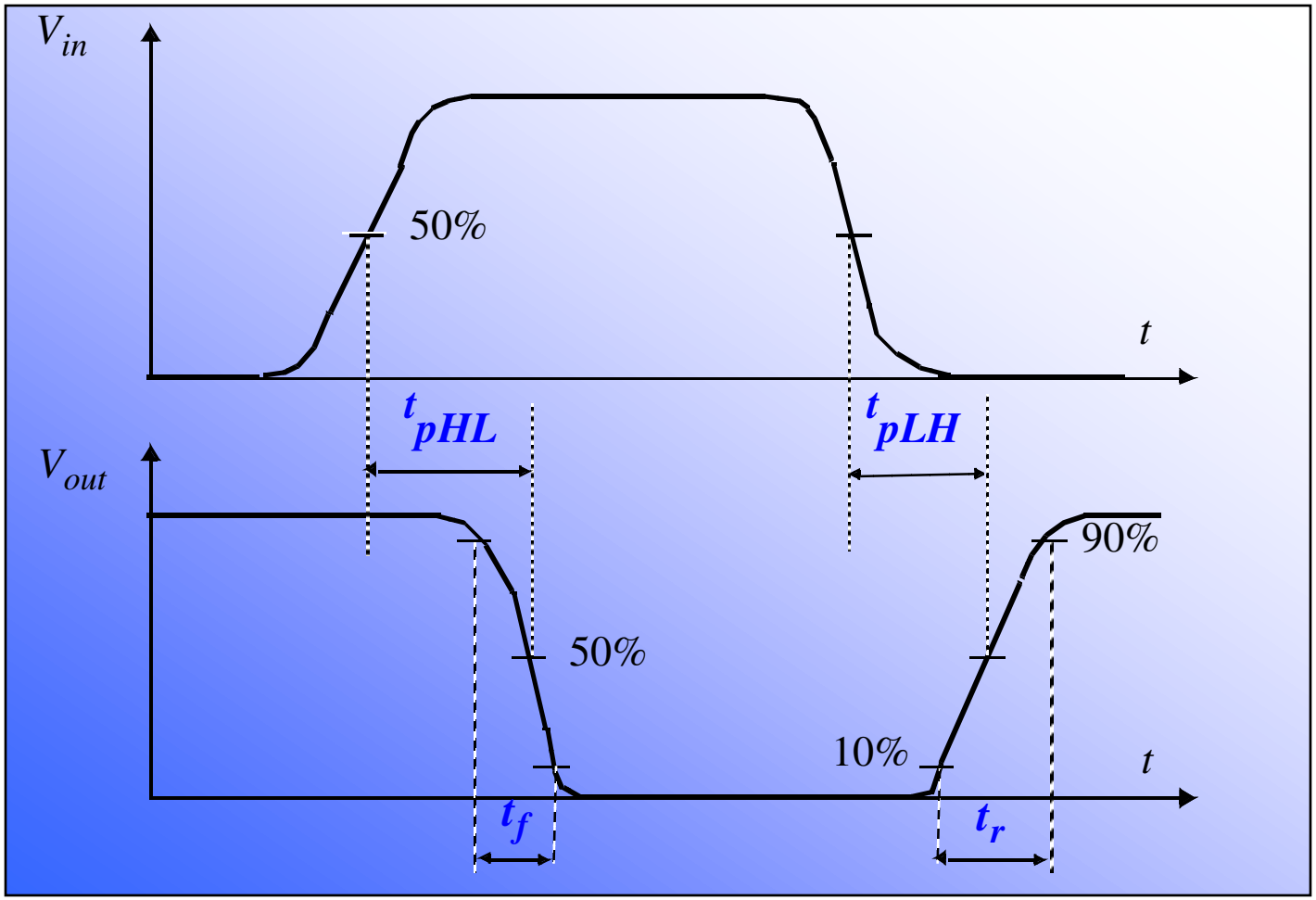
Dynamic Behavior

Rise and fall time, T_r and T_f

- Defines slope of the signal
- Defined between the 10% and 90% of the signal swing

Propagation delay and rise and fall times affected by the fan-out due to larger capacitance loads

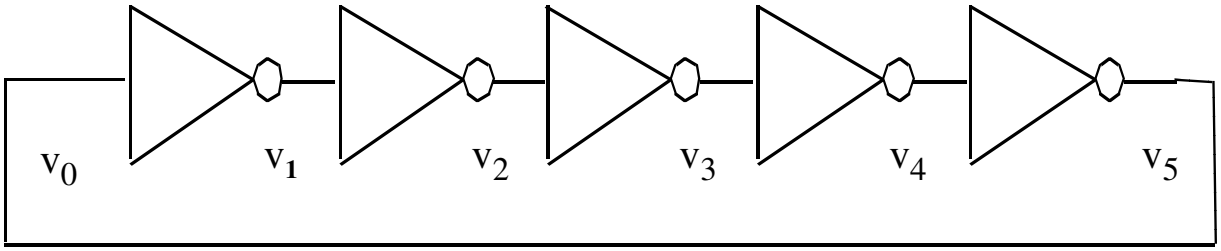
Delay Definitions

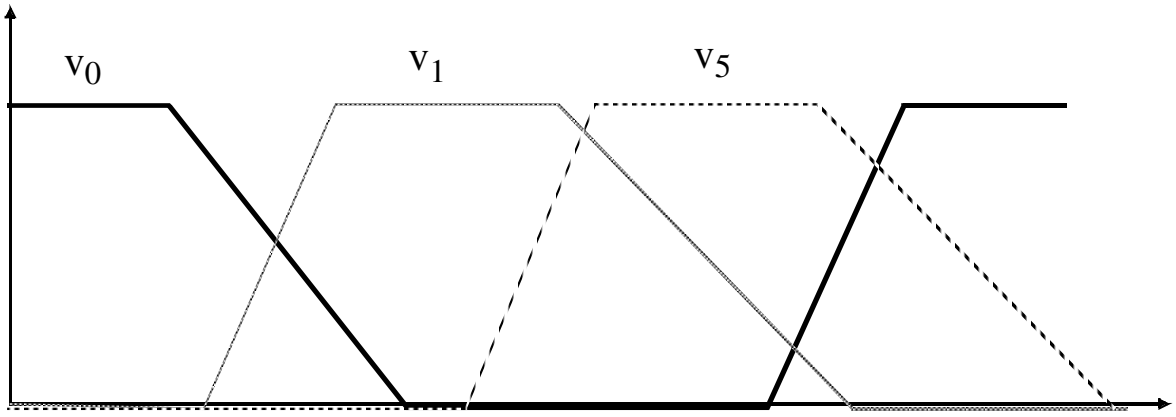


The Ring Oscillator

- A standard method is needed to measure the gate delay
- It is based on the ***ring oscillator***
- $2Nt_p >> t_f + t_r$ for proper operation

Ring Oscillator

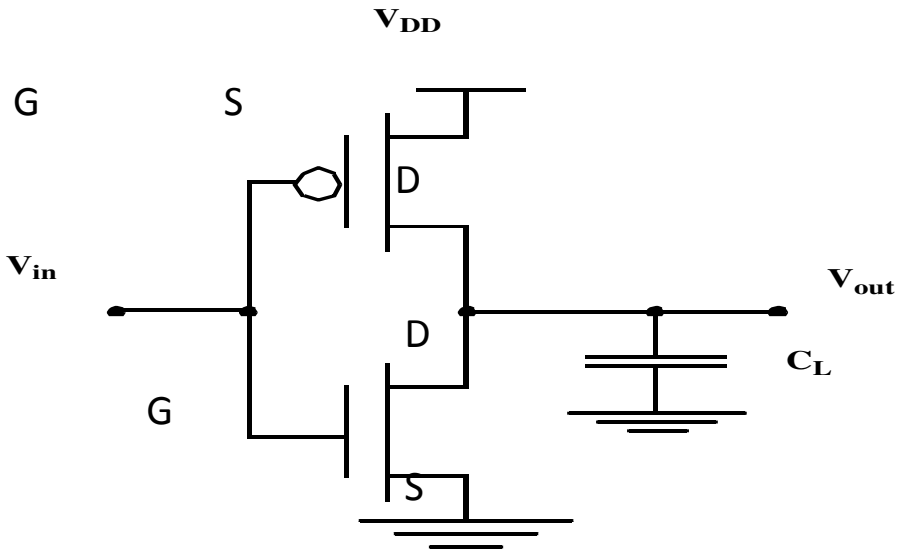




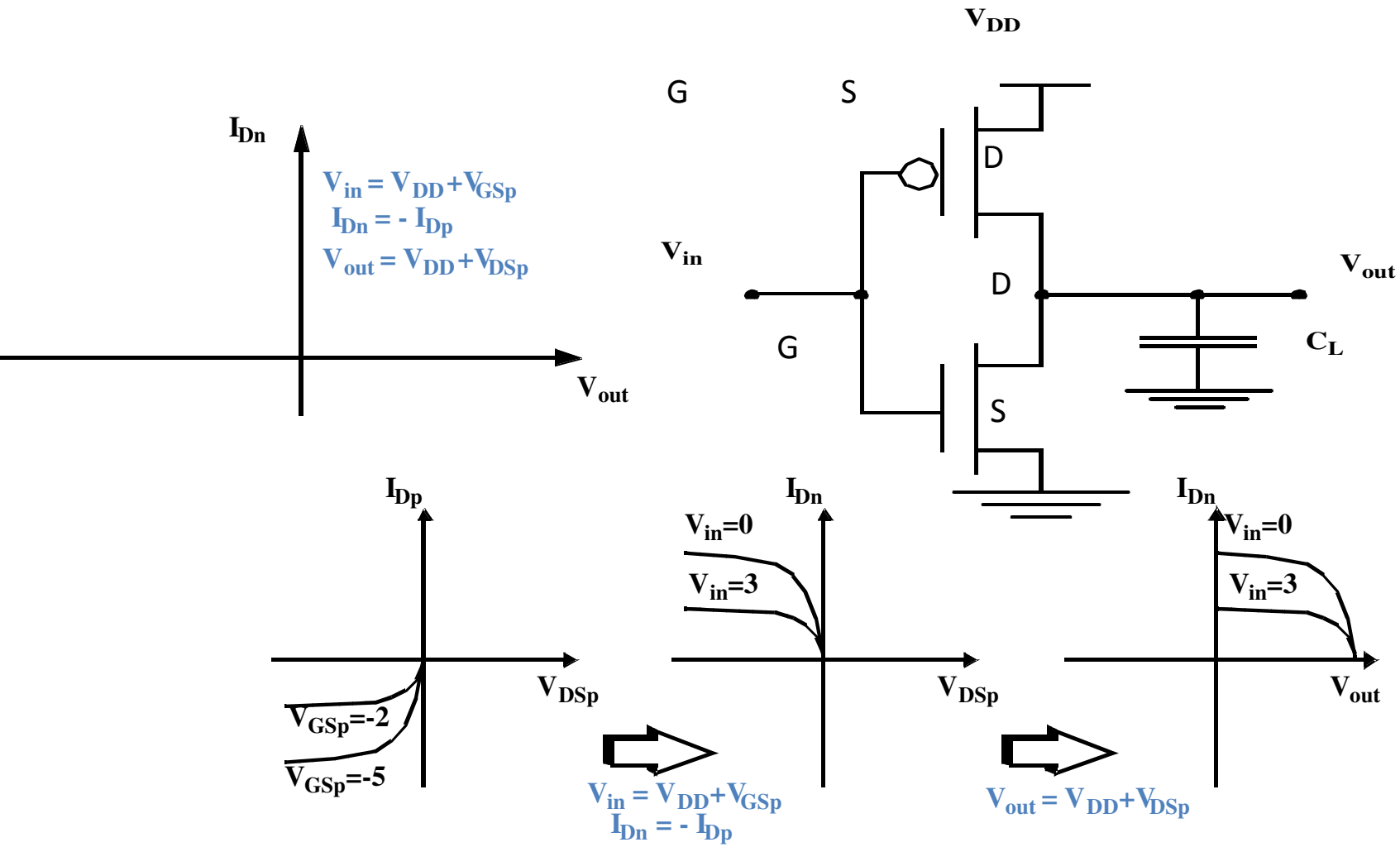
$$T = 2 \times t_p \times N$$

Voltage Transfer Characteristic

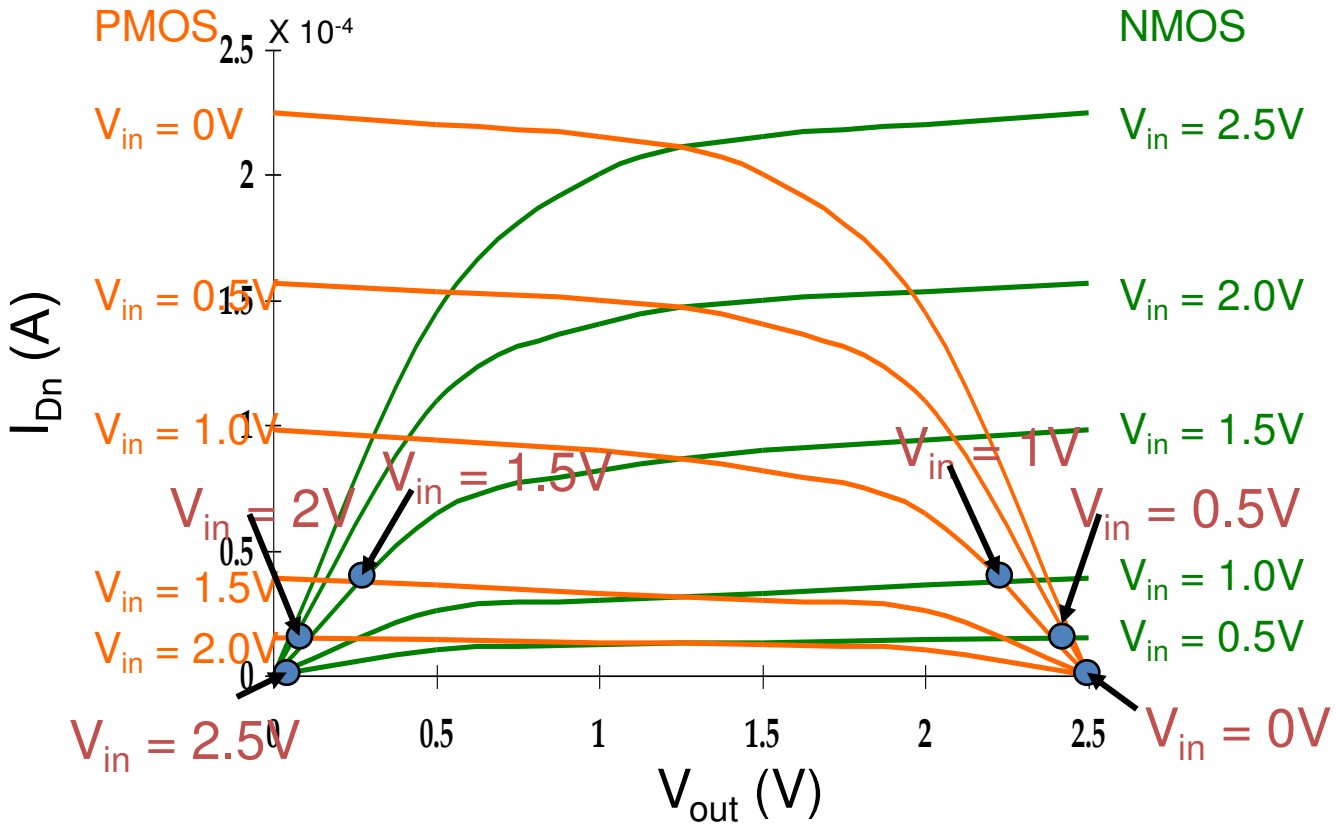
CMOS Inverter Load Characteristics



PMOS Load Lines

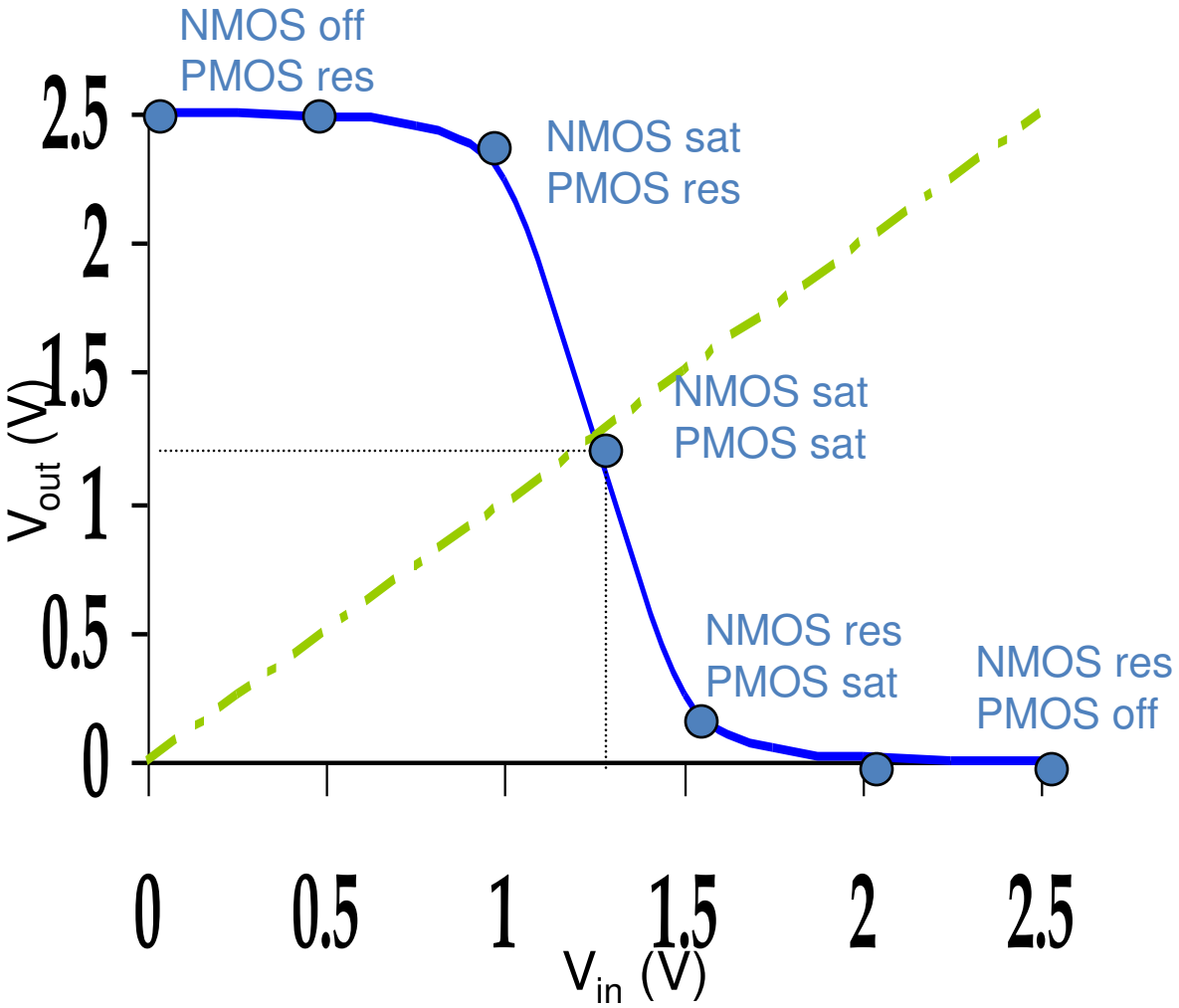


CMOS Inverter Load Lines



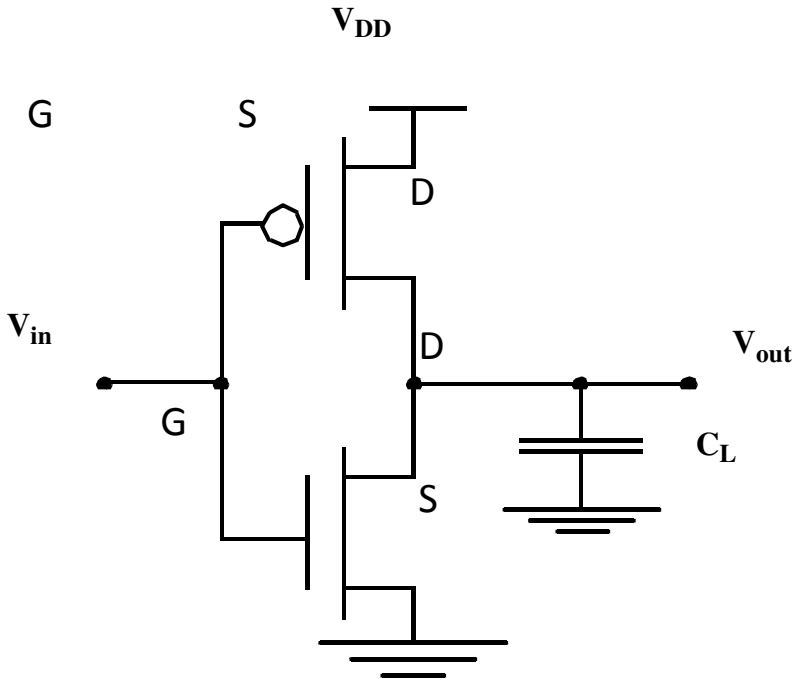
0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

CMOS Inverter VTC



	Cutoff	Linear	Saturation
pMOS	$V_{in} - V_{DD} = V_{GS} > V_T$	$V_{in} - V_{DD} = V_{GS} < V_T$ $V_{in} - V_{out} = V_{GD} < V_T$	$V_{in} - V_{DD} = V_{GS} > V_T$ $V_{in} - V_{out} = V_{GD} > V_T$
nMOS	$V_{in} = V_{GS} < V_T$	$V_{in} = V_{GS} > V_T$ $V_{in} - V_{out} = V_{GD} > V_T$	$V_{in} = V_{GS} > V_T$ $V_{in} - V_{out} = V_{GD} < V_T$

Regions of operations
For nMOS and pMOS
In CMOS inverter



CMOS Inverter Load Characteristics

- For valid dc operating points:
  - current through NMOS = current through PMOS
  - => dc operating points are the intersection of load lines
- All operating points located at high or low output levels
  - => VTC has narrow transition zone
  - high gain of transistors during switching
  - transistors in saturation
    - high transconductance (g_m)
    - high output resistance (voltage controlled current source)

Switching Threshold

- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)

$$V_M \approx rV_{DD}/(1 + r) \text{ where } r = k_p V_{DSATp}/k_n V_{DSATn}$$

- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS transistors

- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k_p' V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

Switch Threshold Example

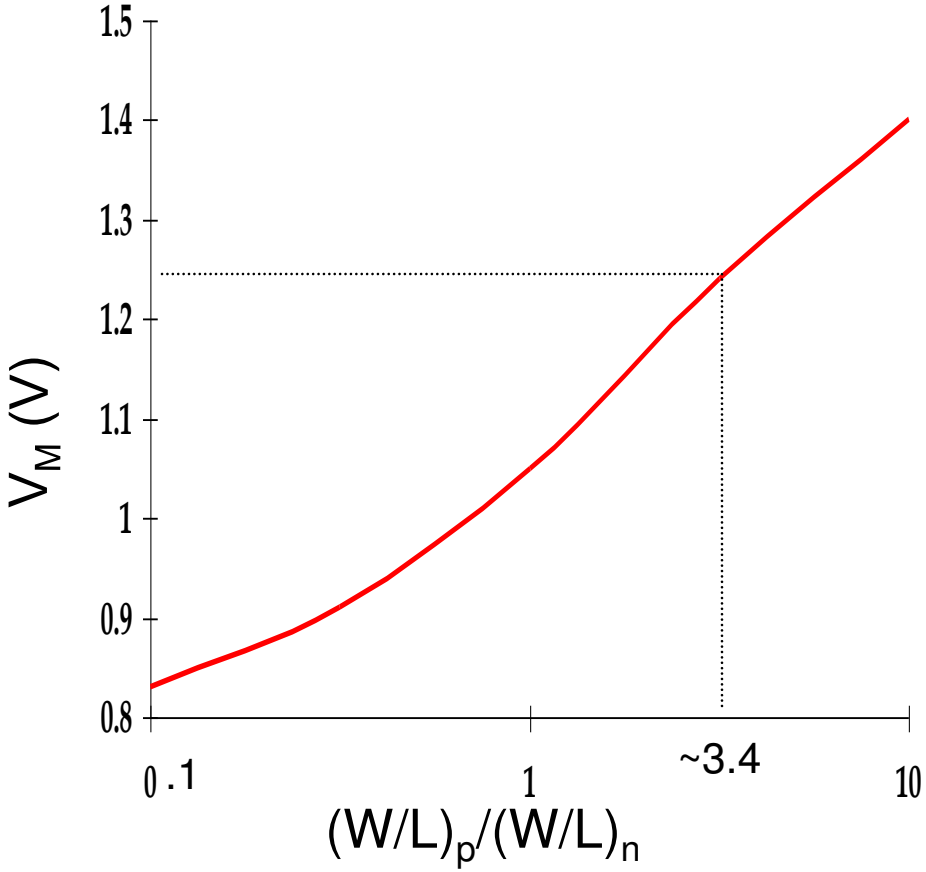
- In 0.25 μm CMOS process, using parameters from table, V_{DD} = 2.5V, and minimum size NMOS ($(W/L)_n$ of 1.5)

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	k'(A/V^2)	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$$(W/L)_p = 3.5 \times 1.5 = 5.25 \text{ for a } V_M \text{ of } 1.25V$$

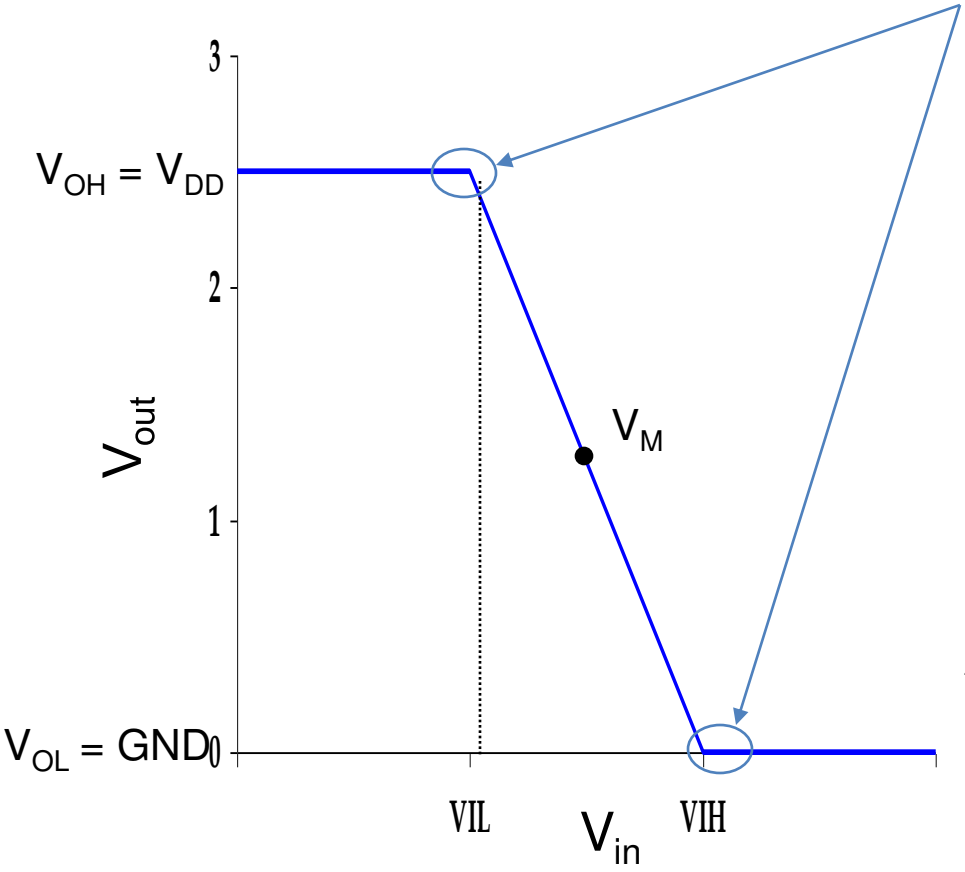
Simulated Inverter V_M



- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}

Note: **x-axis is semilog**

Noise Margins Determining V_{IH} and V_{IL}



By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

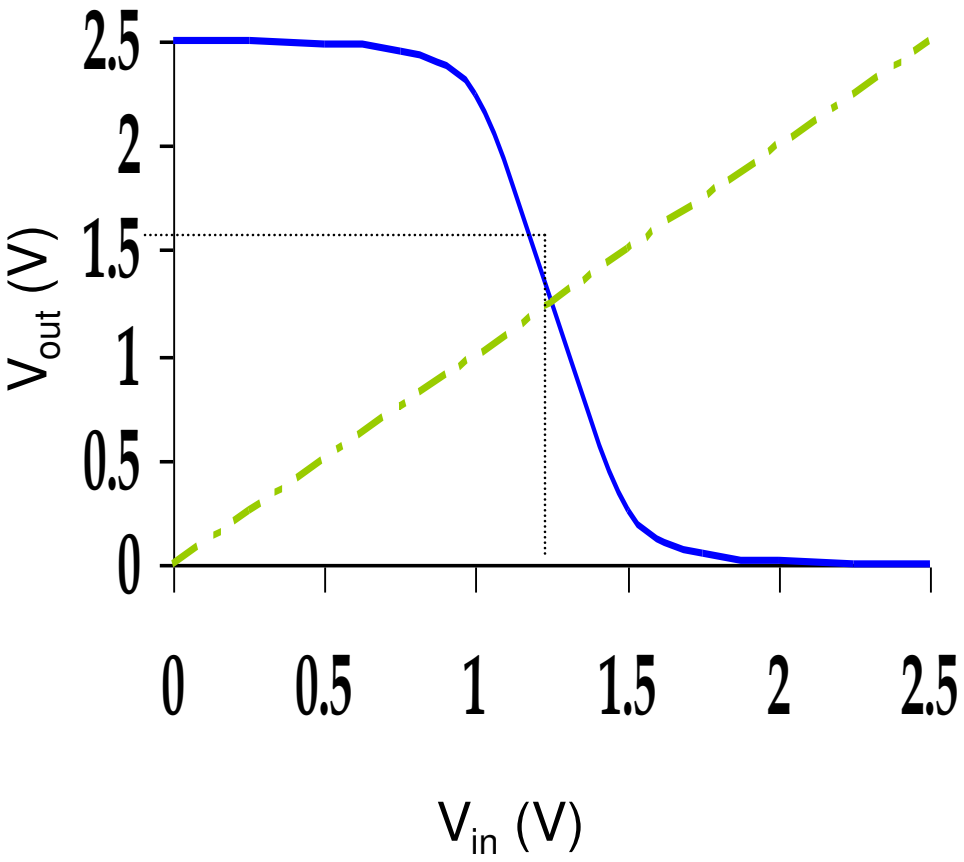
$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL} - GND$

Approximating:
$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

A piece-wise linear approximation of VTC

So high gain in the transition region is very desirable

CMOS Inverter VTC from Simulation



0.25um, $(W/L)_p/(W/L)_n = 3.4$
$(W/L)_n = 1.5$ (min size)
$V_{DD} = 2.5V$

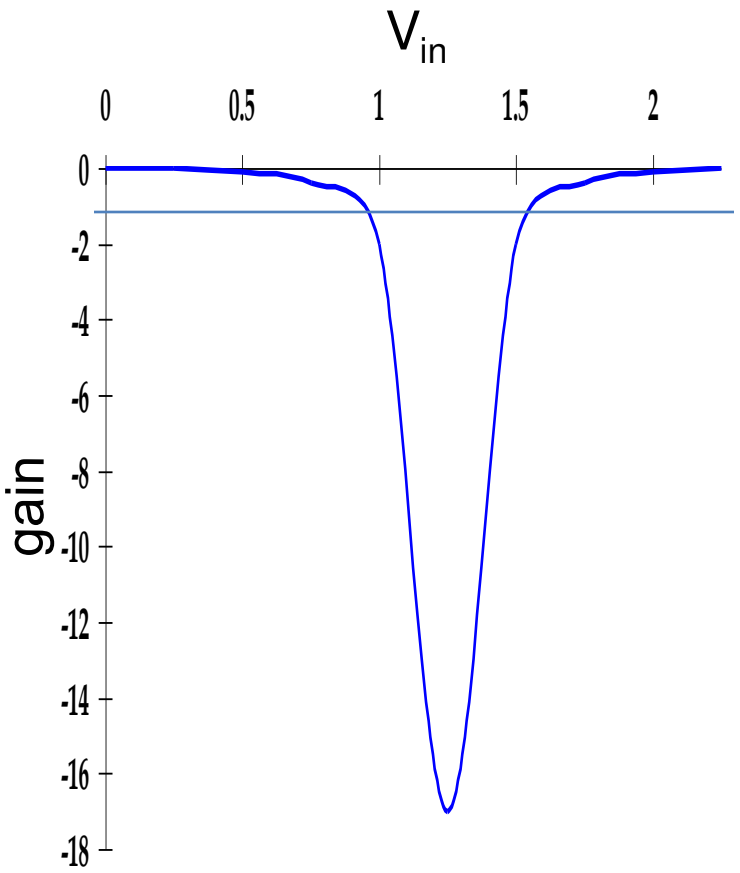
$V_M \approx 1.25V$, $g = -27.5$

$V_{IL} = 1.2V$, $V_{IH} = 1.3V$
$NM_L = NM_H = 1.2$

(actual values are
$V_{IL} = 1.03V$, $V_{IH} = 1.45V$
$NM_L = 1.03V$ & $NM_H = 1.05V$)

Output resistance
low-output = 2.4kΩ
high-output = 3.3kΩ

Gain Determinates



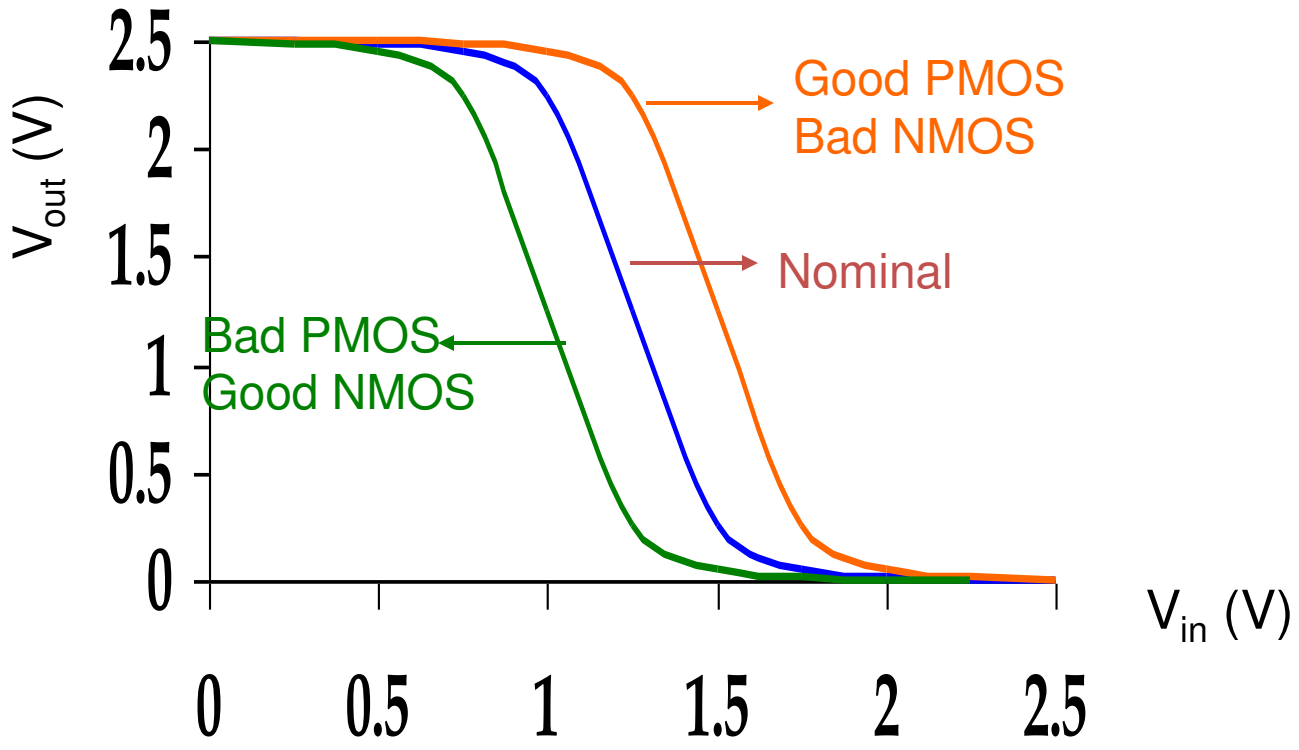
Gain is a function of the current slope in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

✓Determined by technology parameters, especially λ.

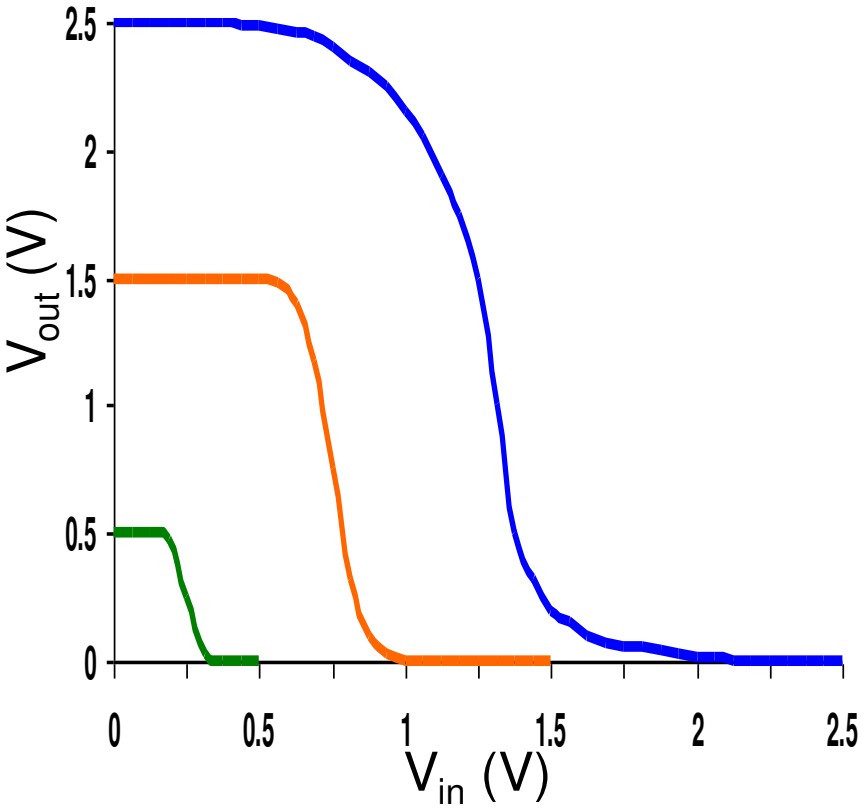
✓Only designer influence through supply voltage and V_M (transistor sizing).

Impact of Process Variation

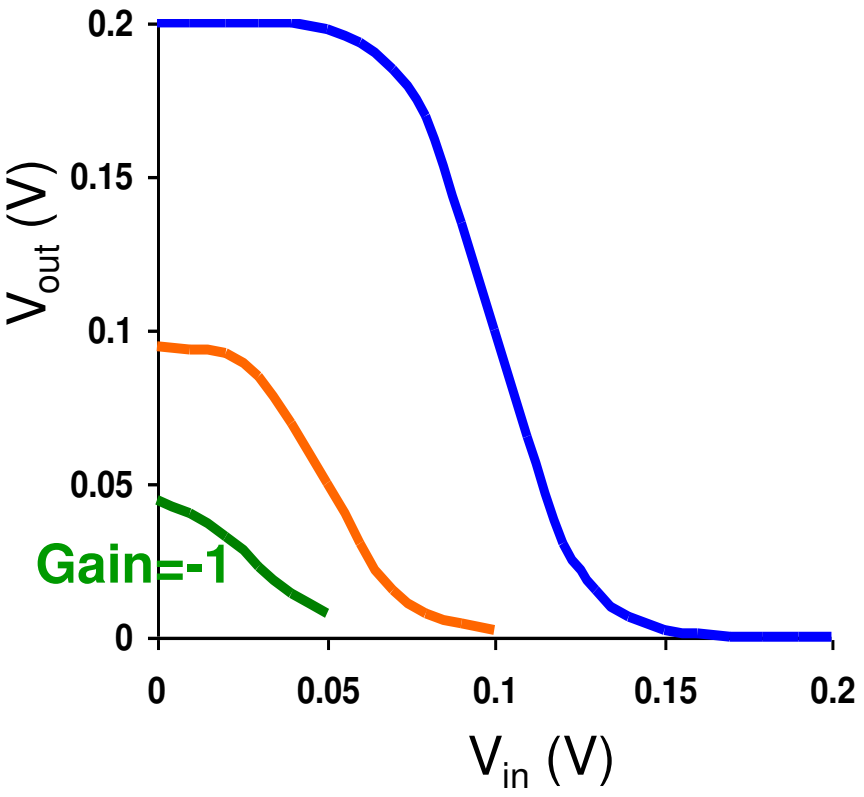


- Pprocess variations (mostly) cause a shift in the switching threshold

Scaling the Supply Voltage



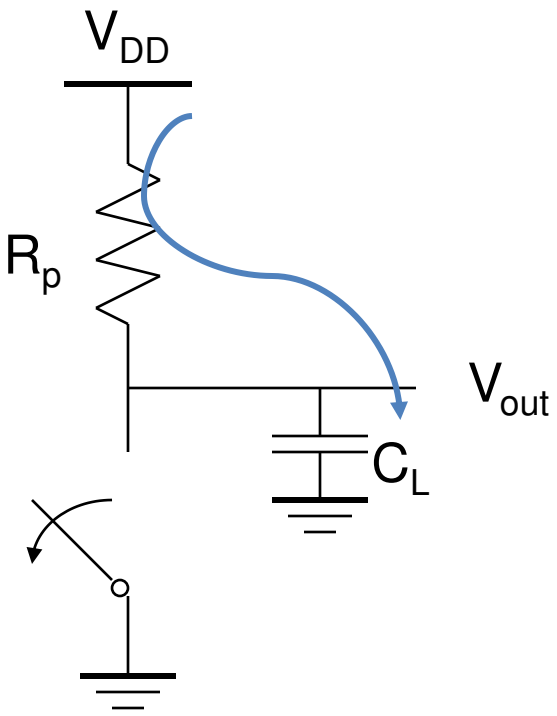
Device threshold voltages are kept (virtually) constant



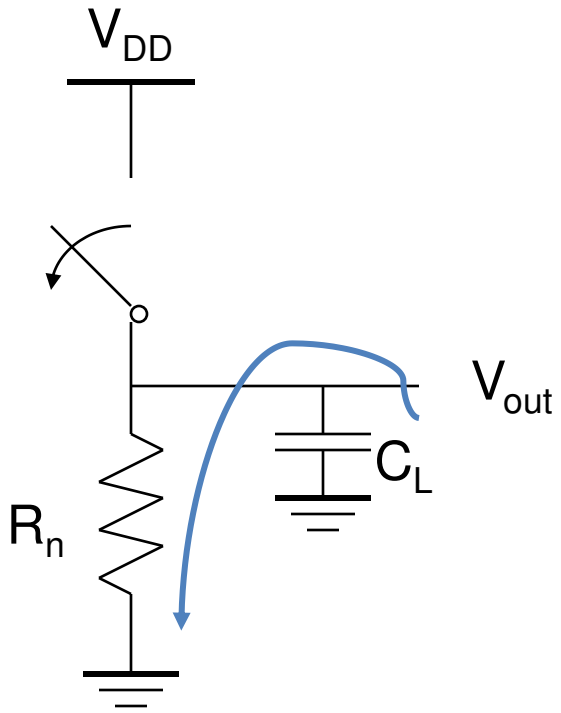
Device threshold voltages are kept (virtually) constant

Propagation Delay

Switch Model of Dynamic Behavior



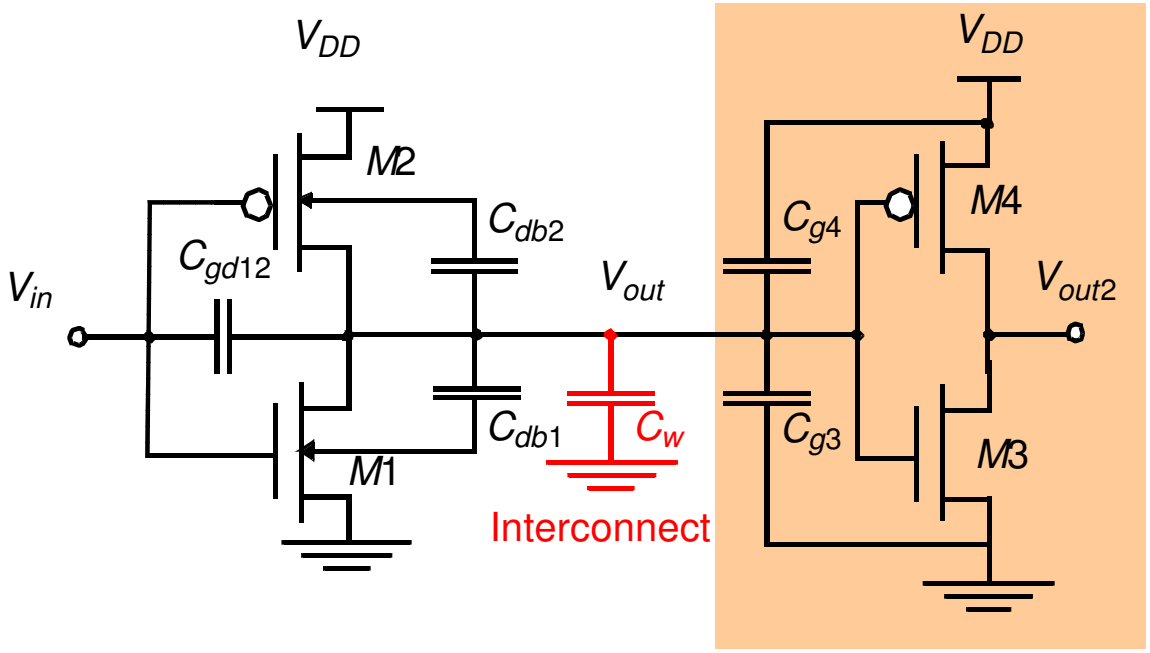
$V_{in} = 0$



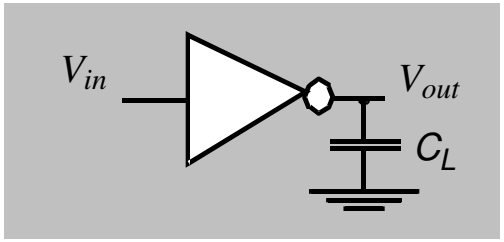
$V_{in} = V_{DD}$

- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

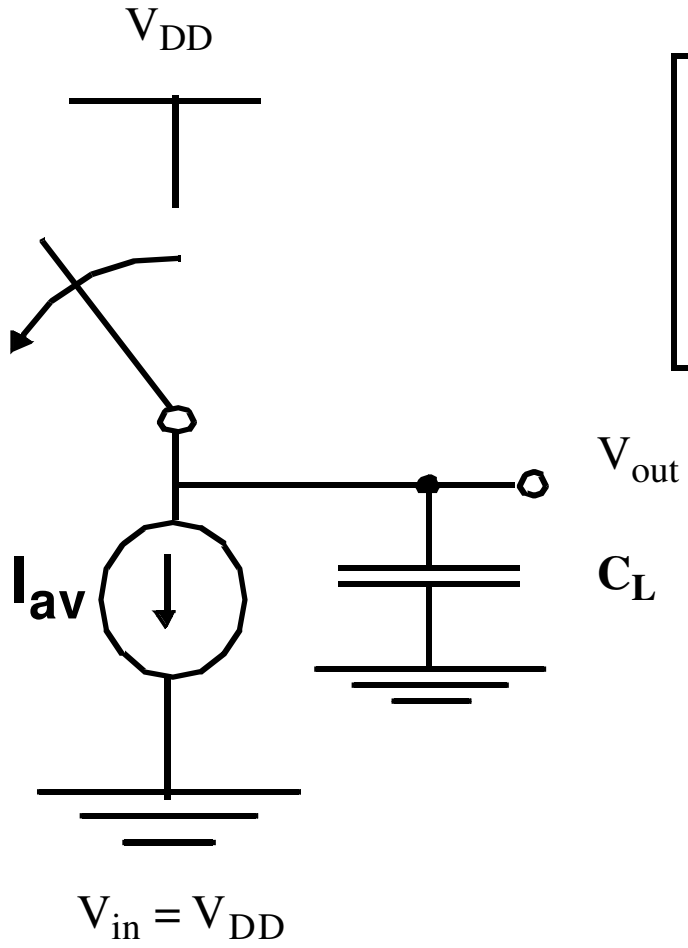
What is the Inverter Driving?



Simplified Model



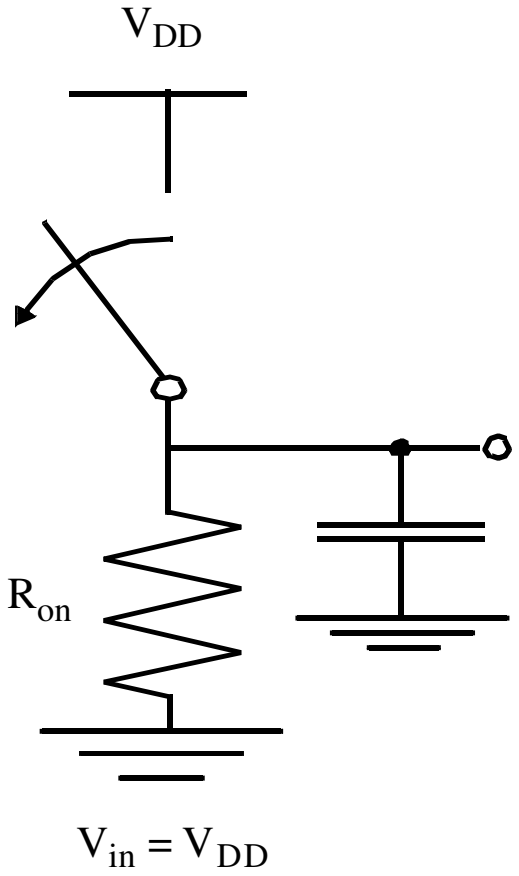
CMOS Inverter Propagation Delay Approach 1



$$t_{pHL} = \frac{C_L \, V_{swing}/2}{I_{av}}$$

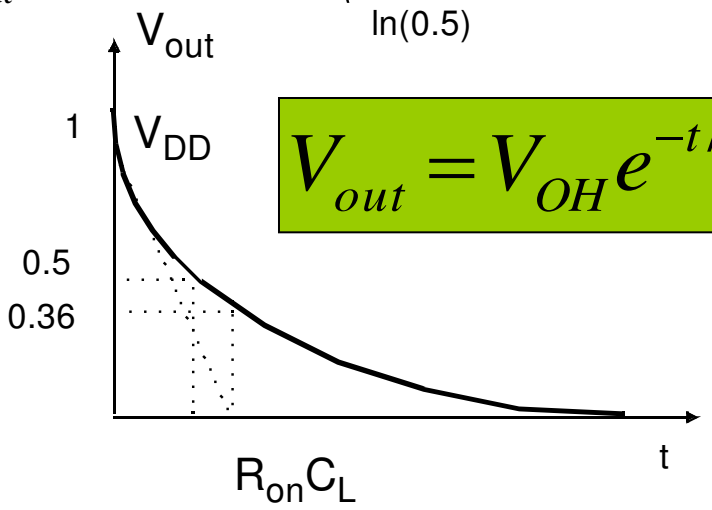
$$\sim \frac{C_L}{k_n \, V_{DD}}$$

CMOS Inverter Propagation Delay Approach 2



$$t_{pHL} = f(R_{on}.C_L) = 0.69\ R_{on}C_L$$

ln(0.5)



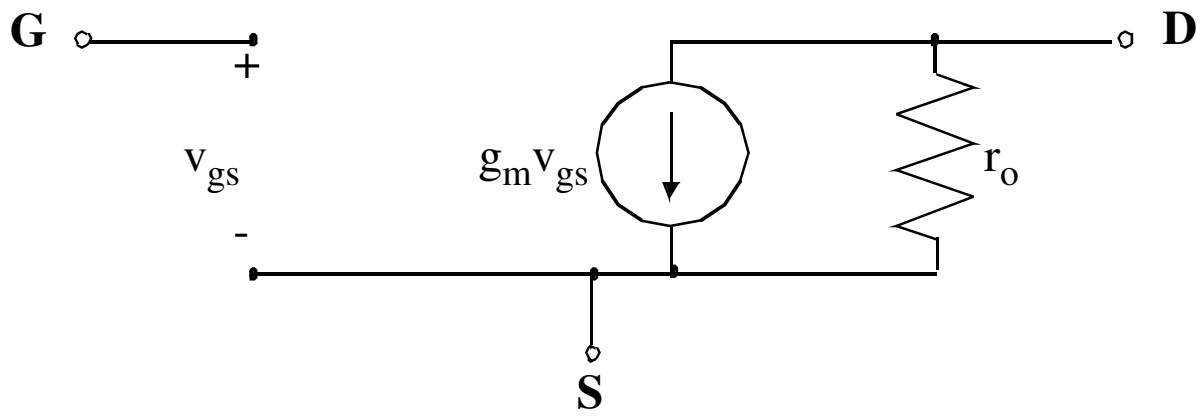
$$V_{out} = V_{OH} e^{-t/(R_{on}C_L)}$$

CMOS Inverter: Transient Response

How can the designer build a fast gate?

- $t_{pHL} = f(R_{on} * C_L)$
- **Keep output capacitance, C_L, small**
  - **low fan-out**
  - **keep interconnections short (floor-plan your layout!)**
- **Decrease on-resistance of transistor**
  - **increase W/L ratio**
  - **make good contacts (slight effect)**

MOS Transistor Small Signal Model



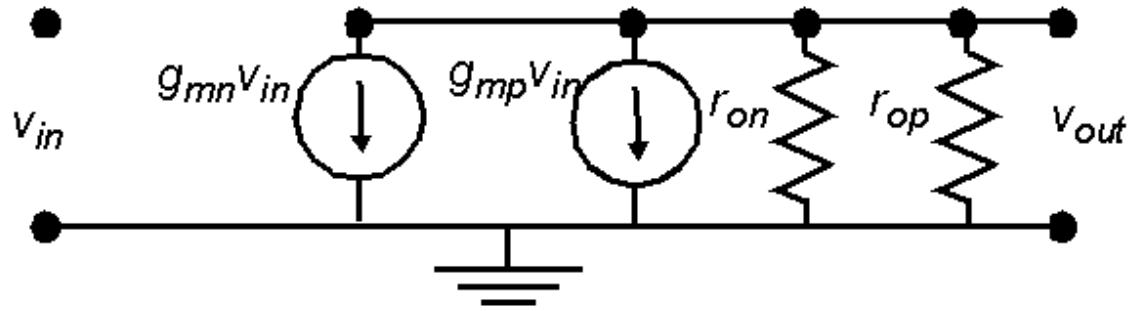
Define

	g_m	r_o
linear	kV_{DS}	$[k(V_{GS}-V_T-V_{DS})]^{-1}$
saturation	$k(V_{GS}-V_T)$	$1/\lambda I_D$

Determining V_{IH} and V_{IL}

At V_{IH} (V_{IL}): $$\frac{\partial V_{out}}{\partial V_{in}} = -1$$

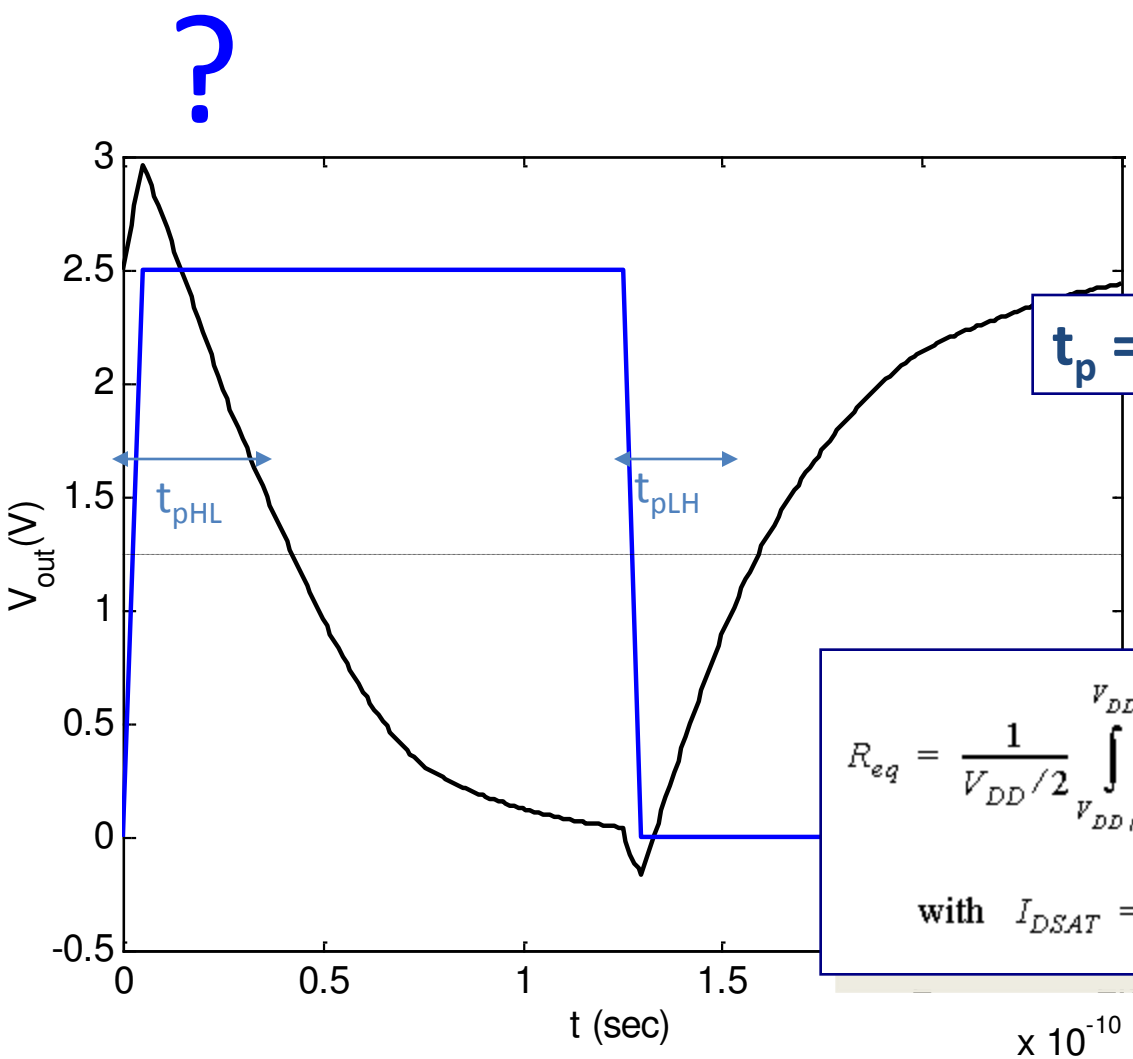
small-signal model of inverter



V_{IH} and V_{IL} are based on derivative of VTC equal to -1

$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \| r_{op}) = -1$$

Transient Response

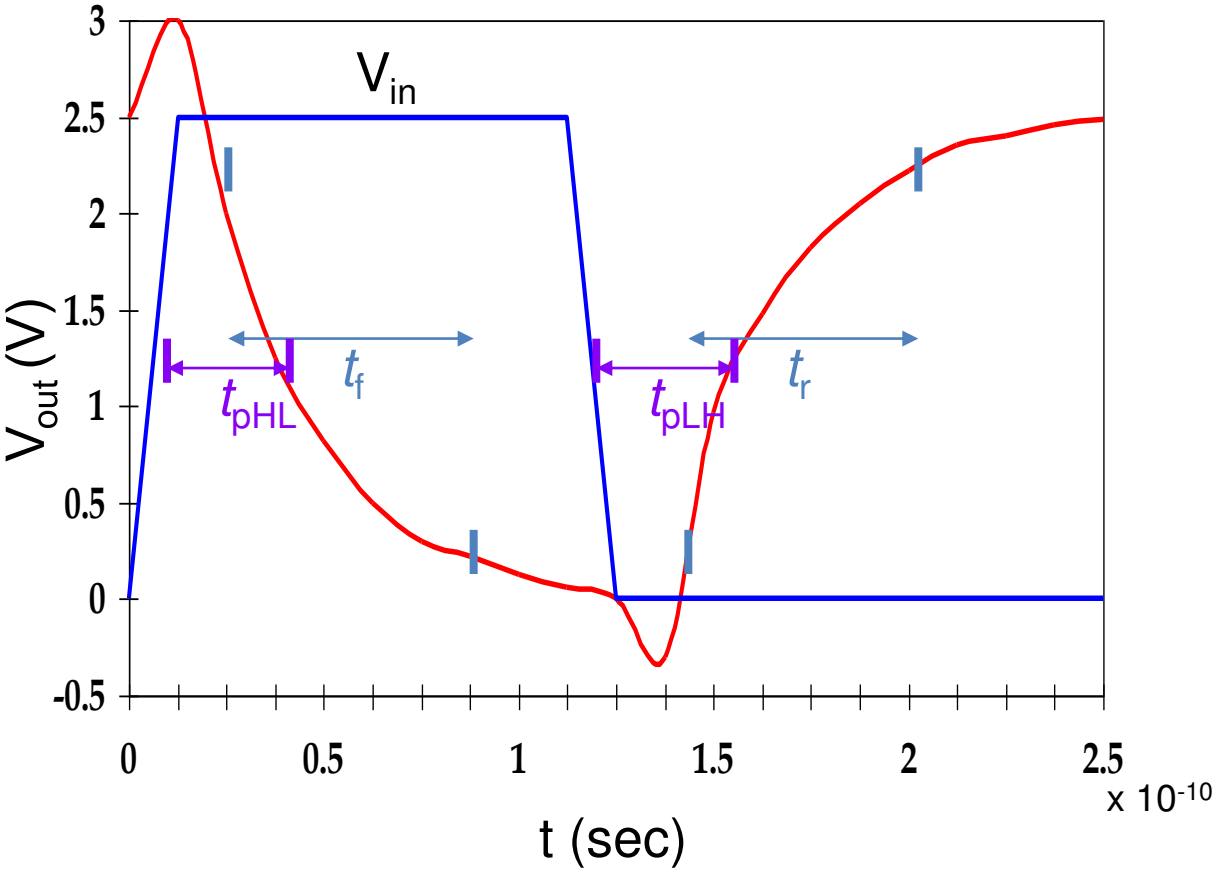


$$t_p = 0.69\, C_L\, (R_{eqn}+R_{eqp})/2$$

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

$$\text{with} \quad I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Inverter Transient Response



V_{DD}=2.5V
0.25μm
W/L_n = 1.5
W/L_p = 4.5
R_{eqn}= 13 kΩ (÷ 1.5)
R_{eqp}= 31 kΩ (÷ 4.5)

t_{pHL} = 36 psec

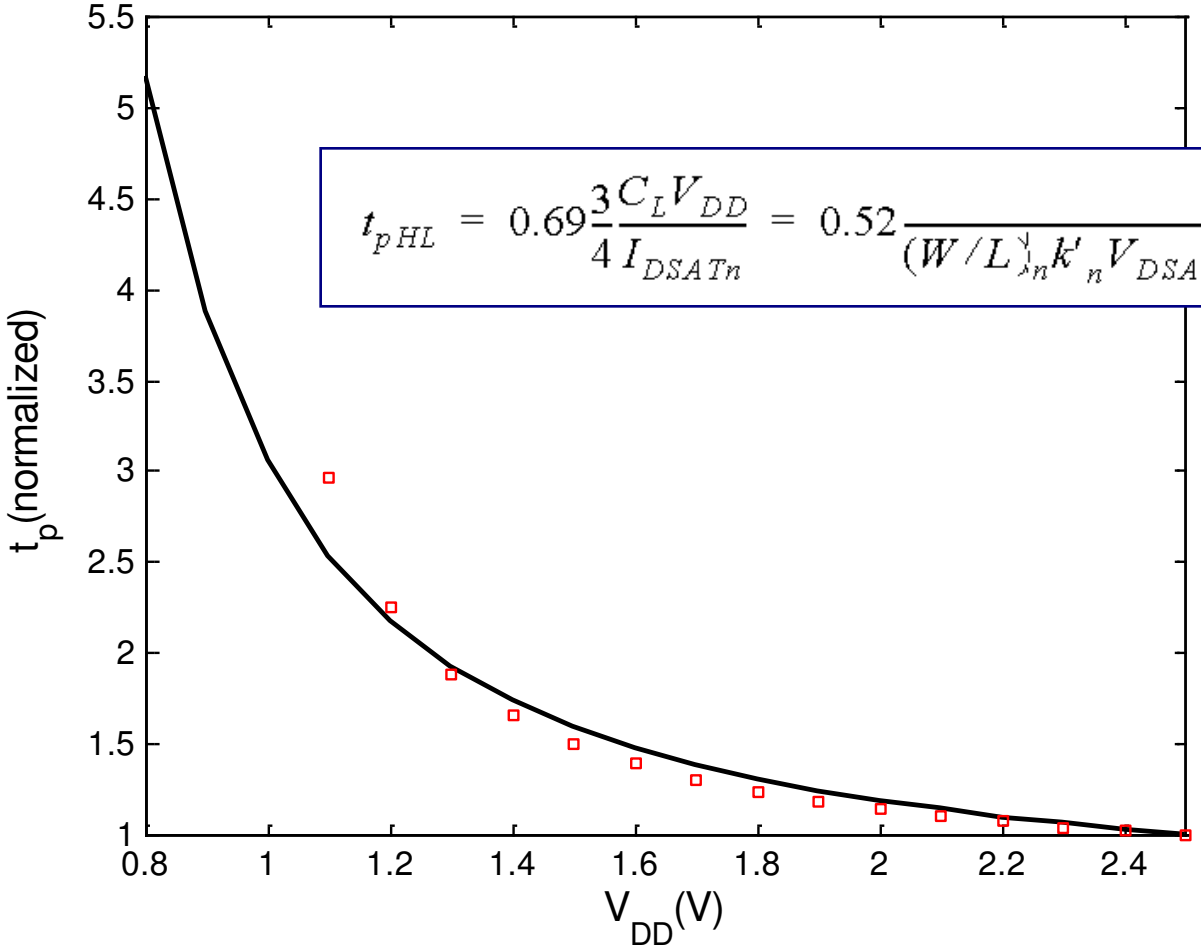
t_{pLH} = 29 psec

so

t_p = 32.5 psec

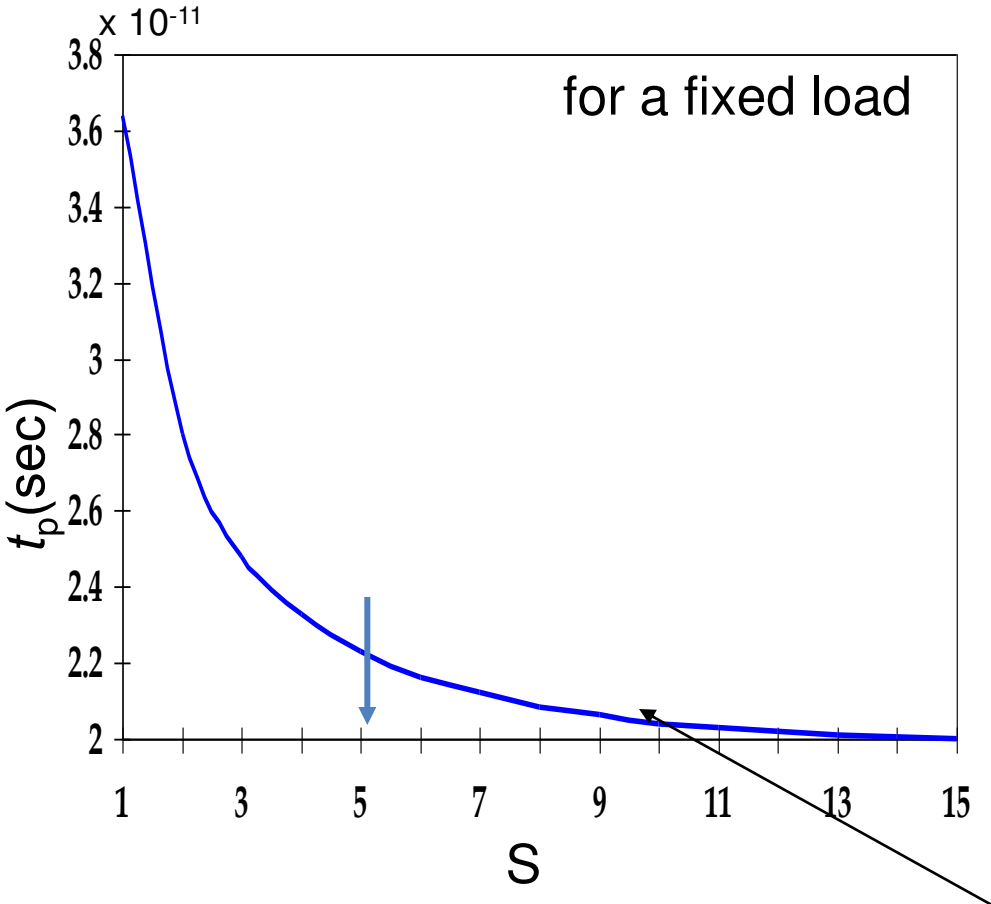
From simulation: t_{pHL} = 39.9 psec and t_{pLH} = 31.7 psec

Delay as a function of V_{DD}



$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

Sizing Impacts on Delay

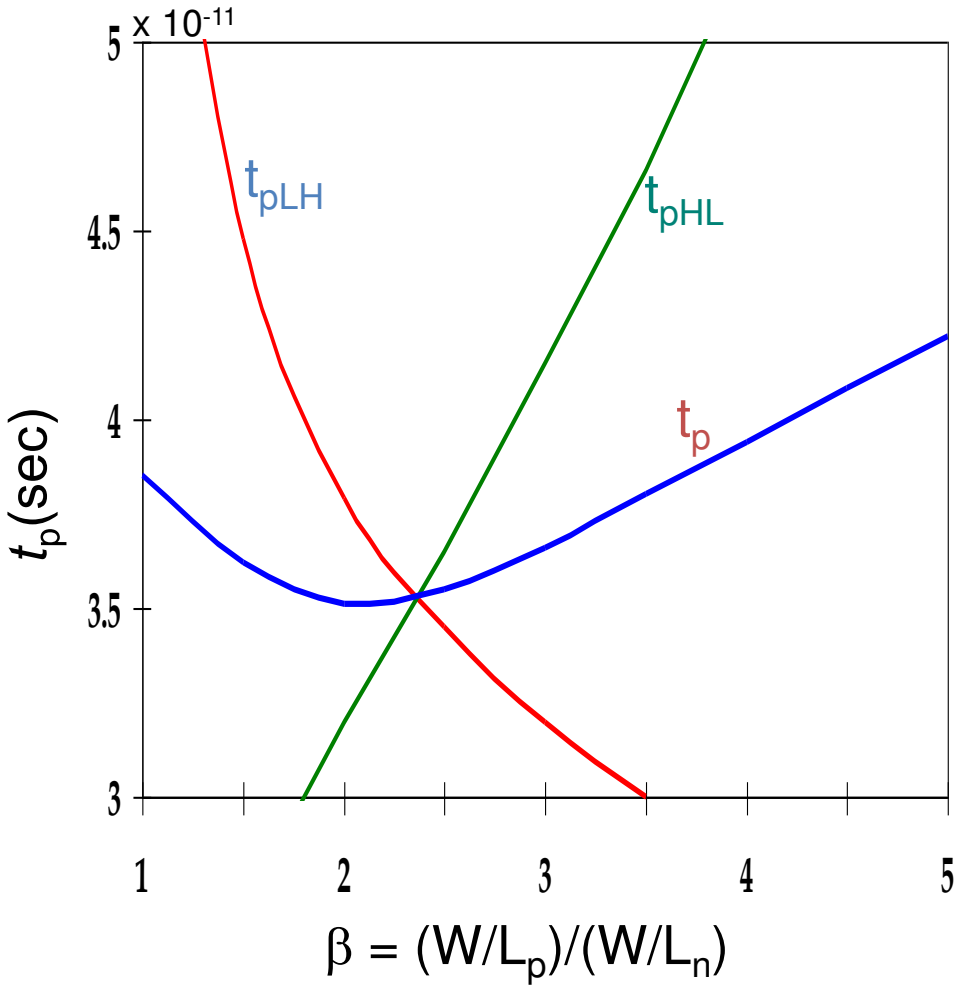


The majority of improvement is obtained for S = 5.

Sizing factors larger than 10 barely yields any extra gain (and cost significantly more area).

self-loading effect (intrinsic capacitance dominates)

PMOS/NMOS Ratio Effects



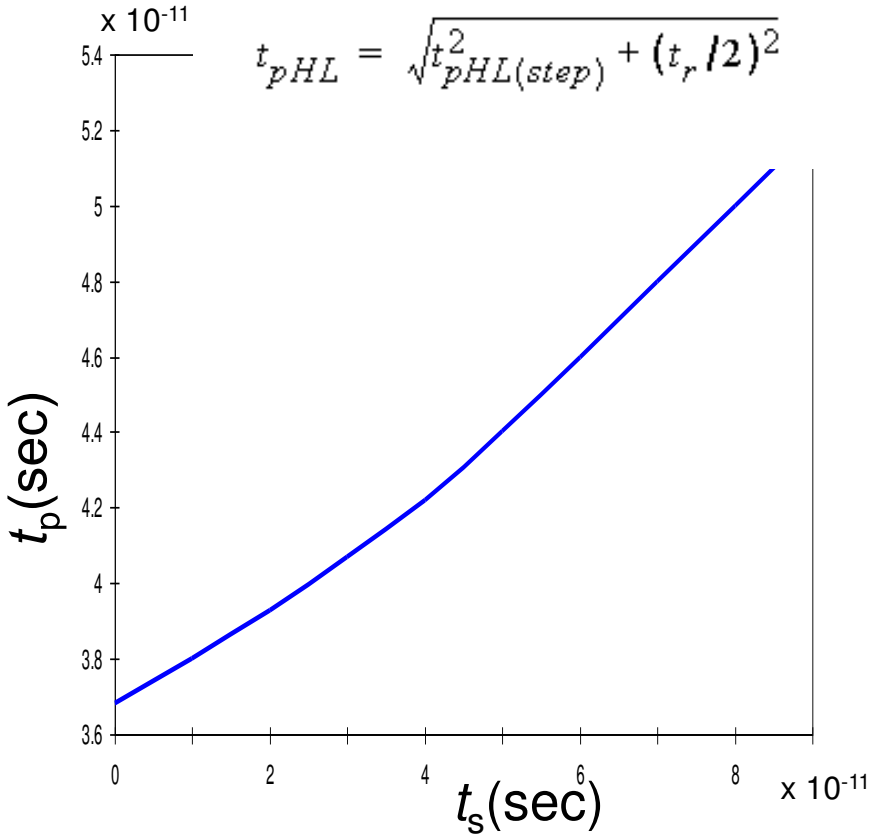
β of 2.4 (= 31 kΩ/13 kΩ) gives symmetrical response

β of 1.6 to 1.9 gives optimal performance

Input Signal Rise/Fall Time

- The input signal changes gradually (and both PMOS and NMOS conduct for a brief time).
- This affects the current available for charging/discharging C_L and impacts propagation delay.

- t_p increases linearly with increasing input rise time, t_r, once $t_r > t_p$
- t_r is due to the limited driving capability of the preceding gate



for a minimum-size inverter with a fan-out of a single gate