Unit 3
Combinational MOS Logic Circuits

Overview

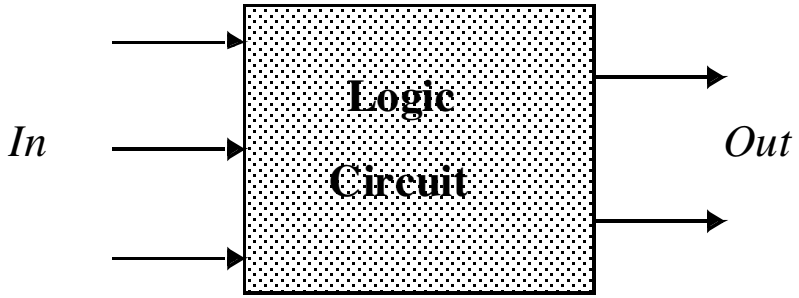
Static CMOS

- **Conventional Static CMOS Logic**
- **Ratioed Logic**
- **Pass Transistor/Transmission Gate Logic**

Dynamic CMOS Logic

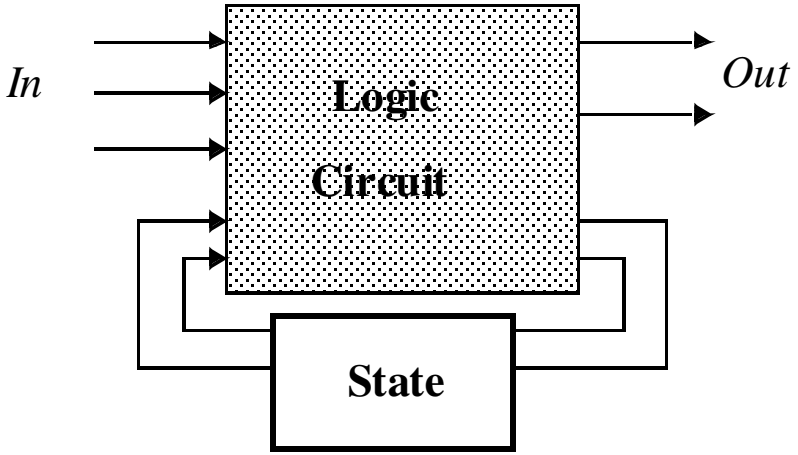
- **Domino**
- **np-CMOS**

Combinational vs. Sequential Logic



(a) Combinational

Output = *f*(*In*)



(b) Sequential

Output = *f*(*In, Previous In*)

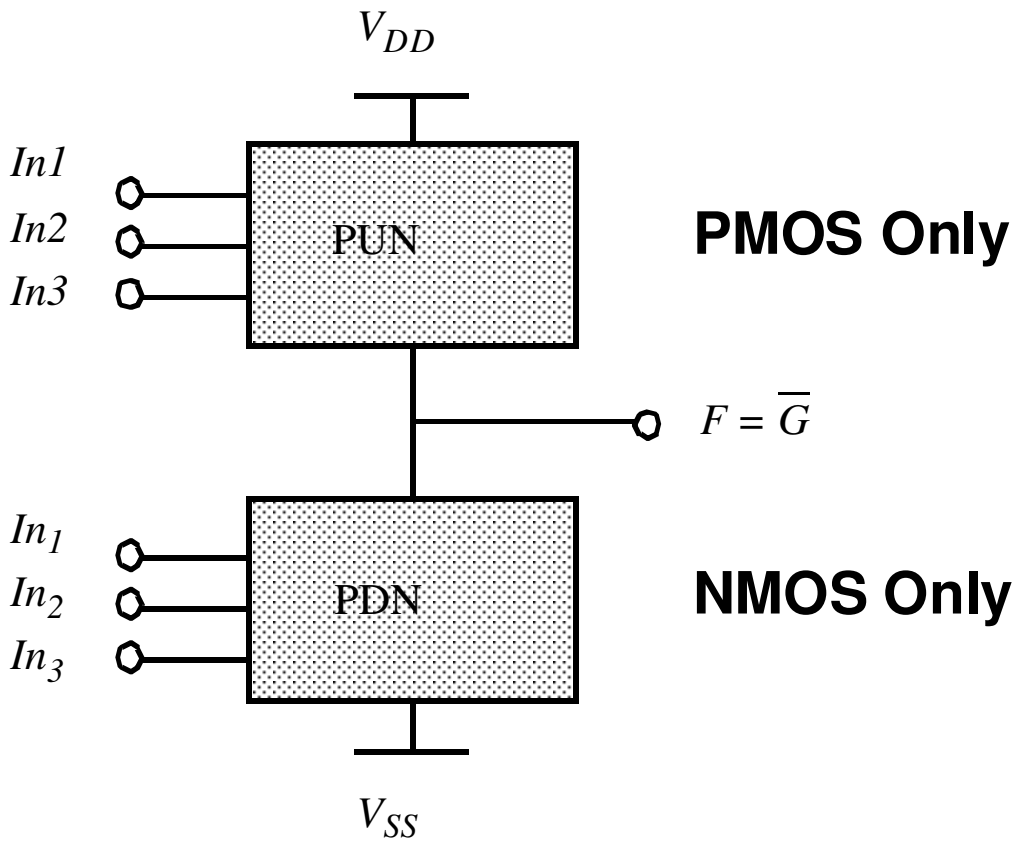
Static CMOS Circuit

At every point in time (except during the switching transients) each gate output is connected to either V_{DD} or V_{ss} via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

This is in contrast to the *dynamic* circuit class, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.

Static CMOS

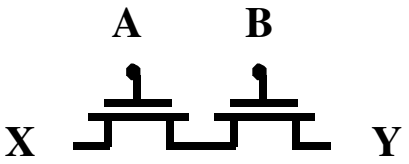


PUN and PDN are Dual Networks

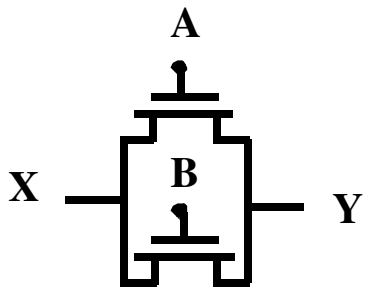
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

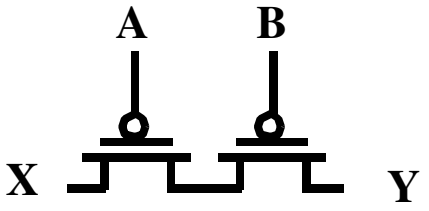


Y = X if A OR B

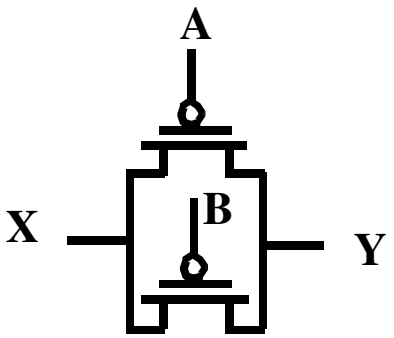
NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$



$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

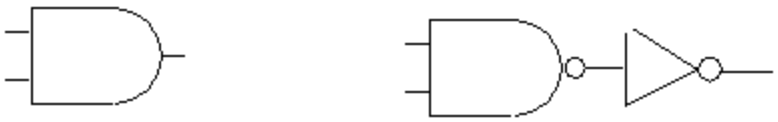
Complementary CMOS Logic Style Construction (cont.)

- **PUP is the DUAL of PDN**
  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- **The complementary gate is inverting**

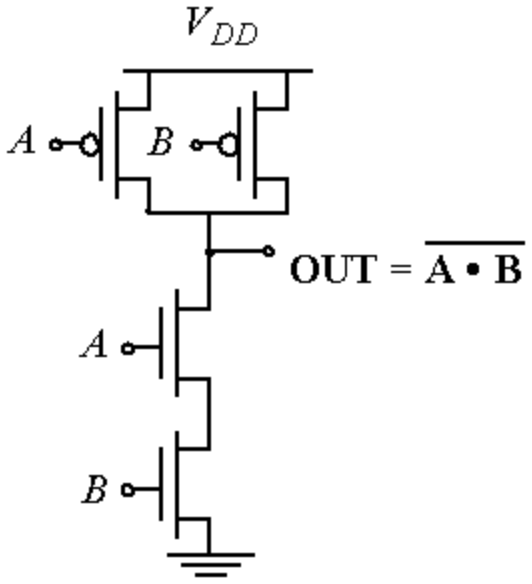


AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B $\Rightarrow$ Conduction to GND

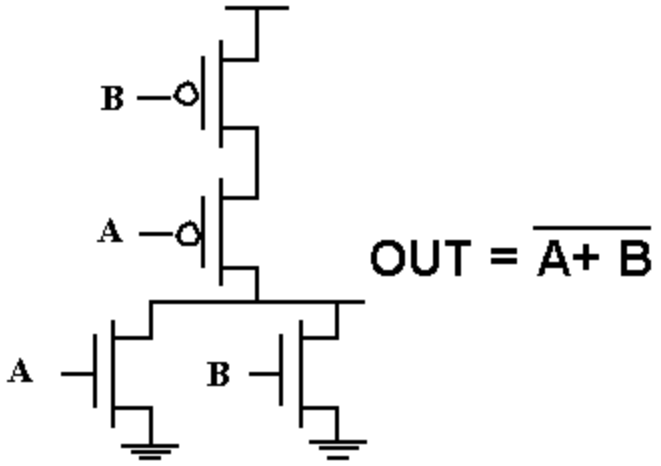
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

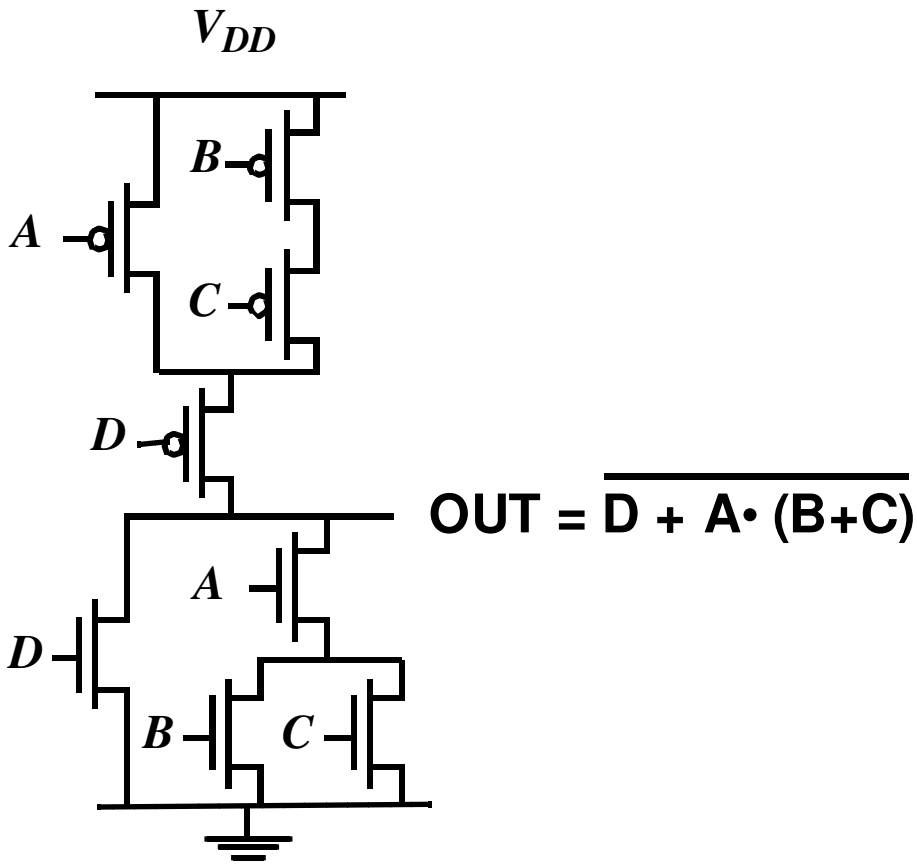
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

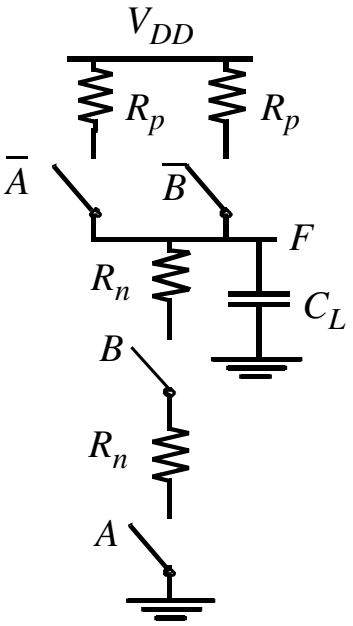
Truth Table of a 2 input NOR gate



Example Gate: COMPLEX CMOS GATE



Analysis of Propagation Delay



2-input NAND

1. Assume R_n=R_p= resistance of minimum sized NMOS inverter

2. Determine "Worst Case Input" transition (Delay depends on input values)

3. Example: t_{pLH} for 2input NAND

- Worst case when only ONE PMOS Pulls up the output node

- For 2 PMOS devices in parallel, the resistance is lower

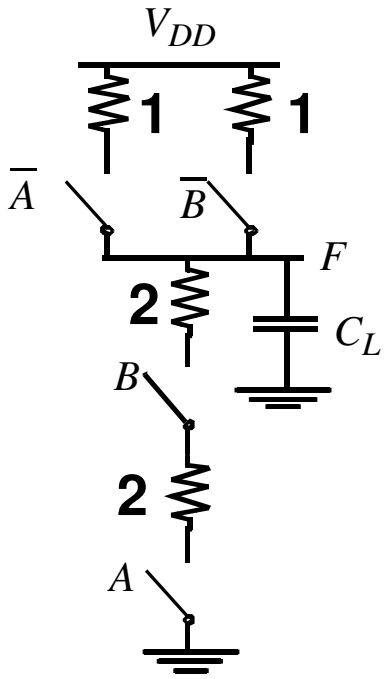
$$t_{pLH} = 0.69 R_p C_L$$

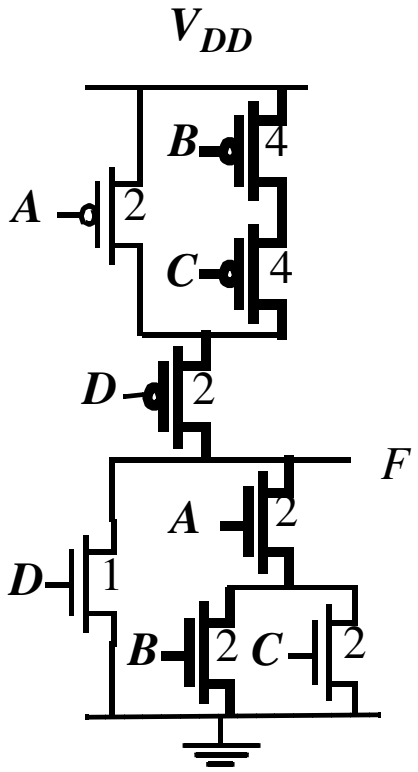
4. Example: t_{pHL} for 2input NAND

- Worst case : TWO NMOS in series

$$t_{pHL} = 0.69(2R_n) C_L$$

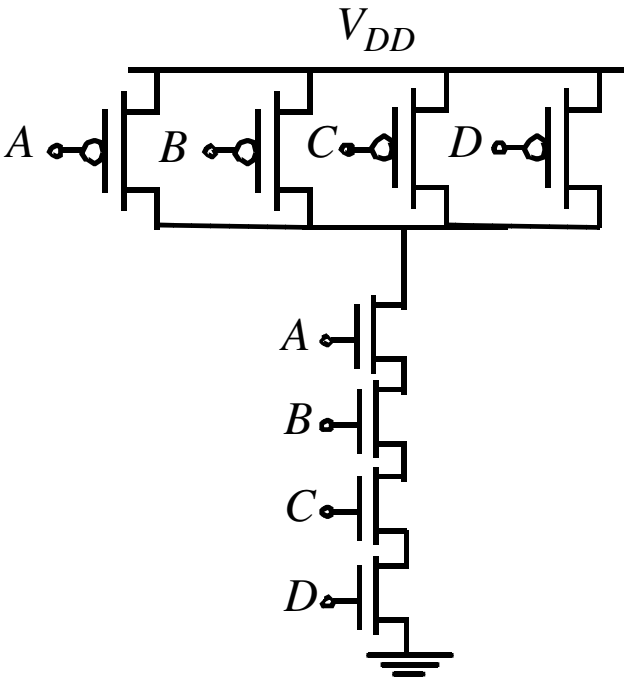
Design for Worst Case





Here it is assumed that $R_p = R_n$

Influence of Fan-In and Fan-Out on Delay



Fan-Out: Number of Gates Connected

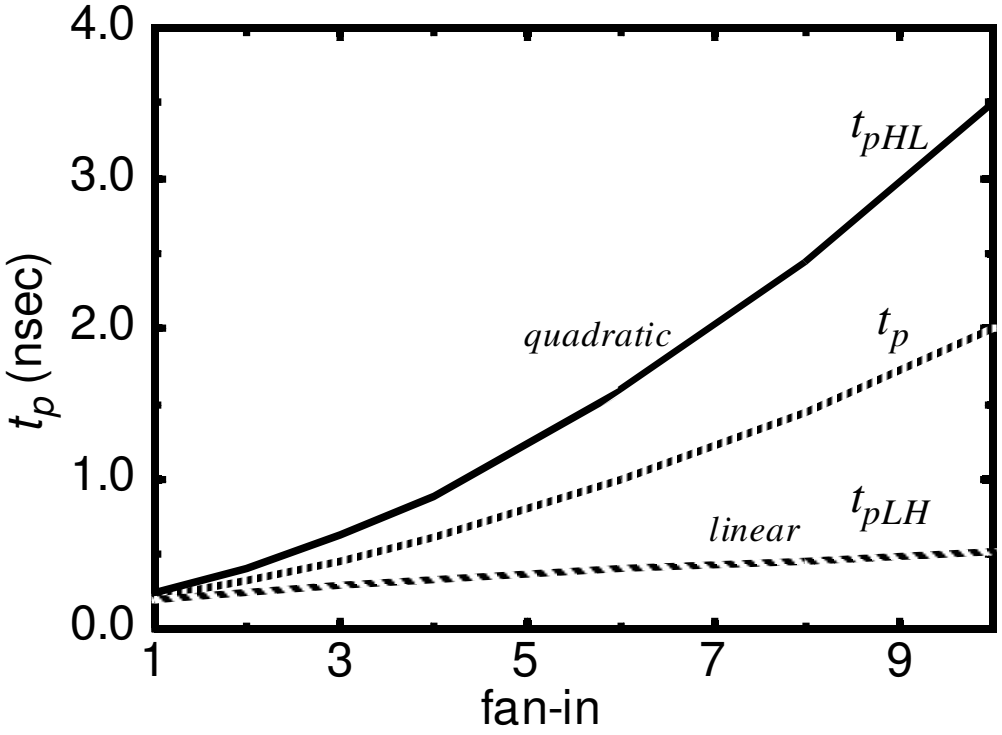
2 Gate Capacitances per Fan-Out

FanIn: Quadratic Term due to:

1. Resistance Increasing
2. Capacitance Increasing
(t_{pHL})

$$t_p = a_1 FI + a_2 FI^2 + a_3 FO$$

t_p as a function of Fan-In



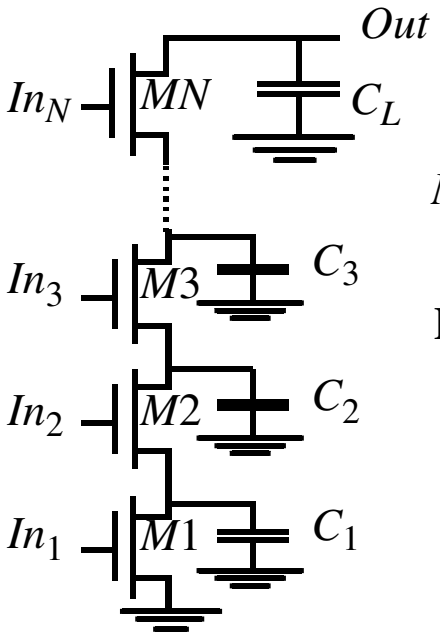
AVOID LARGE FAN-IN GATES! (Typically not more than FI < 4)

Fast Complex Gate - Design Techniques

- **Transistor Sizing:**

  As long as Fan-out Capacitance dominates

- **Progressive Sizing:**



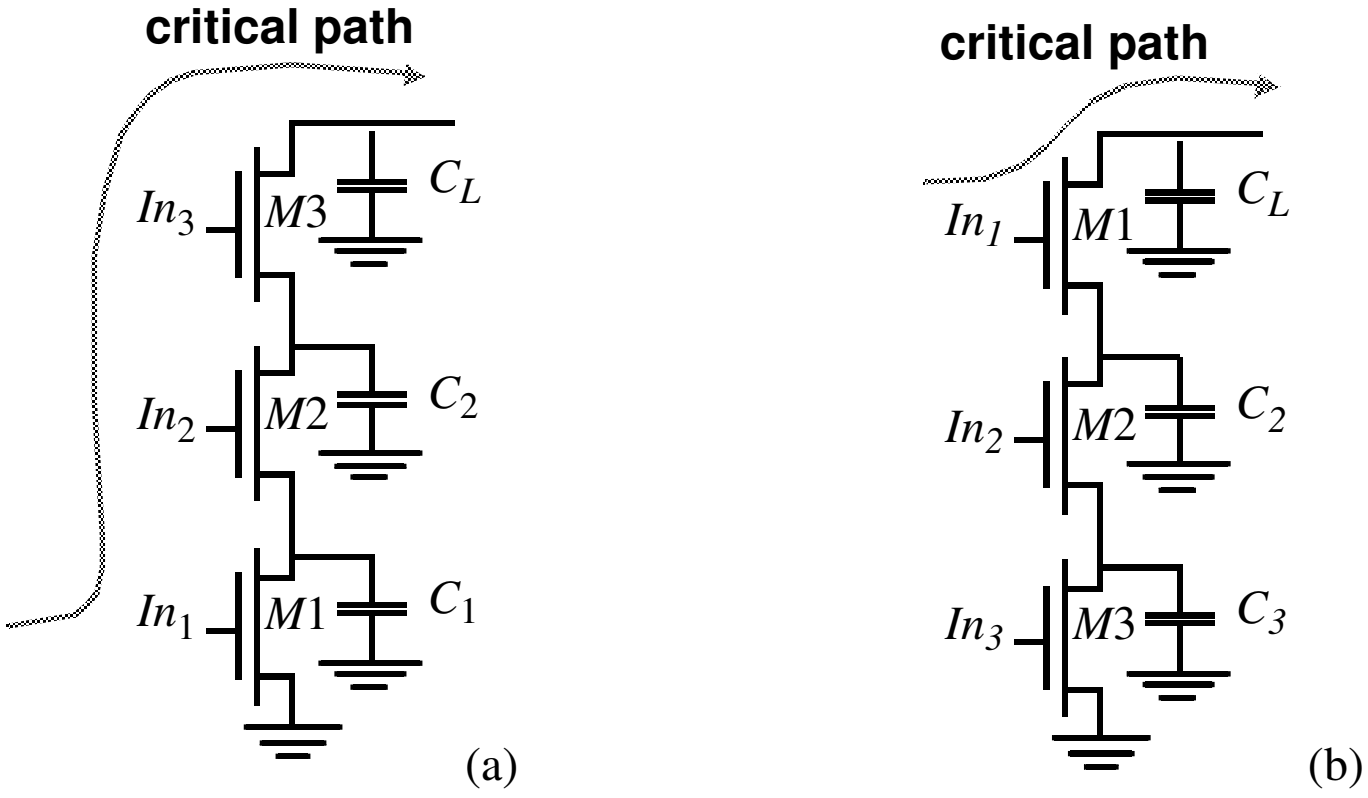
$M1 > M2 > M3 > MN$

Distributed RC-line

Can Reduce Delay with more than 30%!

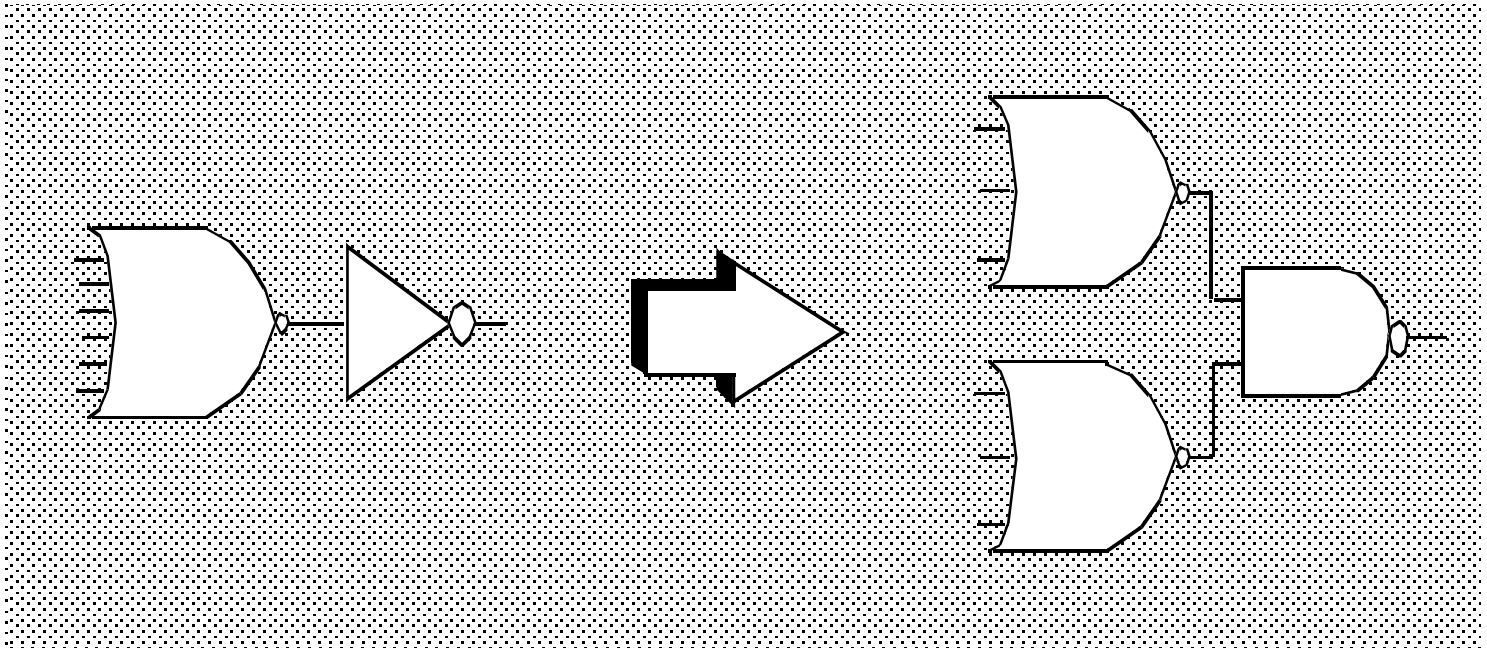
Fast Complex Gate - Design Techniques (2)

- **Transistor Ordering**



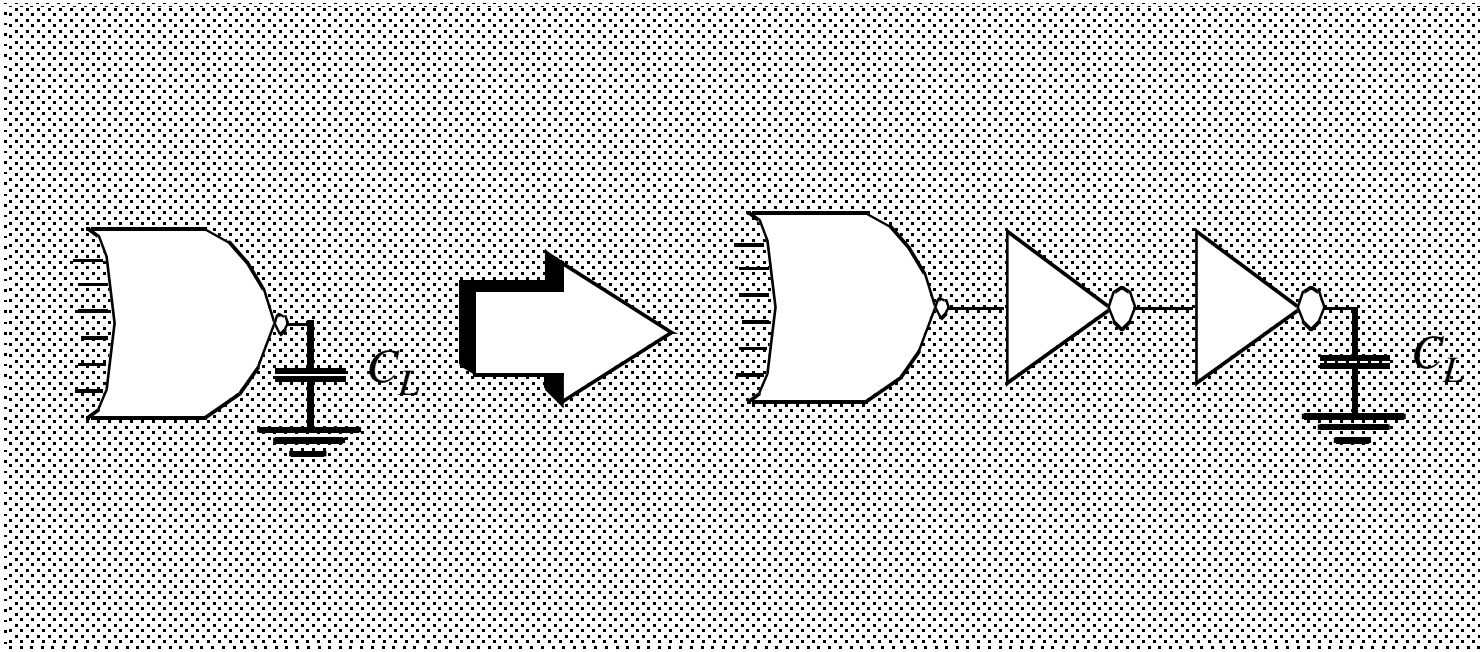
Fast Complex Gate - Design Techniques (3)

- **Improved Logic Design**

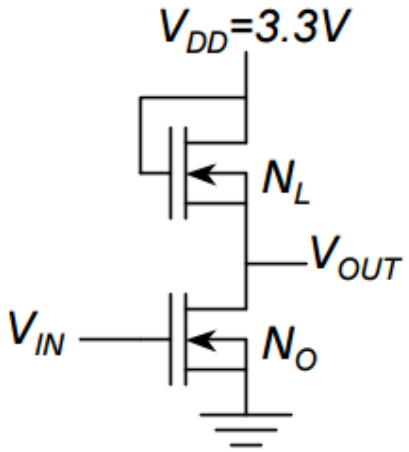


Fast Complex Gate - Design Techniques (4)

- **Buffering: Isolate Fan-in from Fan-out**

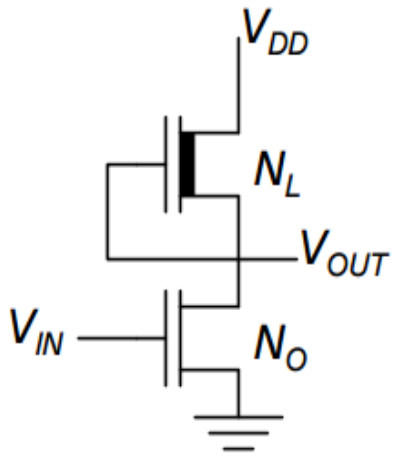


NMOS Inverter w/ Saturated Enhancement Load



- *A MOSFET replaces the resistive load, greatly improving the packing density.*
- *The two MOSFET's are fabricated with identical thresholds and process transconductance parameters, for simplicity and high circuit yield.*
- *The load has a positive threshold and has V_{GS}=V_{DS}; therefore it is always saturated.*
- $V_{OH} = V_{DD} - V_T$.

NMOS Inverter w/ Depletion Type Load



- *For the depletion type device,*

$$V_{GSL} = 0$$

This necessitates $V_{TL} \leq 0$ for conduction in the load. Also, linear or saturated operation of the load is possible:

$$V_{DD} - V_{OUT} > -V_{TL} \Rightarrow \text{saturation}$$
$$V_{DD} - V_{OUT} < -V_{TL} \Rightarrow \text{linear operation}$$

- *This circuit achieves $V_{OH} = V_{DD}$ without the need for two supply voltages.*

- *The disadvantage is fabrication complexity, because transistors with two different threshold voltages are required.*

n-Channel MOSFET connected as saturated load device

- An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter.
- Since the gate and drain of the transistor are connected, we have

$V_{GS}=V_{DS}$

When $V_{GS}=V_{DS}>V_{TN}$, a non zero drain current is induced in the transistor and thus the transistor operates in saturation only. And following condition is satisfied.

$V_{DS}>(V_{GS}-V_{TN})$

$V_{DS}(sat)=(V_{DS}-V_{TN})$ because
$V_{GS}=V_{DS}$ or $V_{DS}(sat)=(V_{GS}-V_{TN})$

In the saturation region the drain current is

$i_D=K_n(V_{GS}-V_{TN})^2=K_n(V_{DS}-V_{TN})^2$

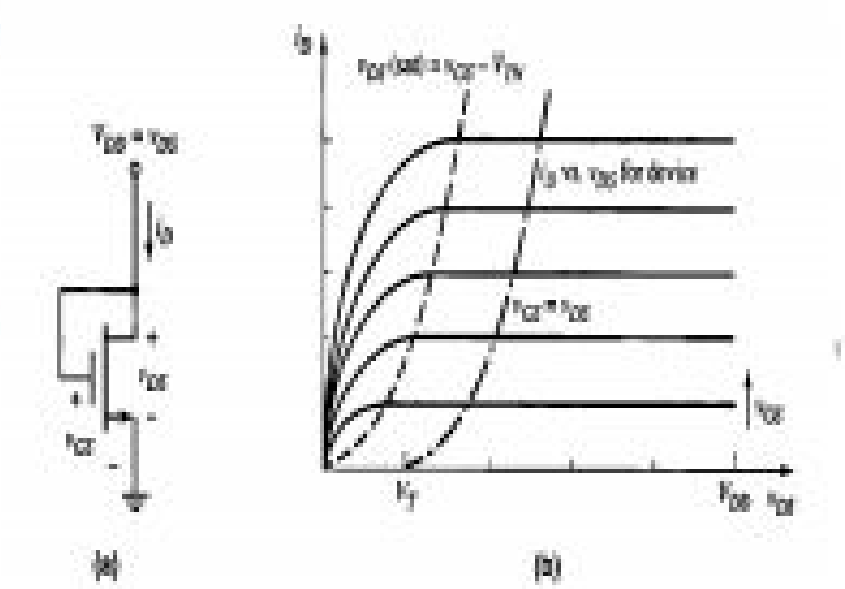
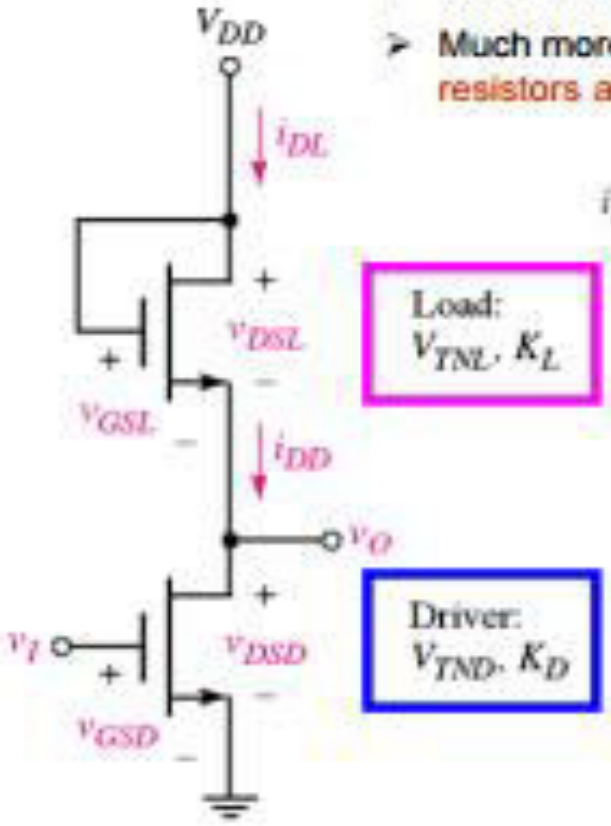


Figure 16.7 (a) n-channel MOSFET connected as saturated load device and (b) current-voltage characteristics of saturated load device

The i_D versus v_{DS} characteristics are shown in Figure 16.7(b), which indicates that this device acts as a nonlinear resistor.

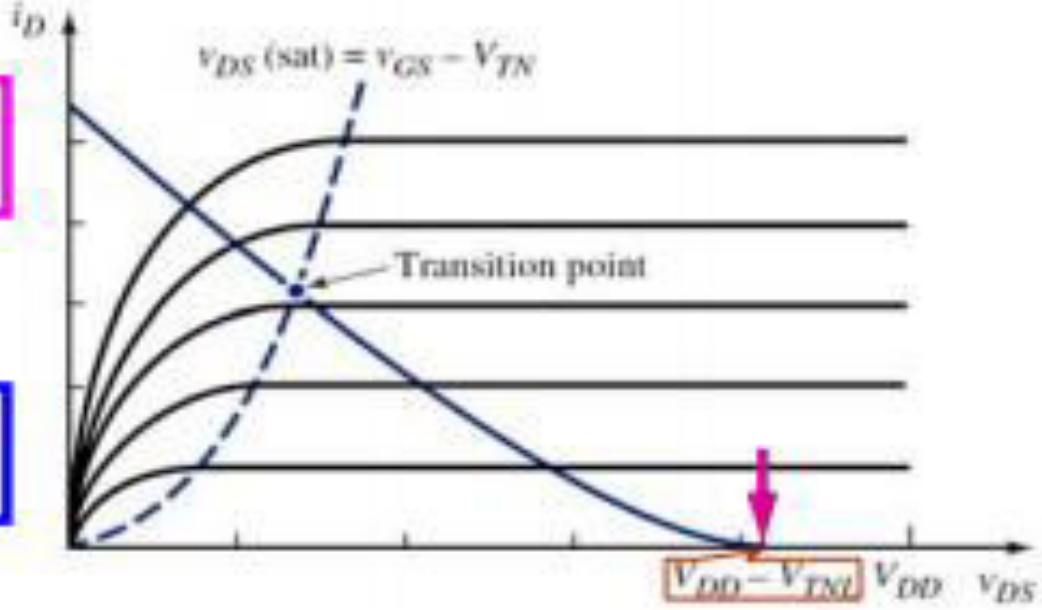
NMOS Inverter with Enhancement Load

- This basic inverter consist of two enhancement-only NMOS transistors
- Much more practical than the resister loaded inverter, because the resistors are thousand of times larger size than a MOSFET.



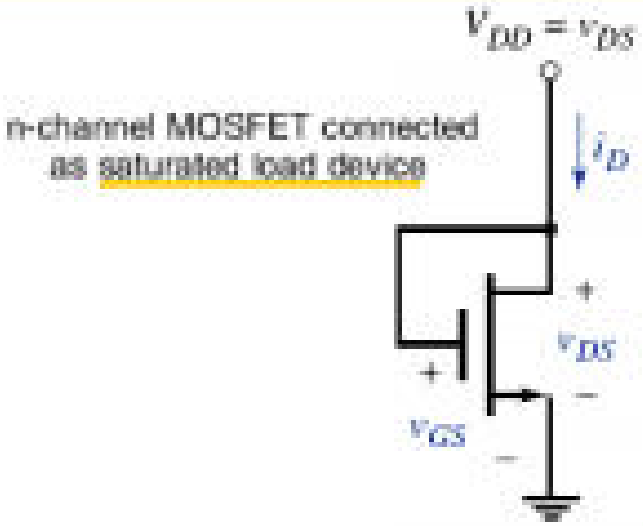
Load:
V_{TNL}, K_L

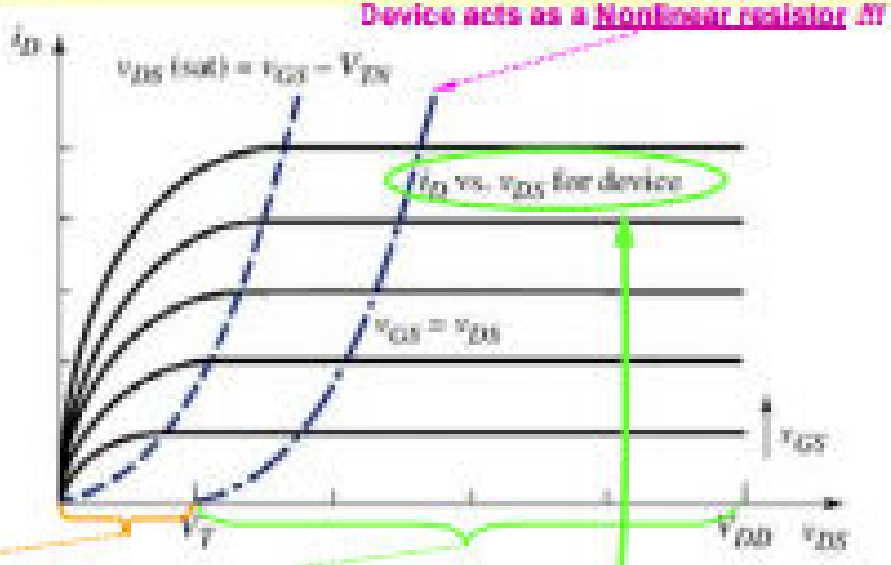
Driver:
V_{TND}, K_D



NMOS Inverter with Enhancement Load

- An n-channel **enhancement-mode MOSFET** with gate connected to the drain can be used as a **load device**.





For $v_{GS} = v_{DS} \leq V_{TN}$, the drain current is zero.

$v_{GS} = v_{DS} > V_{TN}$, a nonzero drain current is induced in the device.

$$v_{DS} > (v_{GS} - V_{TN}) = (v_{DS} - V_{TN}) = v_{DS}(\text{sat})$$

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2$$

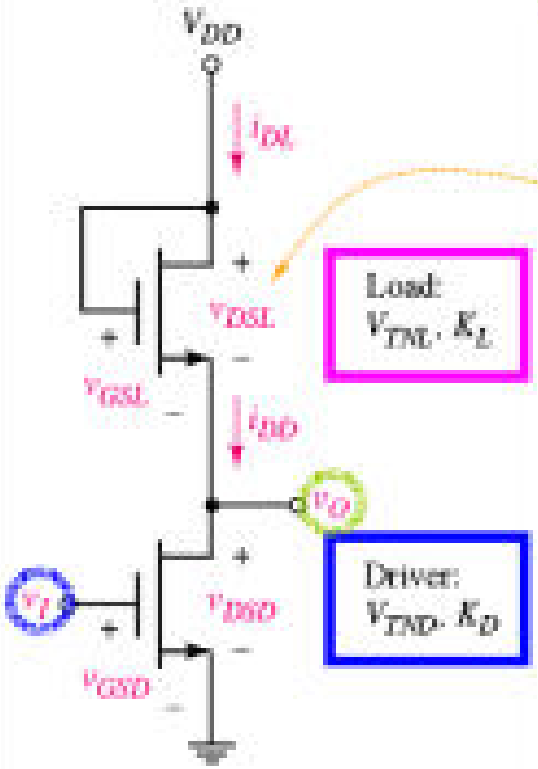
Nonlinear resistor !!!

A transistor with this connection always operates in the saturation region when not in cutoff.

NMOS Inverter with Enhancement Load

When $v_I < V_{TND}$ driver is cut off and the drain currents are zero.

$$i_{DL} = 0 = K_L(v_{DSL} - V_{TNL})^2$$



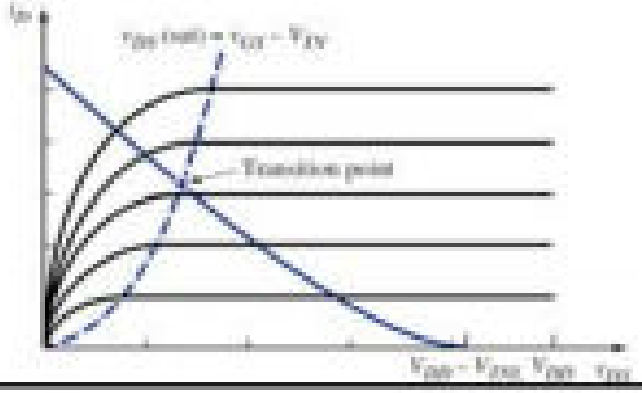
$$v_{DSL} = V_{DD} - v_O$$

$$\rightarrow v_{DSL} - V_{TNL} = V_{DD} - v_O - V_{TNL} = 0$$

maximum output voltage

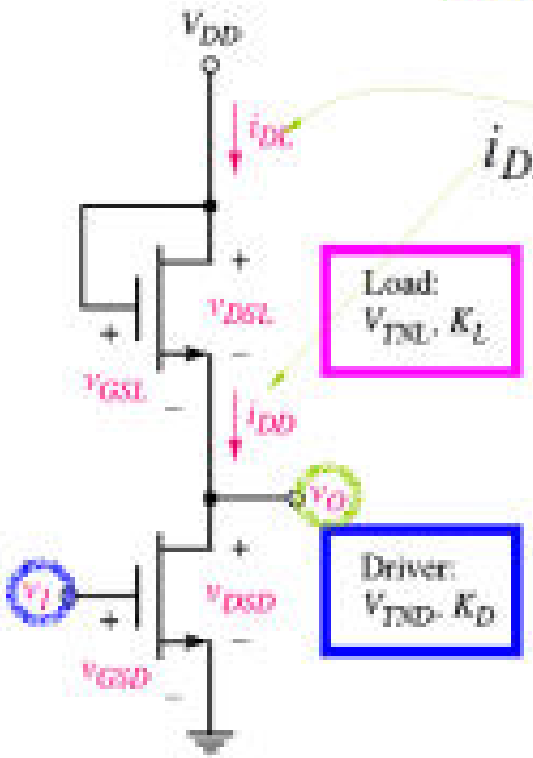
$$v_{O,\max} \equiv V_{OH} = V_{DD} - V_{TNL}$$

For the enhancement-load NMOS inverter, the maximum output voltage, which is the logic 1 level, does not reach the full V_{DD} value.



NMOS Inverter with Enhancement Load

When $v_I > V_{TND}$ driver transistor turns on and is biased in the saturation region.



$$i_{DD} = i_{DL}$$

two drain currents are equal since the output will be connected to the gates of other MOS transistors.

$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$K_D(v_I - V_{TND})^2 = K_L(V_{DD} - v_O - V_{TNL})^2$$

$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

As the input voltage increases, the driver Q-point moves up the load curve and the output voltage decreases linearly with v_I.

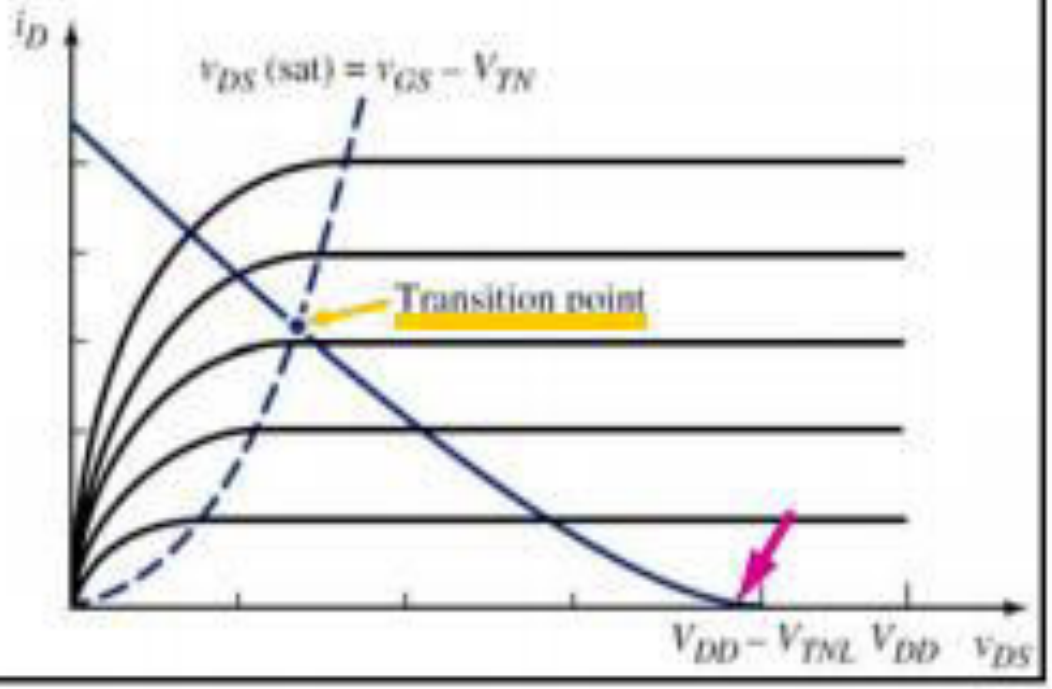
NMOS Inverter with Enhancement Load

At the driver transition point,

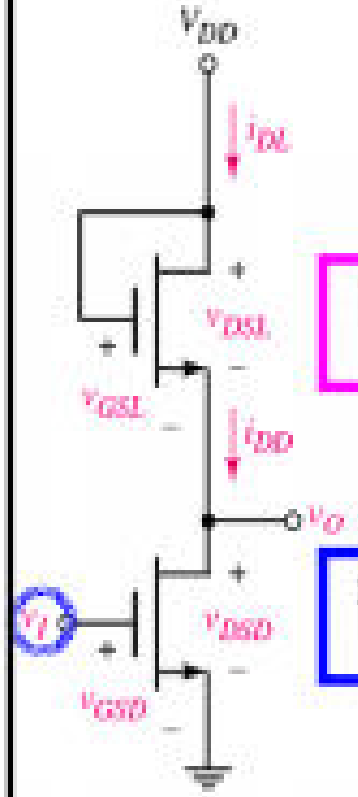
$$v_{DSD}(\text{sat}) = v_{GSD} - V_{TND} \quad \text{or} \quad V_{Ot} = V_{It} - V_{TND}$$

$$v_O = V_{DD} - V_{TNL} - \sqrt{\frac{K_D}{K_L}}(v_I - V_{TND})$$

$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}\left(1 + \sqrt{\frac{K_D}{K_L}}\right)}{1 + \sqrt{\frac{K_D}{K_L}}}$$



NMOS Inverter with Enhancement Load



Load:
V_{TNL}, K_L

Driver:
V_{TND}, K_D

When $v_I > V_{tt}$ the driver transistor Q-point continues to move up the load curve and the driver becomes biased in the nonsaturation region.

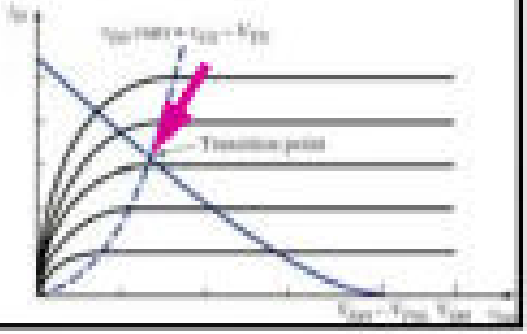
Since $i_{DD} = i_{DL}$,

$$K_D[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2] = K_L(v_{DSL} - V_{TNL})^2$$

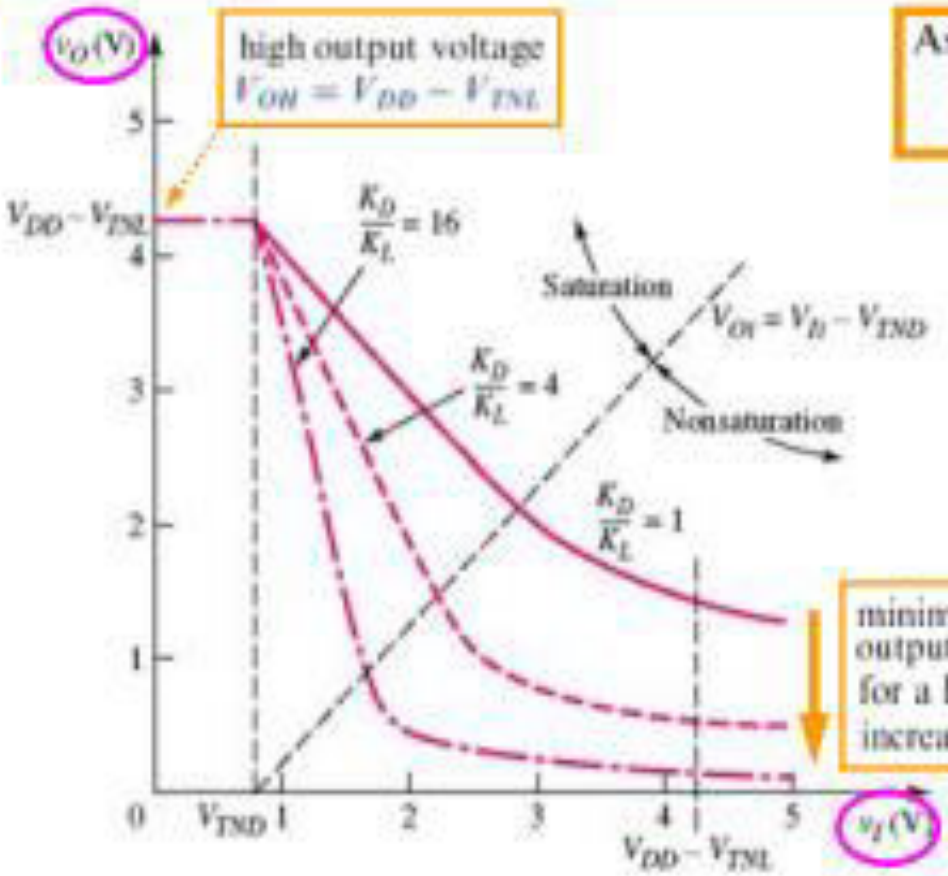
$$K_D[2(v_I - V_{TND})v_O - v_O^2] = K_L(V_{DD} - v_O - V_{TNL})^2$$

the relationship between v_I and v_O in this region is not linear.

K_D/K_L aspect ratio
width-to-length parameters
of the driver and load transistors.



NMOS Inverter with Enhancement Load



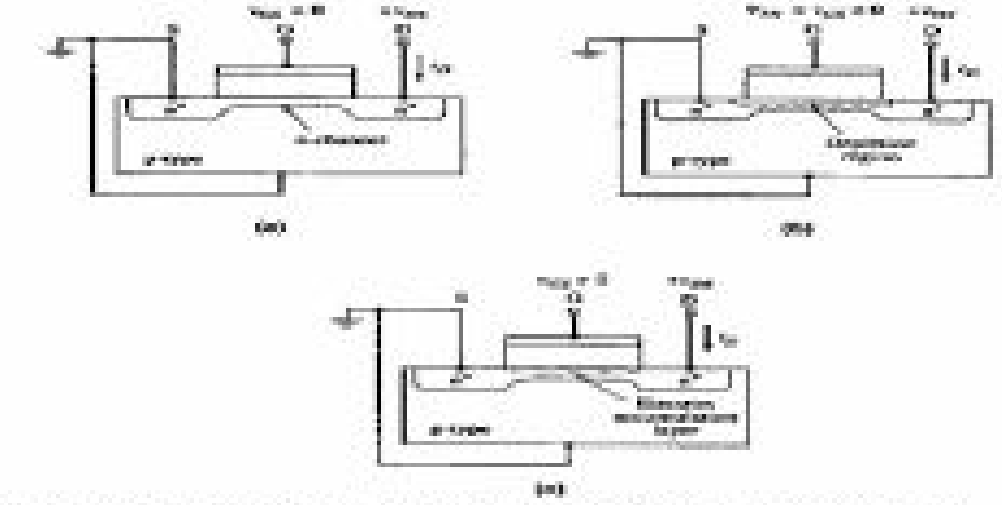
As the width-to-length ratio of the load transistor decreases, the effective resistance increases

minimum output voltage, or the logic 0 level, for a high input decreases with an increasing K_D/K_L ratio.

Voltage transfer characteristics, NMOS inverter with saturated load, for three aspect ratios

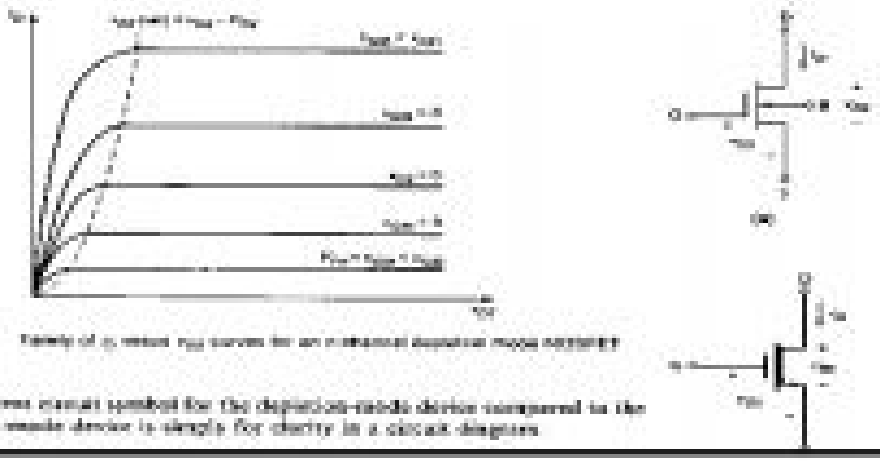
N-Channel Depletion-Mode MOSFET

- In n- channel depletion mode MOSFET, an n-channel region or inversion layer exists under the gate oxide layer even at zero gate voltage and hence term **depletion mode**.

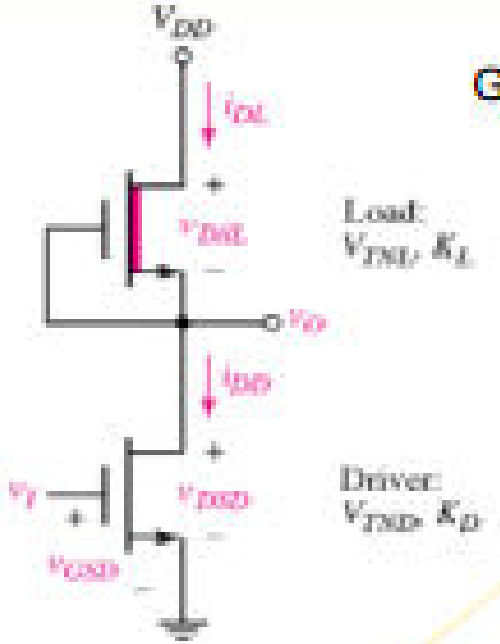


- A negative voltage must be applied to the gate to turn the **device off**.

- The ***threshold voltage*** is always ***negative*** for this kind of device.



NMOS Inverter with Depletion Load

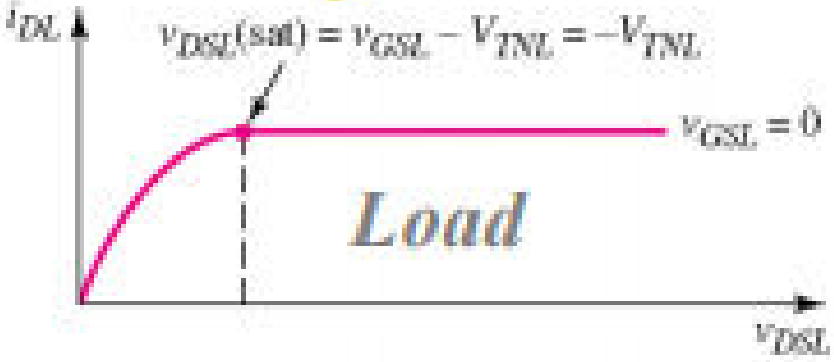


Gate and source are connected, $v_{GSL} = 0$

Since the threshold voltage of load transistor is negative.

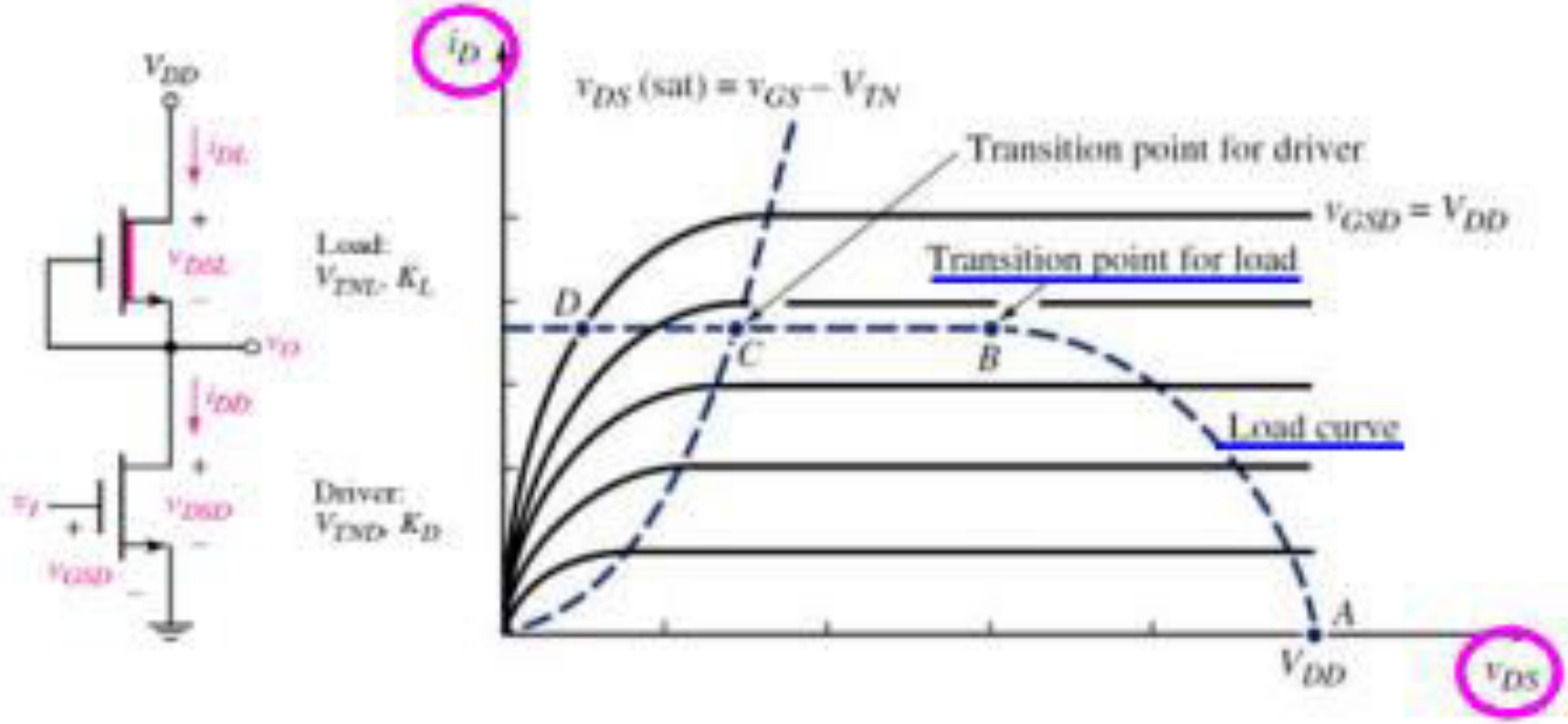
$$v_{DSL}(\text{sat}) = v_{GSL} - V_{TNL} = -V_{TNL}$$

$v_{GSL} = 0$



NMOS Inverter with Depletion Load

driver transistor characteristics and load curve



NMOS Inverter with Depletion Load (cont.)

Case I: when $V_I < V_{TND}$ (drive is cutoff): No drain current conduct in either transistor. That means the load transistor must be in the linear region of the operation and the output current can be expressed as fellows

$$i_{DL}(linear) = K_L[2(V_{GSL} - V_{TNL})V_{DSL} - V_{DSL}^2]$$

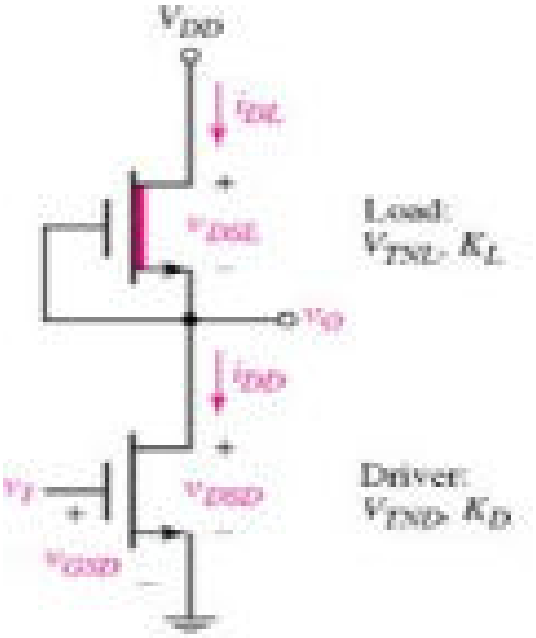
Since $V_{GSL}=0$, and $i_{DL}=0$

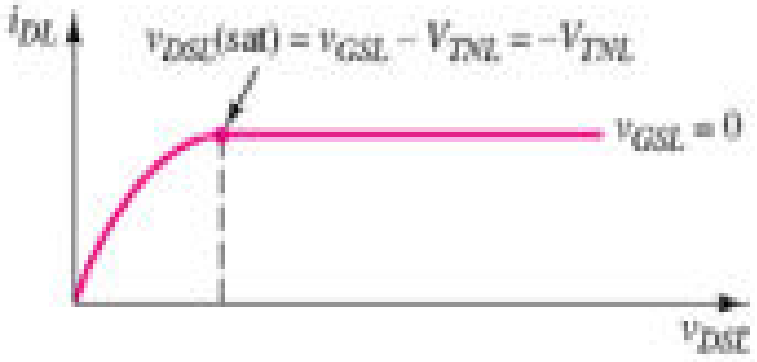
$$0 = -K_L[2V_{TNL}V_{DSL} + V_{DSL}^2]$$

Which gives $V_{DSL}=0$ thus

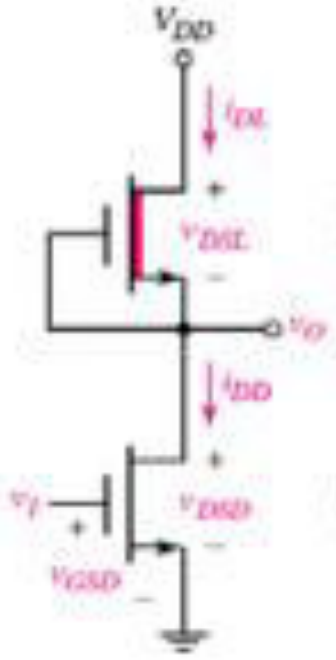
$$V_O = V_{DD}$$

This is the advantage of the depletion load inverter over the enhancement load inverter.





NMOS Inverter with Depletion Load



Load: V_{TNL}, K_L

Driver: V_{TND}, K_D

When $v_I > V_{TND}$ (just greater than)

driver turns on and in the saturation region; however, load is in the nonsaturation region. Q-point lies between points A and B

two drain currents equal, $i_{DD} = i_{DL}$

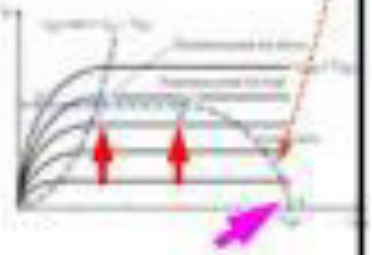
$$K_D[v_{GSD} - V_{TND}]^2 = K_L[2(v_{GSL} - V_{TNL})v_{DSL} - v_{DSL}^2]$$

($v_{GSL} = 0$)

$$K_D[v_I - V_{TND}]^2 = K_L[2(-V_{TNL})(V_{DD} - v_O) - (V_{DD} - v_O)^2]$$

There are two transition points one for the load and one for the driver.

B C

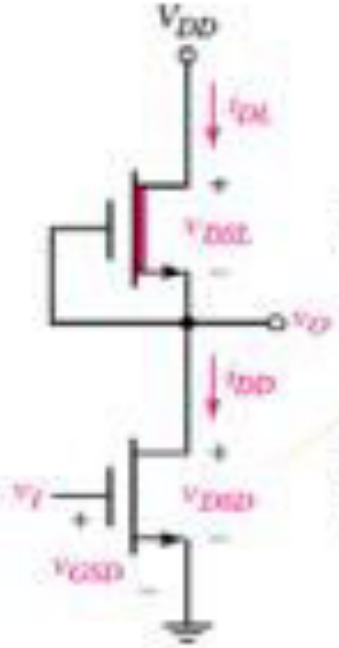


transition point for the load

$$v_{DSL} = V_{DD} - V_{Ot} = v_{GSL} - V_{TNL} = -V_{TNL}$$

$V_{Ot} = V_{DD} + V_{TNL}$ Since V_{TNL} is negative, the output voltage at the transition point is less than V_{DD}.

NMOS Inverter with Depletion Load



transition point for the driver

$v_{DSD} = v_{GSD} - V_{TND}$ $\quad v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

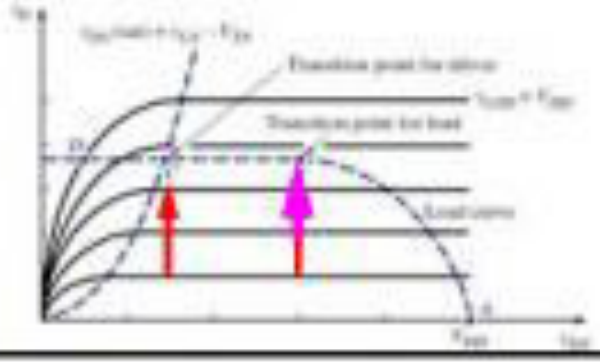
$V_{Ot} = V_{It} - V_{TND}$

When the Q-point lies between points B and C both devices are in the saturation region,

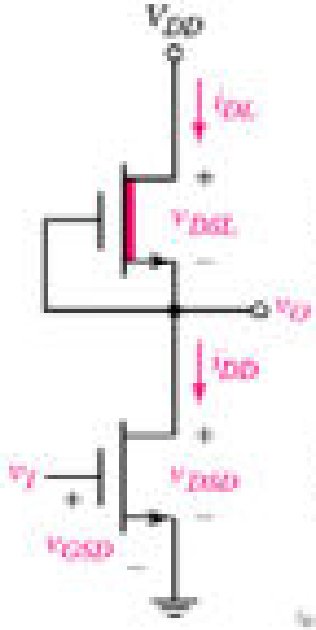
$$K_D(v_{GSD} - V_{TND})^2 = K_L(v_{GSL} - V_{TNL})^2$$

$$\sqrt{\frac{K_D}{K_L}}(v_I - V_{TND}) = -V_{TNL}$$

This implies that input voltage is constant as the Q-point passes this region.



NMOS Inverter with Depletion Load



Load:
V_{TNL}, K_L

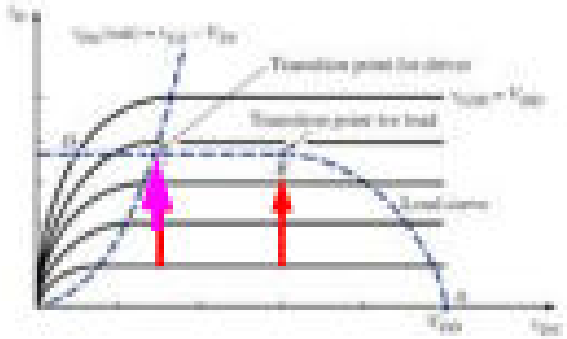
Driver:
V_{TND}, K_D

driver is biased in the nonsaturation region while the load is in the saturation region. Q-point is between points C and D

$$K_D\left[2(v_{GSD} - V_{TND})v_{DSD} - v_{DSD}^2\right] = K_L(v_{GSL} - V_{TNL})^2$$

$$\frac{K_D}{K_L}\left[2(v_I - V_{TND})v_O - v_O^2\right] = (-V_{TNL})^2$$

This implies that input and output voltages are not linear in this region.



NMOS Inverter with Depletion Load

Voltage transfer characteristics,
NMOS inverter with depletion load,