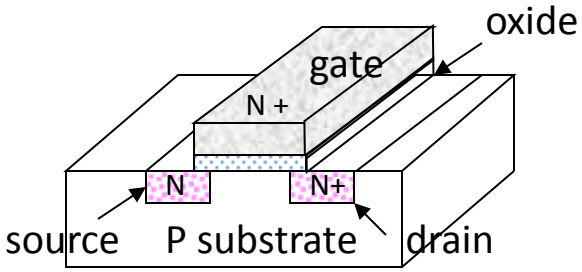
Unit 3
Combinational MOS Logic Circuits

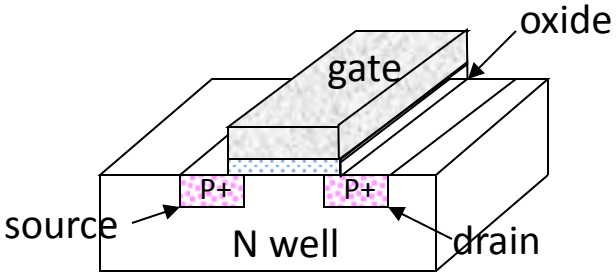
Introduction to CMOS Logic Circuits

- CMOS stands for ***Complementary Metal Oxide Semiconductor***
  - **Complementary**: there are N-type and P-type transistors. N-type transistors use electrons as the current carriers. P-type transistors use holes as the current carriers.
    - Electrons are free carriers in the conduction band with energy of Ec or just above the conduction band edge. Free electrons are generated by doping the silicon with an N-type impurity such as phosphorous or arsenic.
    - A hole is a current carrier due to the absence of an electron in a covalent bond state, i.e. a missing electron which would otherwise be part of a silicon-to-silicon bond. Holes are free carriers in the valence band with energy of Ev or just below the valence band edge. Holes are generated by doping the silicon with a P-type impurity such as boron.
  - **Metal**: the gate of the transistor was made of aluminum metal in the early days, but is made of polysilicon today (for the past 25 years or more).
  - **Oxide**: silicon dioxide is the material between the gate and the channel
  - **Semiconductor**: the semiconductor material is silicon, a type IV element in the periodic chart. Each silicon atom bonds to four other silicon atoms in a tetrahedral crystal structure.

CMOS NFET and PFET Transistors



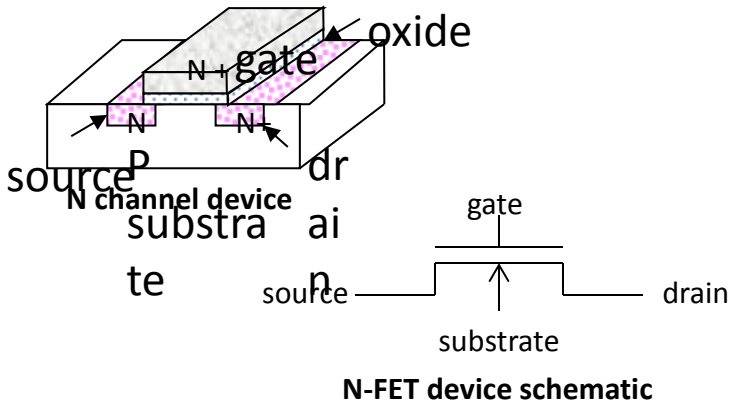
N channel device



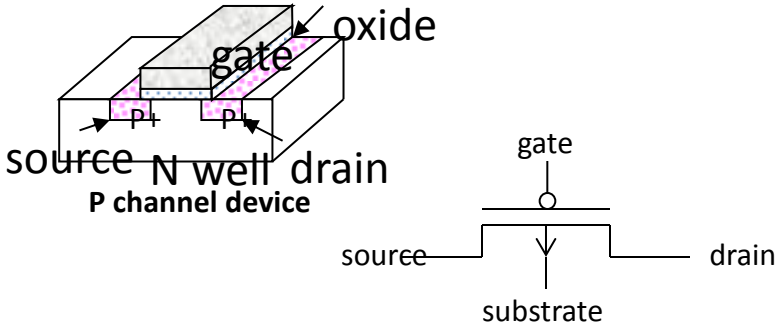
P channel device

- N channel device: built directly in the P substrate with N-doped source and drain junctions and normally N-doped gate conductor
  - Requires positive voltage applied to gate and drain (with respect to source) for electrons to flow from source to drain (thought of as positive drain current)
- P channel device: built in an N-well (a deep N-type junction diffused into the P substrate) with P-doped source and drain junctions and N or P-doped gate
  - Requires negative voltage applied to gate and drain (with respect to source) for electrons to flow from drain to source (thought of as negative drain current)

N-FET and P-FET Devices as Switches



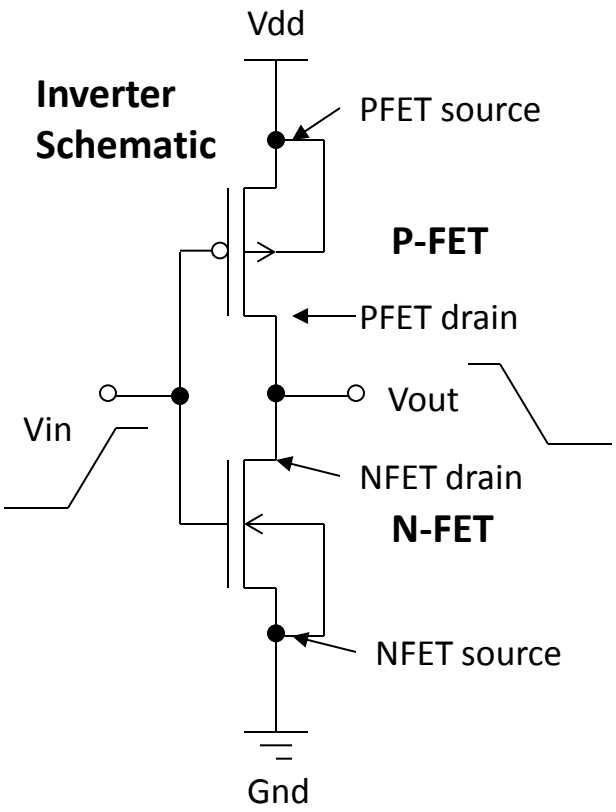
N-FET device schematic

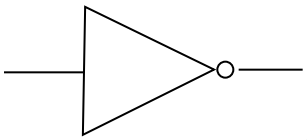


P-FET device schematic

- NFET Device:
  - positive voltage (“1” or high) on gate relative to source turns device ON and allows positive current to flow from drain to source (switch closed)
  - zero volts on gate (“0” or low) turns device OFF (open circuit)
  - Source (vs drain) is the most negative terminal
- PFET Device:
  - Negative voltage (“0” or low) on gate relative to source turns device ON and allows (negative) current to flow from drain to source (closes switch)
  - Zero volts on gate relative to source (“1” or high) turns device OFF (closes switch)
  - source (vs drain) is the most positive terminal

Simple CMOS Circuits: ***The Inverter Gate***



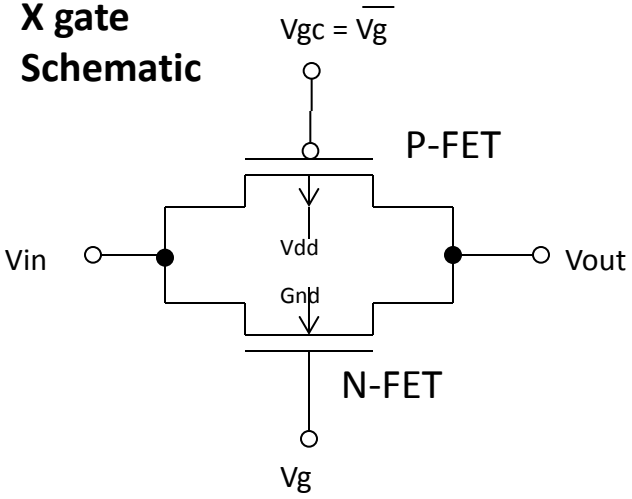


Inverter Symbol

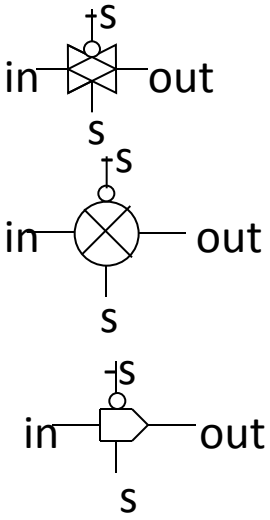
- The simplest complementary MOS (CMOS) circuit is the inverter:
  - NFET & PFET gates are connected together as the input
  - NFET & PFET drains are connected together as the output
  - NFET & PFET sources are connected to Gnd and Vdd, respectively.
  - NFET substrate is normally connected to Gnd for all NFET devices in the circuit
  - PFET well is normally connected to Vdd (most positive voltage in circuit) for all PFET devices
- Operation:
  - If Vin is down (0 volts), NFET is OFF and PFET is ON pulling Vout to Vdd (high = 1)
  - If Vin is up (at Vdd), NFET is ON hard and PFET is OFF pulling Vout low to Gnd (“0”)
  - With Vin at 0 or Vdd, no dc current flows in inverter

Simple CMOS Circuits: *The Transmission Gate*

X gate Schematic

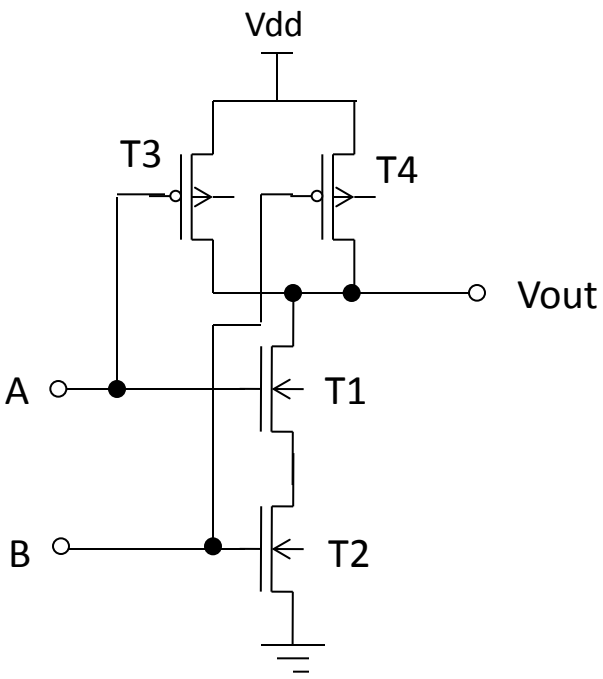


X-gate Symbols

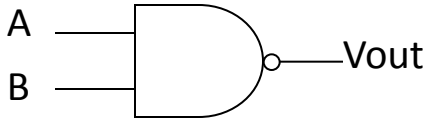


- Circuit topology:
  - N and P devices with sources and drains connected in parallel.
  - Vg is the control signal for the N device; Vgc (complement of Vg) is the control signal for the P device.
- Operation:
  - When Vg is high (at Vdd) and Vgc is therefore low (at Gnd), the NFET and PFET are both ON. (Depending upon the devices' source potentials, one may be ON more strongly than the other.) The switch is therefore CLOSED and Vout will be the same logic level as Vin.
  - When Vg is low (at Gnd) and Vgc is high (at Vdd), both devices are OFF. The switch is therefore OPEN and Vout will be independent of Vin (high Z connection).

Simple CMOS Circuits: ***2-way NAND***

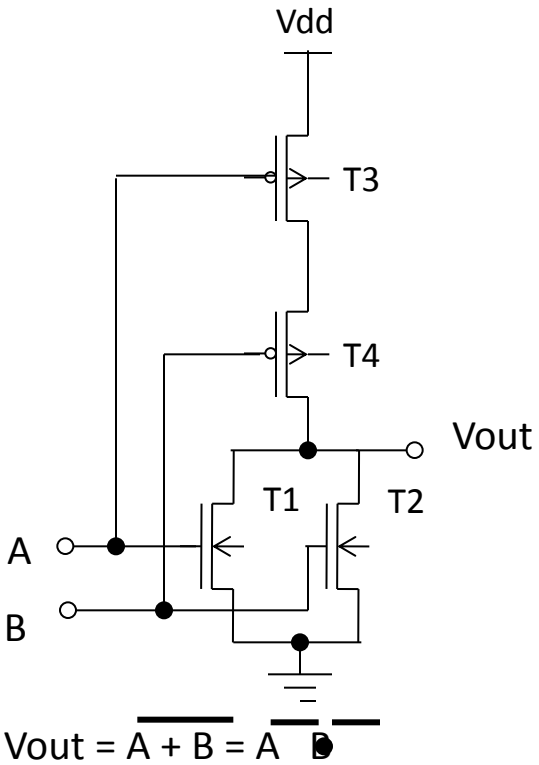


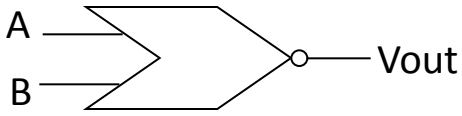
$$Vout = \overline{A \cdot B} = \overline{A} + \overline{B}$$



- Circuit Topology:
  - T1 and T2 are N-FET devices connected in series; T3 and T4 are P-FET devices connected in parallel with their sources at Vdd and their drains at Vout.
  - Inputs A and B are connected to the gates of T1 & T3 and T2 & T4, respectively.
  - T2, T3, & T4 operate as "grounded source" devices, but T1 has its source generally above Gnd potential.
- Operation:
  - If both A and B are high (at Vdd), both T1 and T2 are ON hard, therefore pulling Vout low (to zero volts). Both T3 and T4 are OFF due to their gate-to-source voltages (Vgs) being at 0 volts, thus preventing any dc current.
  - If either A or B (or both) are low (at 0 volts), either T1 or T2 (or both) are OFF; T3 or T4 (or both) are ON hard, thus pulling Vout high to Vdd (a "1" output).

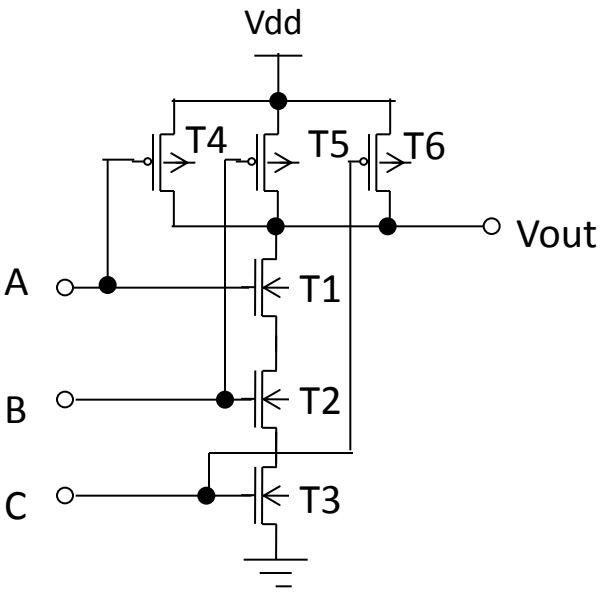
Simple CMOS Circuits: ***2-way NOR***



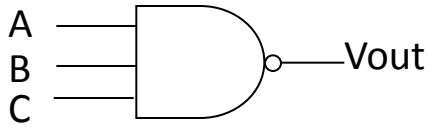


- Circuit Topology:
  - T1 and T2 are N-FET devices connected in parallel with their sources at Gnd and drains at Vout; T3 and T4 are P-FET devices connected in series.
  - Inputs A and B are connected to the gates of T1 & T3 and T2 & T4, respectively.
- Operation:
  - If either A or B is high, T1 and/or T2 are ON hard and either T3 or T4 (or both) are OFF, pulling Vout to gnd. No dc current flows.
  - If both A and B are low (at gnd), both T1 and T2 are OFF and both T3 and T4 are ON hard, thus pulling Vout to Vdd (a “1” output).
  - T1, T2, and T3 operate as common source, but T4’s source potential will drop below Vdd.

Simple CMOS Circuits: ***3-way NAND***

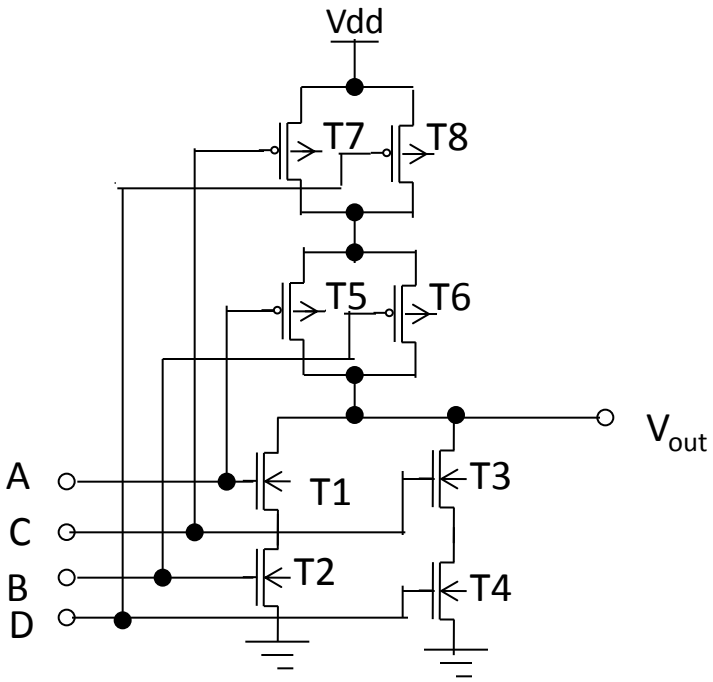


$$Vout = \overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$

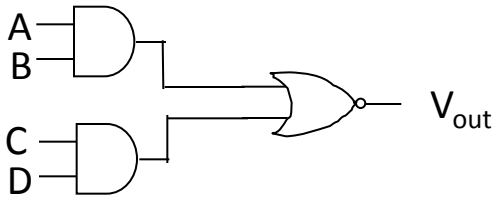


- Circuit Topology:
  - T1,T2,T3 are N-FET devices in series; T4,T5,T6 are P-FET devices in parallel with sources to Vdd.
  - T3, T4, T5, & T6 all operate as grounded source mode; T1 & T2 will have their source potentials above gnd over portions of the switching transient, or if T3 is OFF
- Circuit Operation:
  - If all of T1, T2, & T3 are ON (A, B, & C all high), Vout is pulled low; T4, T5, & T6 are all OFF thus preventing any dc current flow.
  - If one (or more) of A, B, or C are low, then the corresponding P device T4, T5, and/or T6 is ON hard and Vout is pulled high; at the same time one or more of T1, T2, and/or T3 is OFF preventing any dc current flow.

Simple CMOS Circuits: ***Compound Logic***



$$V_{out} = \overline{(A \bullet B) + (C \bullet D)}$$

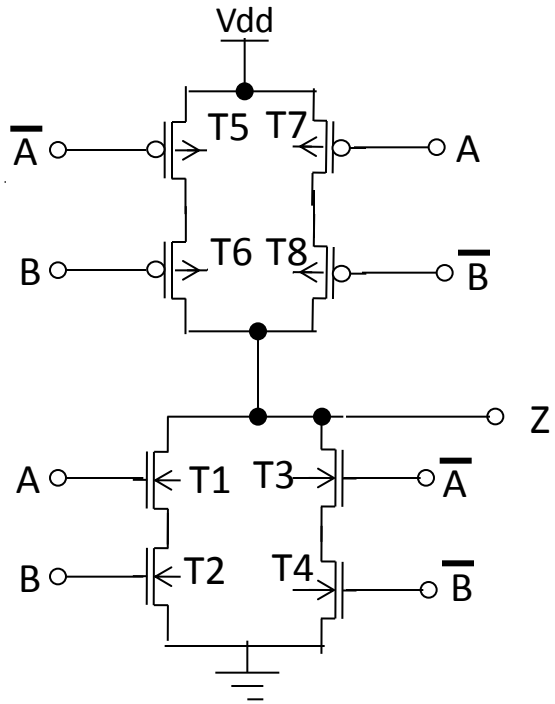


- Circuit Schematic:
  - T1–T4 form a parallel combination of series-connected NFET's; T5-T8 are a series combination of parallel-connected PFET's.
  - T2, T4, T7 & T8 operate as grounded-source devices; T1, T3, T5 & T6 all have their drain's tied together as V_{out}.
  - Note that the P device combination is arranged complementary to the N device combination!
- Operation:
  - If either A and B or C and D are high, NFET devices T1 and T2 or T3 and T4 are ON and pull V_{out} down to ground potential (0 volts). No dc current flows.
  - If either A and C, or A and D, or B and C, or B and D are low, PFET devices T5 and T7, or T5 and T8, or T6 and T7, or T6 and T8 will be ON and pull Vout high to Vdd. No dc current flows.

Simple CMOS Logic Circuits: ***Construction Algorithm***

- Design the N-FET logic combination to pull the output down to zero, i.e. for all the min-terms in truth table with “0”s in the output column.
  - N devices are ON when the truth table inputs corresponding to their respective gate electrodes are “1”s; conversely, any truth table inputs that are zero imply that the corresponding N devices for those inputs are OFF.
- Design the P-FET logic combination to pull output high to VDD, i.e. to cover all min-terms in truth table with “1”s in the output column.
  - P devices are ON when the truth table inputs corresponding to their respective gates are “0”s; conversely, P devices are OFF if the voltages on their respective gates are at the “1” level.
- Start with N pull down logic and P pull up logic which are complementary to each other.
- Then, look for ways to simplify the logic combinations by removing devices having redundant paths.

Simple CMOS Logic Circuits: ***XOR***



$$Z = (A\,\overline{B}) + (\overline{A}\,B)$$

$$= \overline{(A\,\overline{B})\;(\overline{A}\,B)}$$

$$= \overline{(\overline{A} + B)\;(A + \overline{B})}$$

$$= \overline{(A\,\overline{B})} + \overline{(\overline{A}\,B)}$$

- Circuit Schematic:
  - 4 NFET's (T1-T4) and 4 PFET's (T5-T8) are constructed as four parallel sections of two series devices each.
  - Each series connection implements a min-term in the truth table – two for Z=1 and two for Z=0.
  - Could implement either tree first and then apply complement procedure, or use DeMorgan's theorem to implement each min-term of truth table directly.
- Operation:
  - Output is pulled high to VDD by either A=1 and B=0 (turning on T5 and T6), or by A=0 and B=1 (turning on T7 and T8).
    - Implements the "1" min-terms
  - Output is pulled low to ground by either A=1 and B=1 (turning on T1 and T2), or by A=0 and B=0 (turning on T3 and T4).
    - Implements the "0" min-terms

Simple CMOS Logic Circuits: ***Examples from 1.5.5***

In Class Exercise: Work out the following examples from the text.

Design CMOS logic functions for the following gates:

(1-c) $Z = \overline{(A\ B\ C) + D}$

(1-d) $Z = \overline{((A\ B) + C)\ D}$

(1-e) $Z = \overline{(A\ B) + C\ (A + B)}$

Use a combination of CMOS gates to generate the following functions:

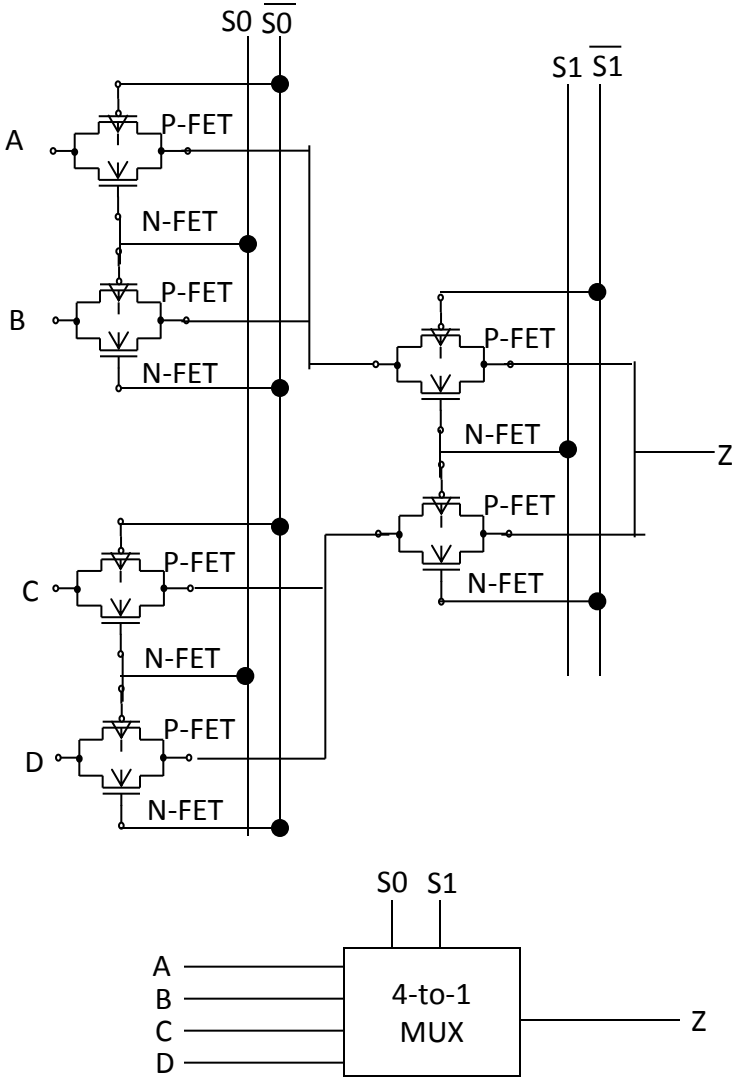
(2-a) $Z = A$ (this is a buffer)

(2-b) $Z = A\ \overline{B} + \overline{A}\ B$ (XOR)

(2-c) $Z = A\ B + \overline{A}\ \overline{B}$ (XNOR)

(2-d) $Z = A\ \overline{B}\ \overline{C} + \overline{A}\ \overline{B}\ C + \overline{A}\ B\ \overline{C} + A\ B\ C$ which is the sum function in the binary adder.

Simple CMOS Logic Circuits: ***The Multiplexer***



- Multiplexers can be implemented with standard CMOS logic gates or with CMOS transmission gates or with a combination of both.!
  - With CMOS gates, a 2-to-1 multiplexer requires 3 gates (2 AND's & 1 OR) having 12 Tx's (plus inverter for select)
  - With Xmission gates, a 2-to-1 multiplexer requires only 4 Tx's (plus inverter for the select)
- 4-to-1 multiplexer shown at right:
  - Using Xmission gates, 12 Tx's (plus 2 inverters for selects)
  - Using CMOS logic, it requires four 3-input AND gates plus one 4-input OR gate for a total of 32 Tx's (plus 2 inverters for the selects)

VLSI Circuit/System Representations

- Design of a digital system may be represented by several different design domains (Behavioral, Structural, and Physical) and within each domain various levels of abstraction (Architectural, Logic, Circuit, Transistor)
  - Behavioral Domain: specifies what the system does
    - Ex: Applications … Operating System … Program … Subroutine … Instruction
  - Structural Domain: specifies how the entities are connected & organized
    - Ex: PC … Processor … Gates & Registers … Transistors
  - Physical Domain: specifies how to build the structure
    - Ex: Box …. Board/Card … Modules … Chips …. Cells … Transistors … Process/Masks

VLSI Circuit/System Representations: ***Behavioral***

- Describes how the particular system, chip, or macro should respond to a set of inputs
- May be specified by:
  - Boolean equations
  - Truth tables
  - Algorithms written in standard high level computer languages (e.g. RTL)
  - Special HDL's (Hardware Description Language) such as VHDL and Verilog
- Example in text from adder implementation
  - Sum and carry functions

VLSI Circuit/System Representations: ***Structural***

- Specifies how components are organized and interconnected to perform the given function
- Levels of specification: (use adder example)
  - Functional block: build a 4 bit adder out of 1 bit adders
  - Module add: specify a 1 bit adder with sum and carry functions
  - Logic level: specify the adder or carry as logic functions
  - Circuit level: specify the circuit as interconnected NMOS and PMOS transistors (CMOS circuit)
    - A full description at the circuit level would be a ***SPICE*** representation which lists the transistor types, transistor interconnections, transistor sizes, junction capacitances, wire capacitances, resistances, etc. for a full circuit performance simulation

VLSI Circuit/System Representations: ***Physical***

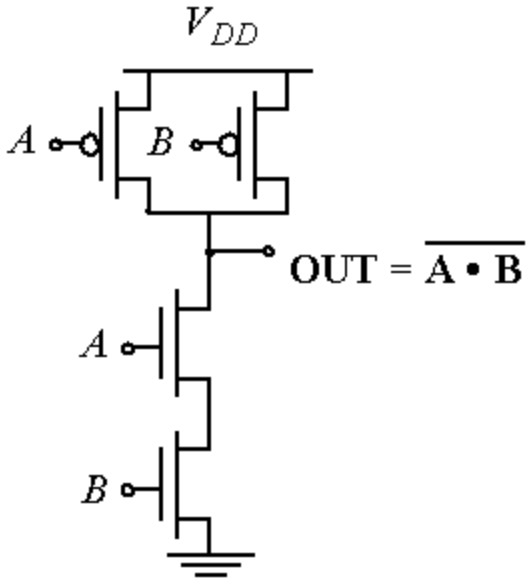
- Specifies how to construct (fabricate) the particular chip or system
- Levels of specification:
  - Process description
  - Photo mask image information for building transistors
  - Recipes for building modules, cards, boards, etc.

Complex Logic Circuits

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B $\Rightarrow$ Conduction to GND

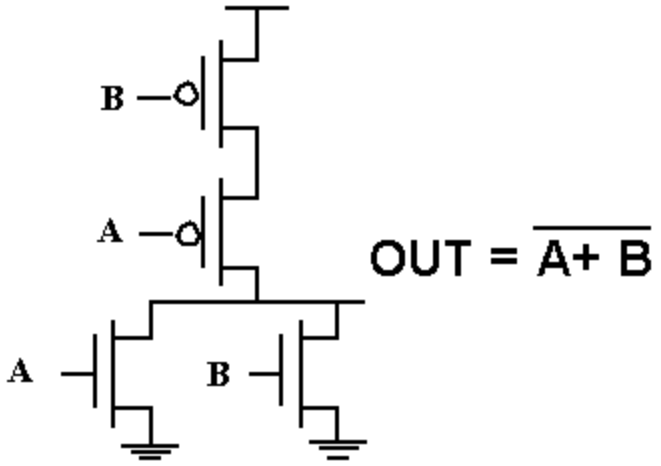
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

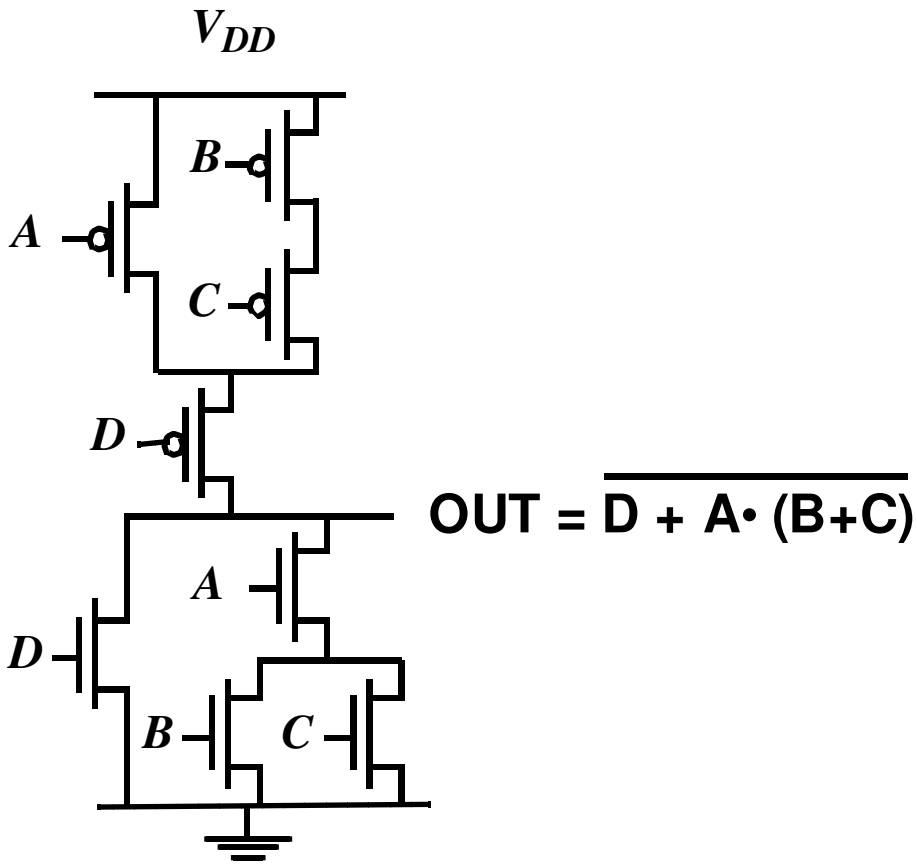
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



Example Gate: COMPLEX CMOS GATE



Properties of Complementary CMOS Gates

***High noise margins*:**

V_{OH} and V_{OL} are at V_{DD} and *GND*, respectively.

***No static power consumption*:**

There never exists a direct path between V_{DD} and V_{SS} (*GND*) in steady-state mode.

Comparable rise and fall times:

(under the appropriate scaling conditions)

Properties of Complementary CMOS Gates

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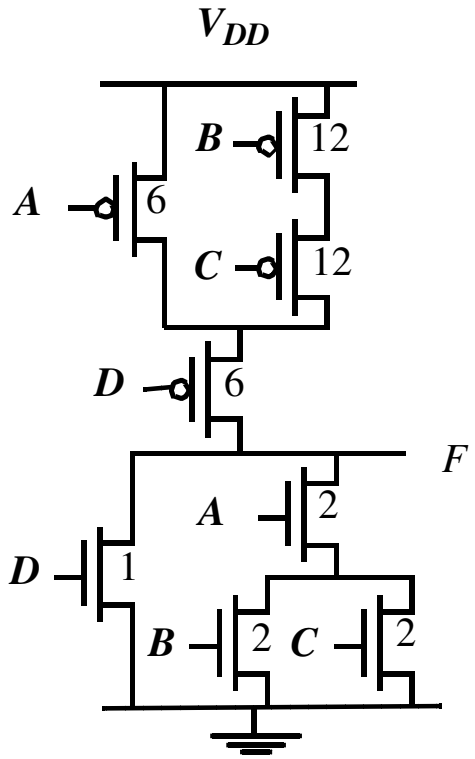
Transistor Sizing

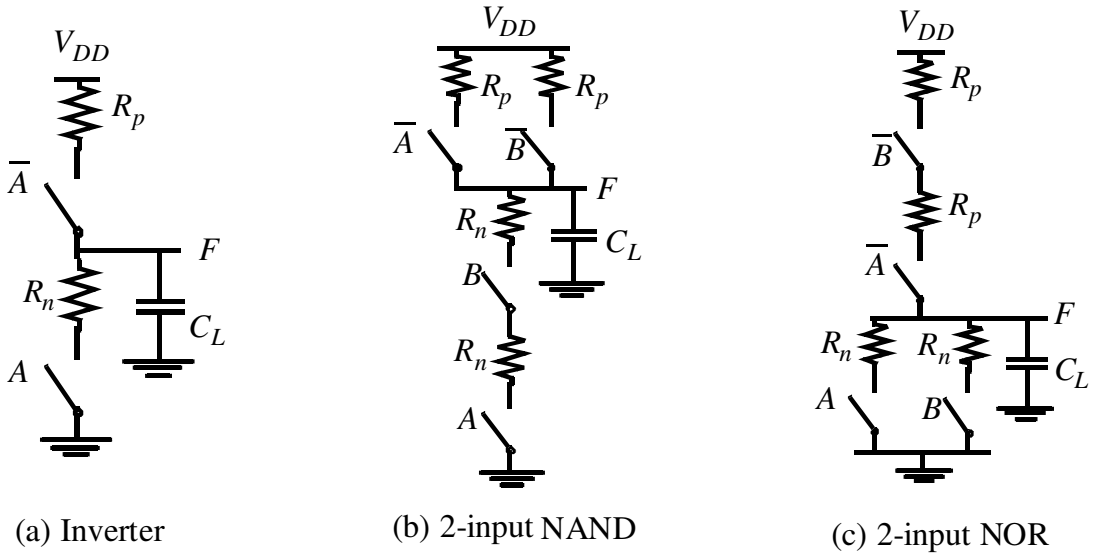
- **for symmetrical response (dc, ac)**
- **for performance**



Input Dependent

Focus on worst-case

Propagation Delay Analysis - The Switch Model



(a) Inverter (b) 2-input NAND (c) 2-input NOR

$$\mathbf{t_p = 0.69\ R_{on}\ C_L}$$

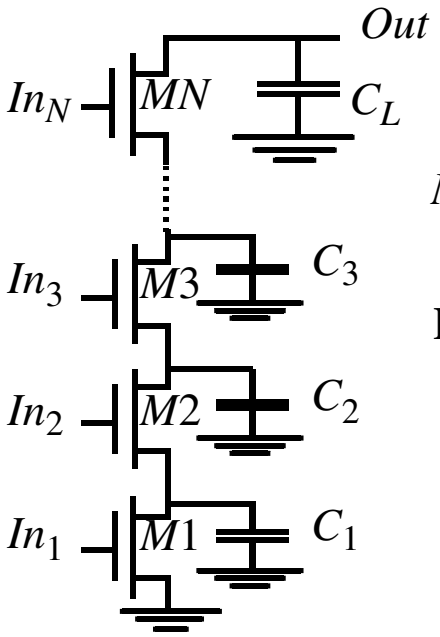
(assuming that $\mathbf{C_L}$ dominates!)

Fast Complex Gate - Design Techniques

- **Transistor Sizing:**

  As long as Fan-out Capacitance dominates

- **Progressive Sizing:**



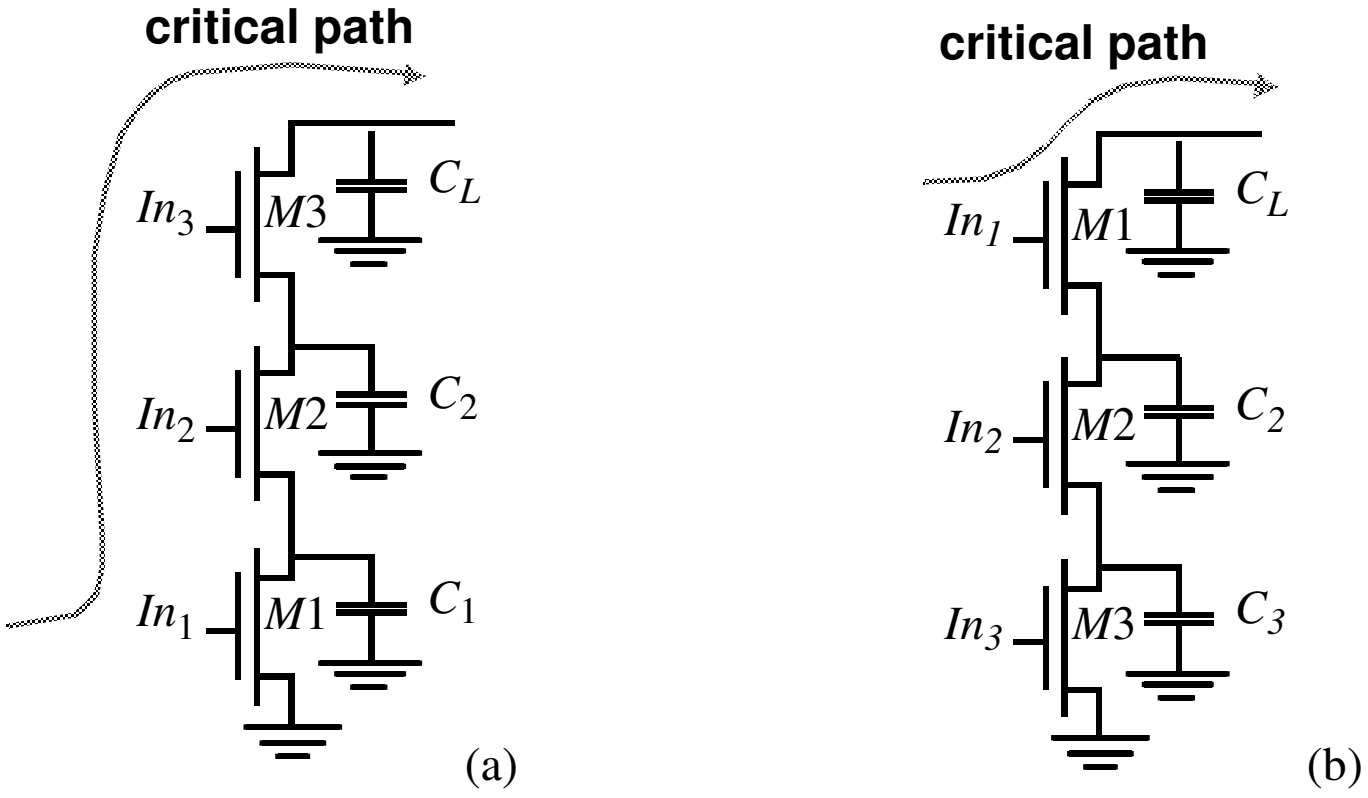
$M1 > M2 > M3 > MN$

Distributed RC-line

Can Reduce Delay with more than 30%!

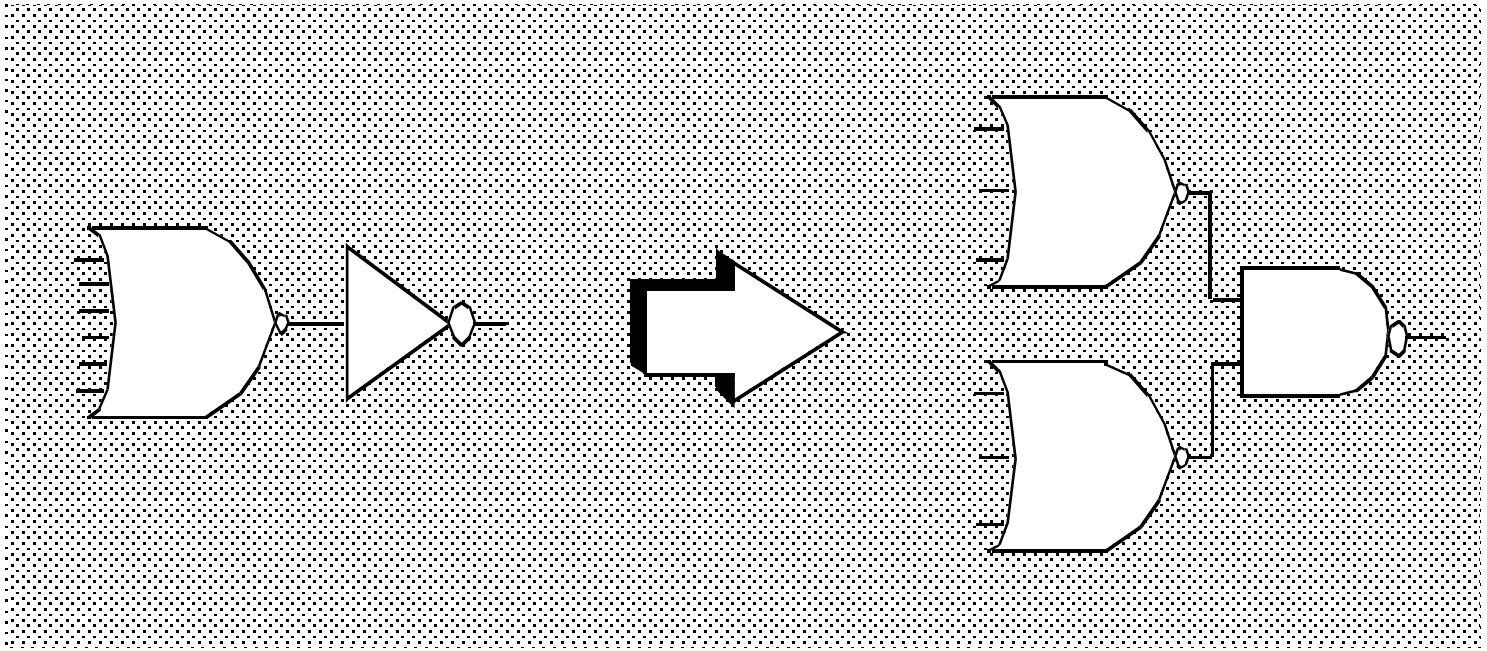
Fast Complex Gate - Design Techniques (2)

- **Transistor Ordering**



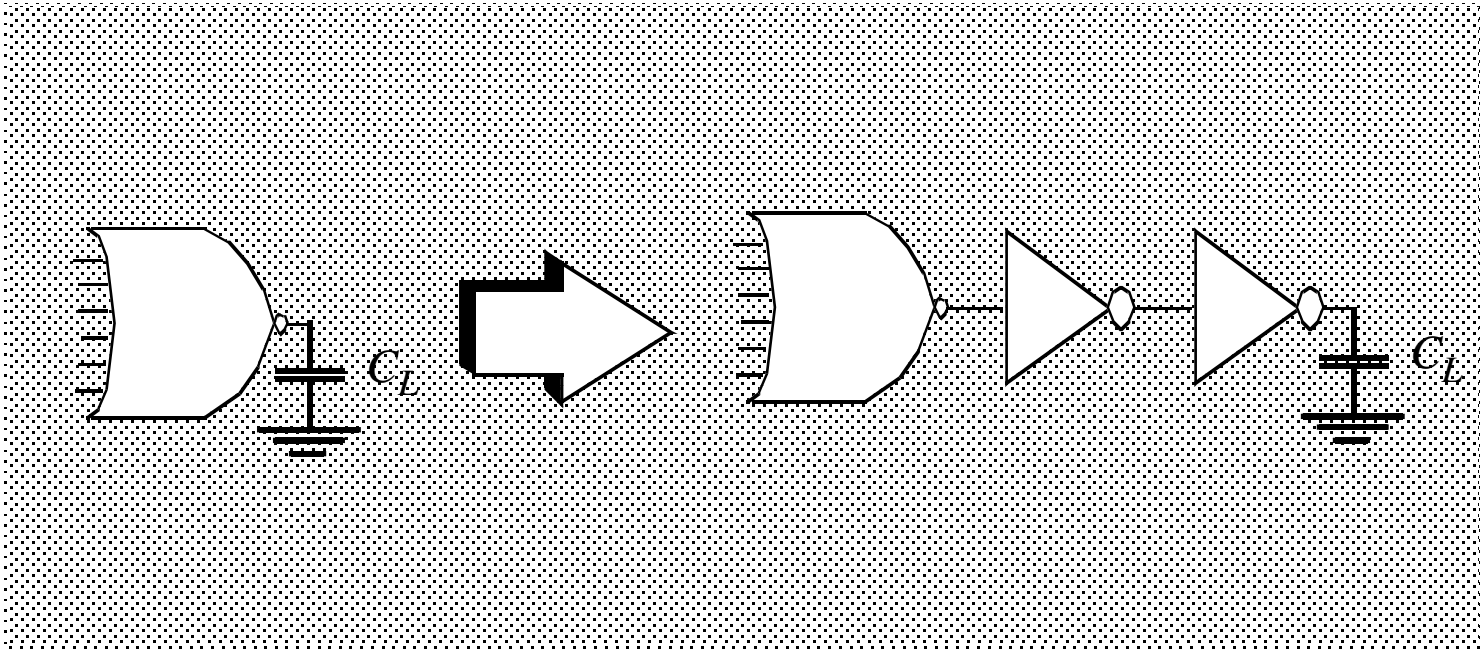
Fast Complex Gate - Design Techniques (3)

- **Improved Logic Design**

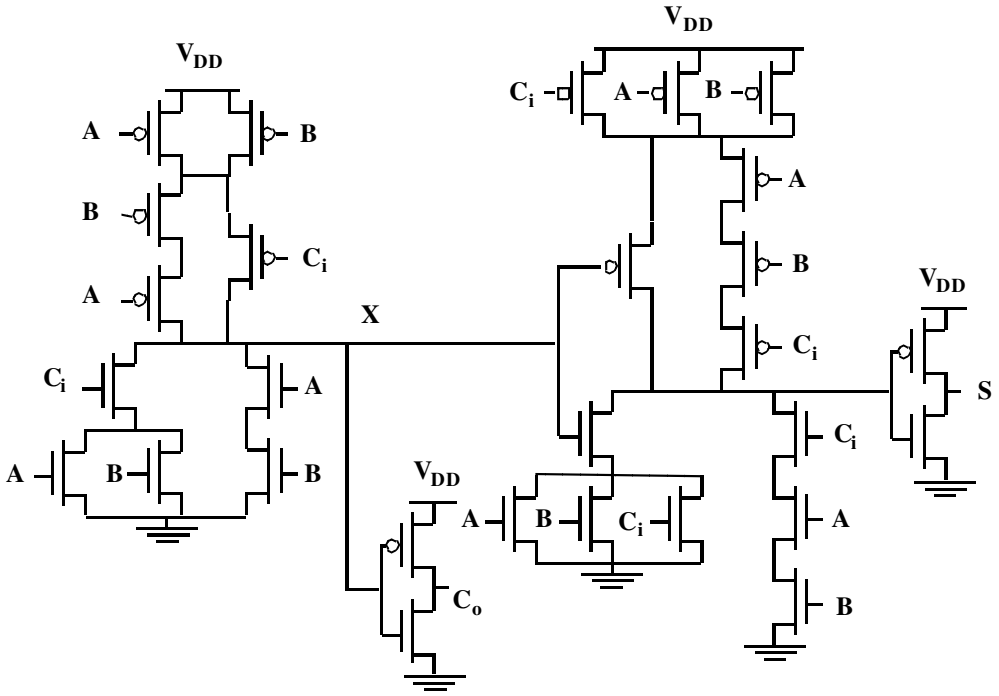


Fast Complex Gate - Design Techniques (4)

- **Buffering: Isolate Fan-in from Fan-out**



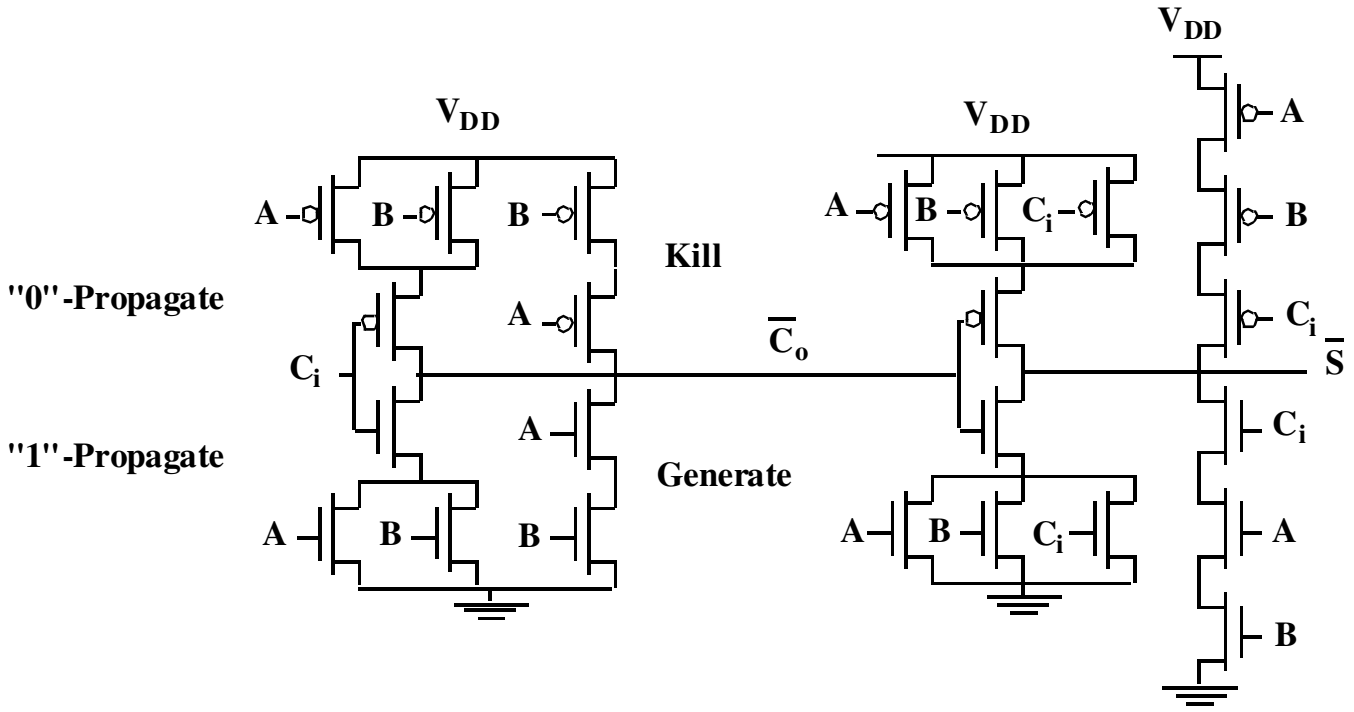
Example: Full Adder



$$C_o = AB + C_i(A+B)$$

28 transistors

A Revised Adder Circuit



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