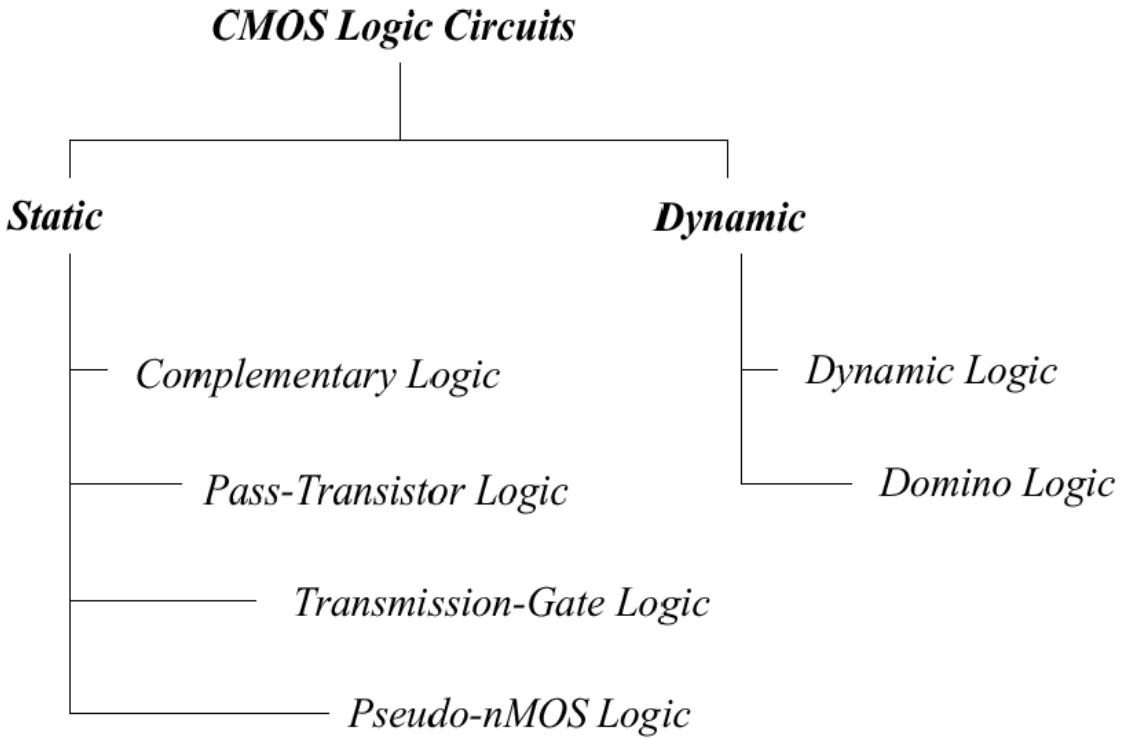
Unit 3
Combinational MOS Logic Circuits

CMOS Logic Structures

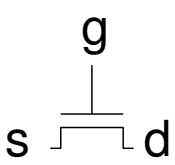
- Static logic circuits hold their output values indefinitely
- Dynamic logic circuits store the output in a capacitor, so it decays with time unless it is refreshed.
- We will look at a few of these structures

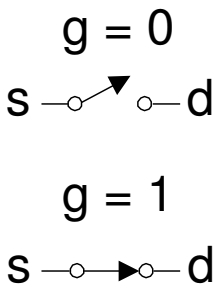


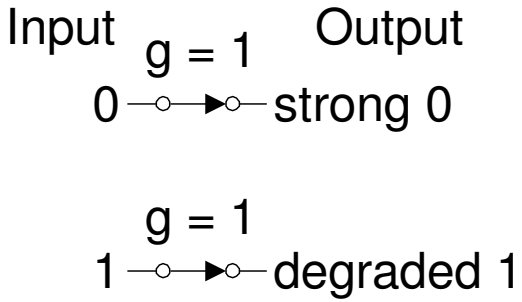
Different structures of CMOS logic circuits.

Pass Transistors

- Transistors can be used as switches





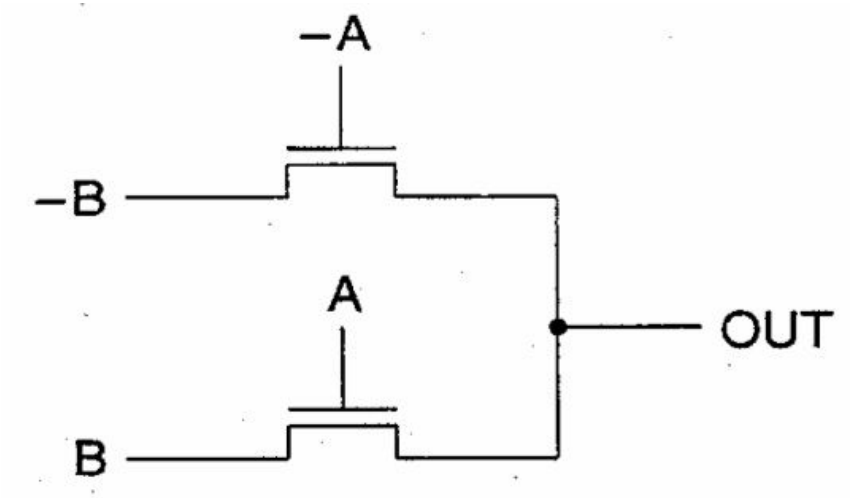


Pass Transistor

- Pass-transistor circuits are formed by dropping the PMOS transistors and using only NMOS pass transistors
- In this case, CMOS inverters (or other means) must be used periodically to recover the full V_{DD} level since the NMOS pass transistors will provide a V_{OH} of $V_{DD} – V_{Tn}$ in some cases
- The pass transistor circuit requires complementary inputs and generates complementary outputs to pass on to the next stage

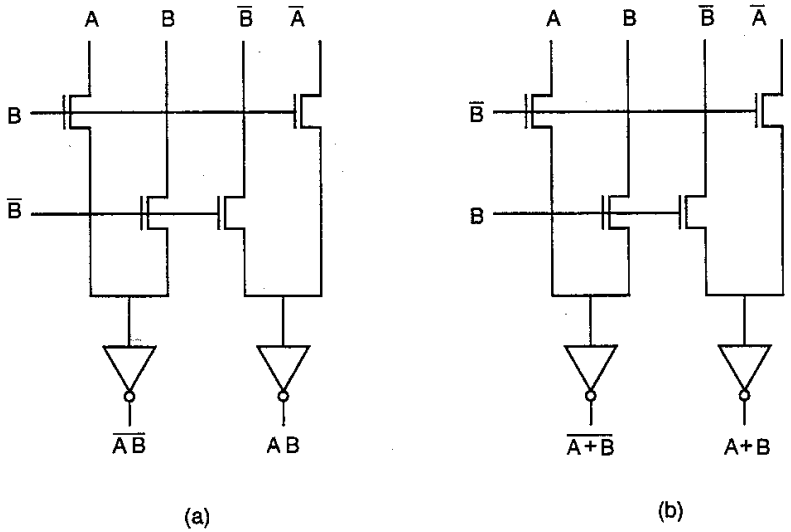
Pass Transistor

- This figure shows a simple XNOR implementation using pass transistors:
- If A is high, B is passed through the gate to the output
- If A is low, -B is passed through the gate to the output



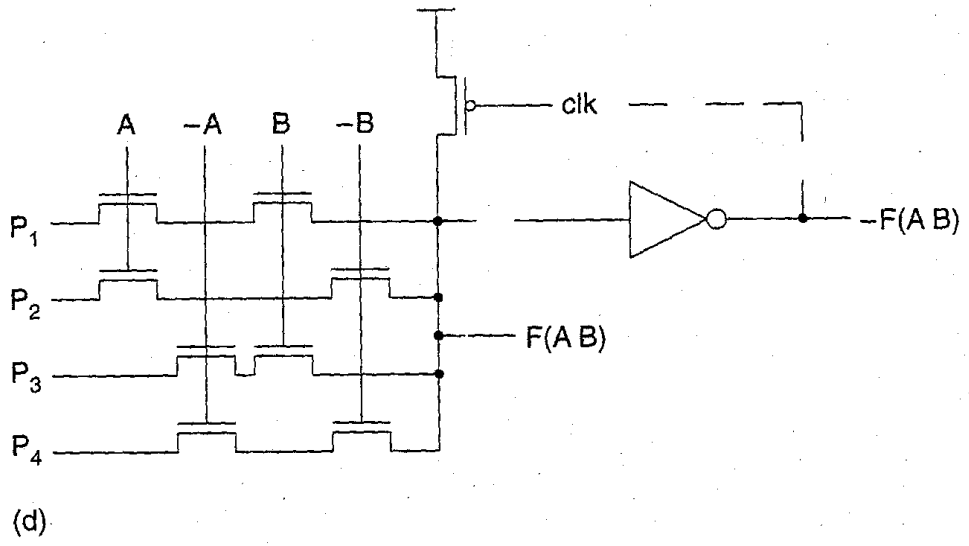
Pass Transistor

- At right,
  - (a) is a 2-input NAND pass transistor circuit
  - (b) is a 2-input NOR pass transistor circuit
- Each circuit requires 8 transistors, double that required using conventional CMOS realizations



Pass Transistor

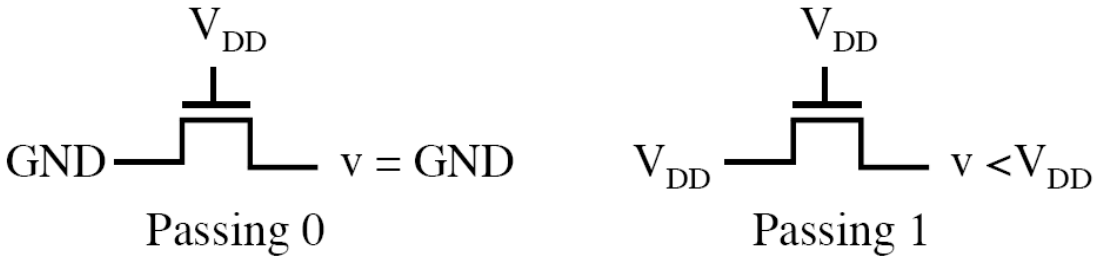
- Pass-transistor logic gate can implement Boolean functions NOR, XOR, NAND, AND, and OR depending upon the P1-P4 inputs, as shown below.
  - P1,P2,P3,P4 = 0,0,0,1 gives F(A,B) = NOR
  - P1,P2,P3,P4 = 0,1,1,0 gives F(A,B) = XOR
  - P1,P2,P3,P4 = 0,1,1,1 gives F(A,B) = NAND
  - P1,P2,P3,P4 = 1,0,0,0 gives F(A,B) = AND
  - P1,P2,P3,P4 = 1,1,1,0 gives F(A,B) = OR



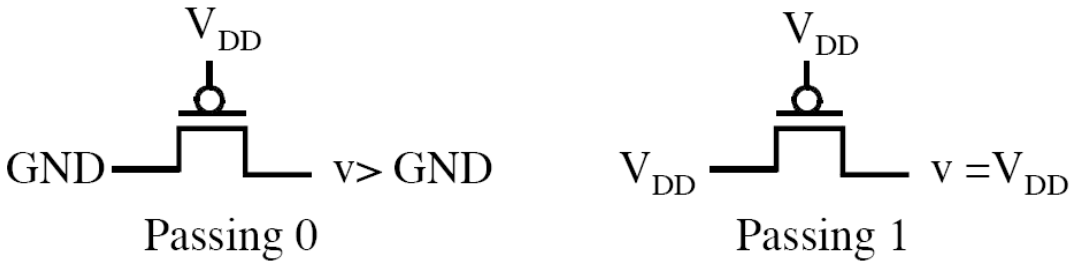
Circuit can be operated with clocked P pull-up device or inverter-based latch

Transmission Gates

- N-Channel MOS Transistors pass a 0 better than a 1



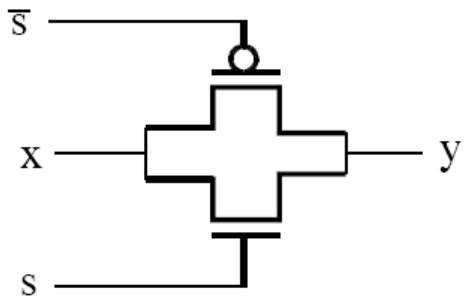
- P-Channel MOS Transistors pass a 1 better than a 0



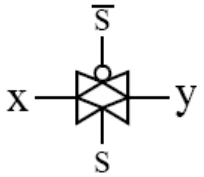
- This is the reason that N-Channel transistors are used in the pull-down network and P-Channel in the pull-up network of a CMOS gate. Otherwise the noise margin would be significantly reduced.

Transmission Gates

- A *transmission gate* is a essentially a switch that connects two points. In order to pass 0's and 1's equally well, a pair of transistors (one N-Channel and one P-Channel) are used as shown below:



Circuit

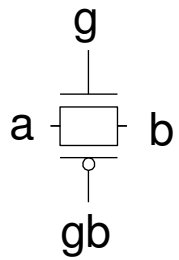


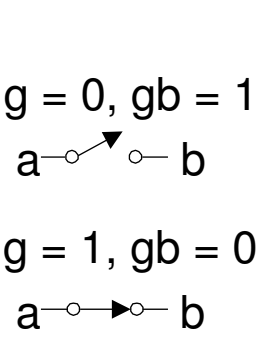
Symbol

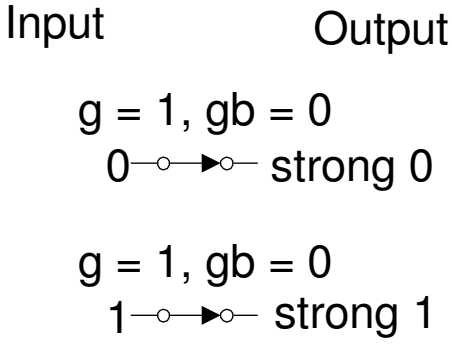
- When s = 1 the two transistors conduct and connect x and y
  - The top transistor passes x when it is 1 and the bottom transistor passes x when it is 0
- When s = 0 the two transistor are cut off disconnecting x and y

Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

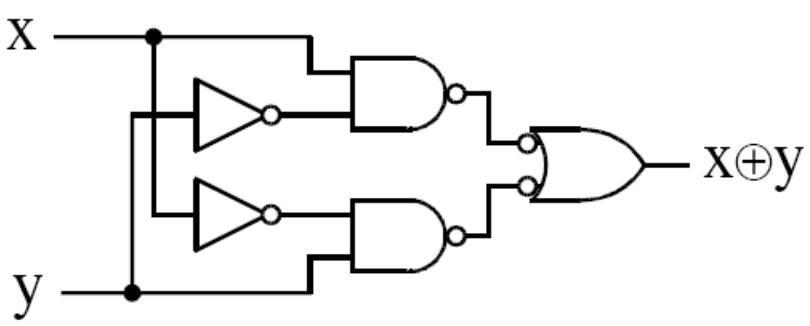




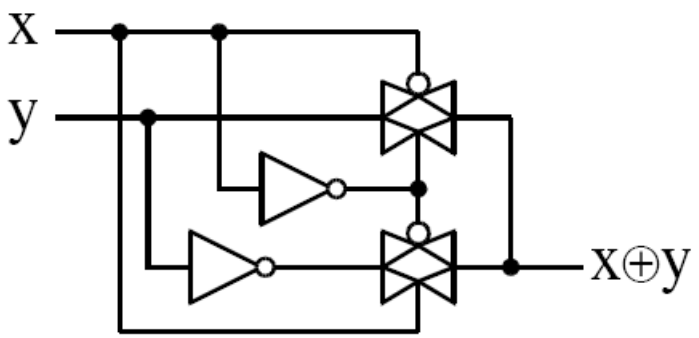


Transmission Gates

- Implementing XOR gates
  - With NAND gates and inverters:



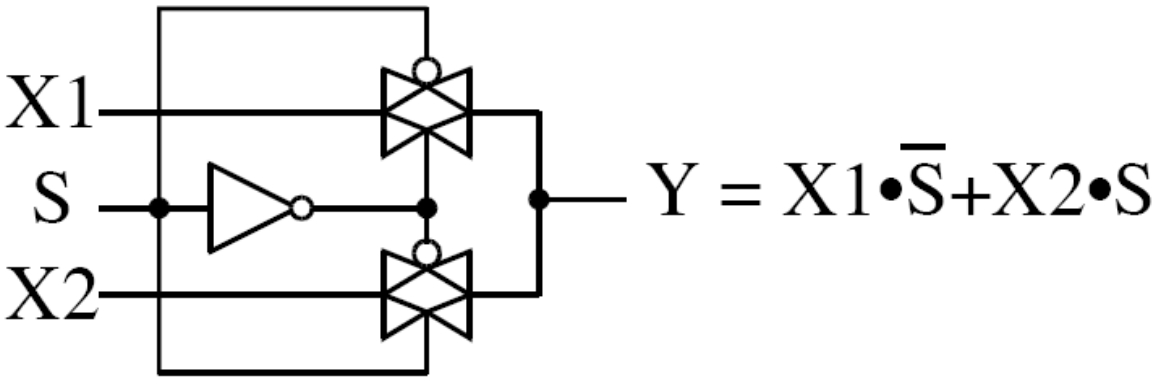
  - With transmission gates:



- Why would one of these circuits be preferable to the other?

Transmission Gates

- Implementing a multiplexer with transmission gates:



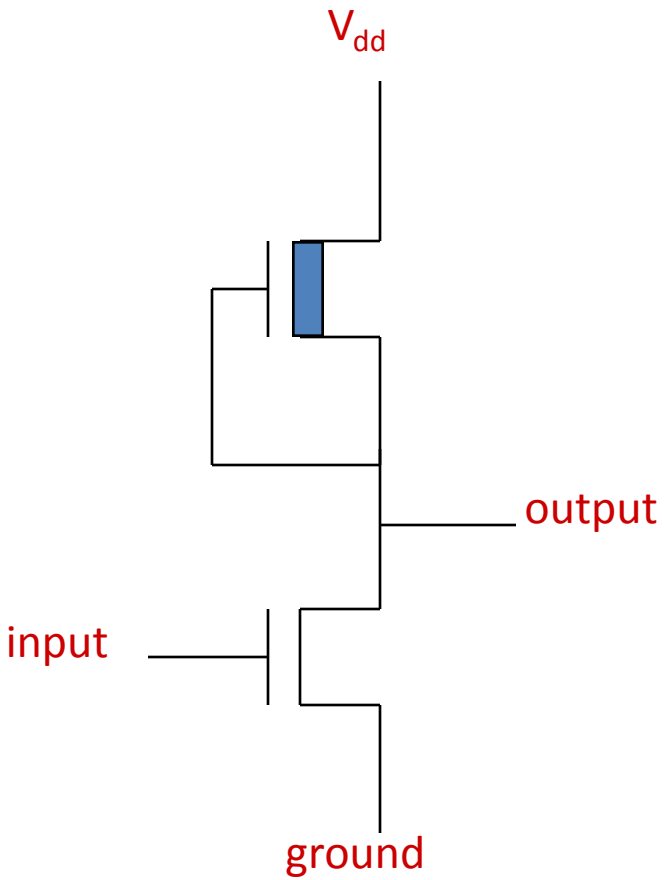
  - When S = 0, input X1 is connected to the output Y
  - When S = 1, input X2 is connected to the output Y

Dynamic Domino CMOS Logic

- One technique to help decrease power in MOS logic circuits is dynamic logic
- Dynamic logic uses different precharge and evaluation phases that are controlled by a system clock to eliminate the dc current path in single channel logic circuits
- Early MOS logic required multiphase clocks to accomplish this, but CMOS logic can be operated dynamically with a single clock

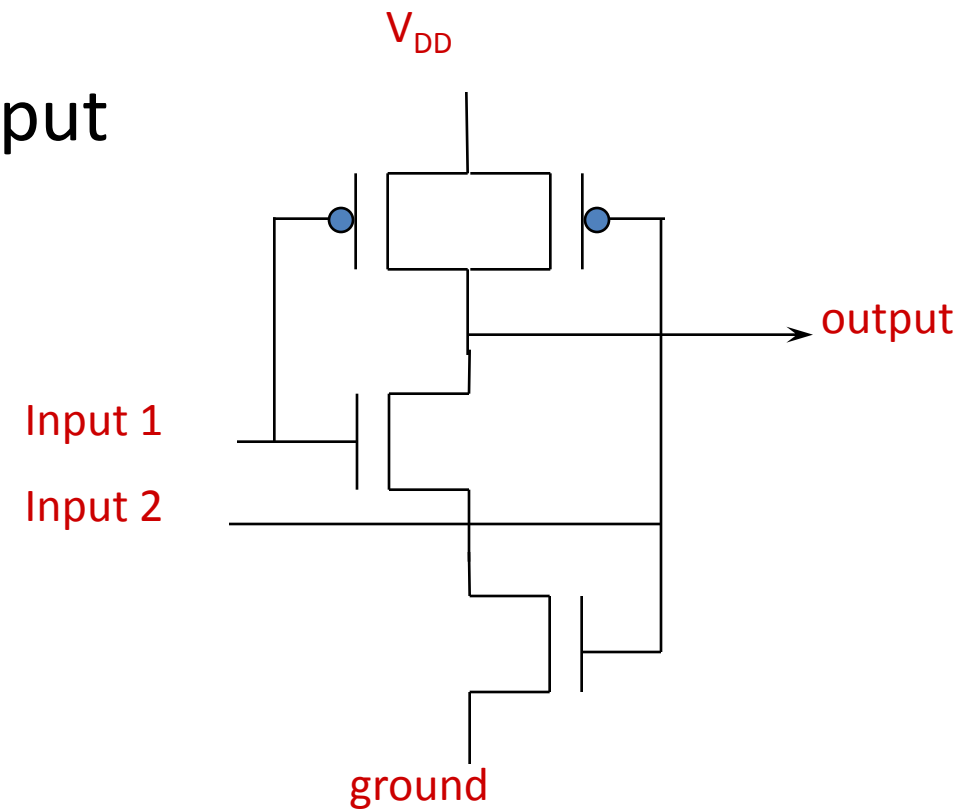
Static NMOS

- Totem-Pole Output
  - as we have seen previously
- Does not need to be refreshed
  - Which is why it is called static
- PMOS Acts as Constant Current Source for Active Pull-Up
  - Faster rise-times as compared to non-CMOS implementations



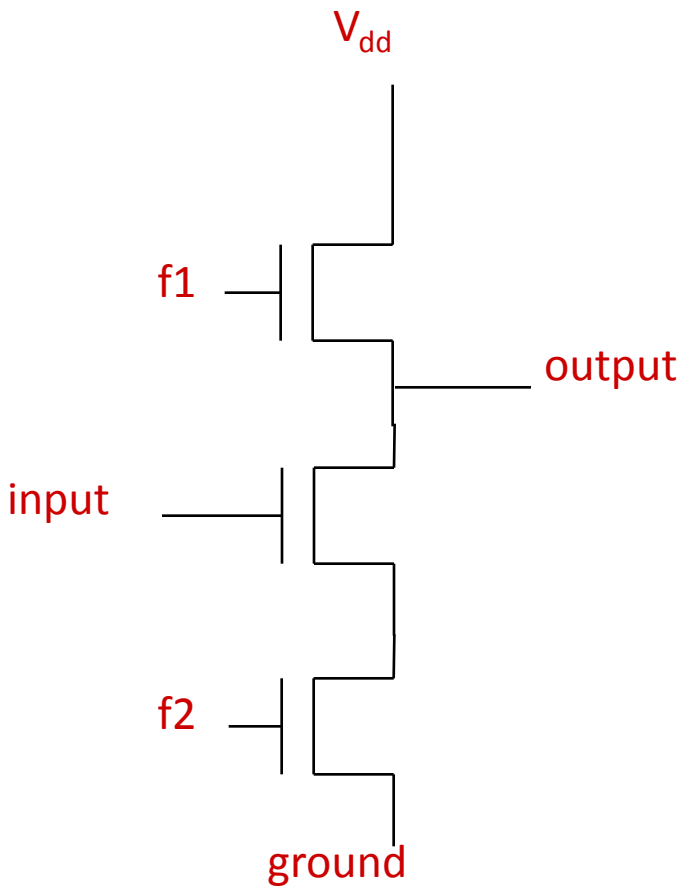
Static CMOS

- Complementary MOS
- Example of a 2-input NAND gate



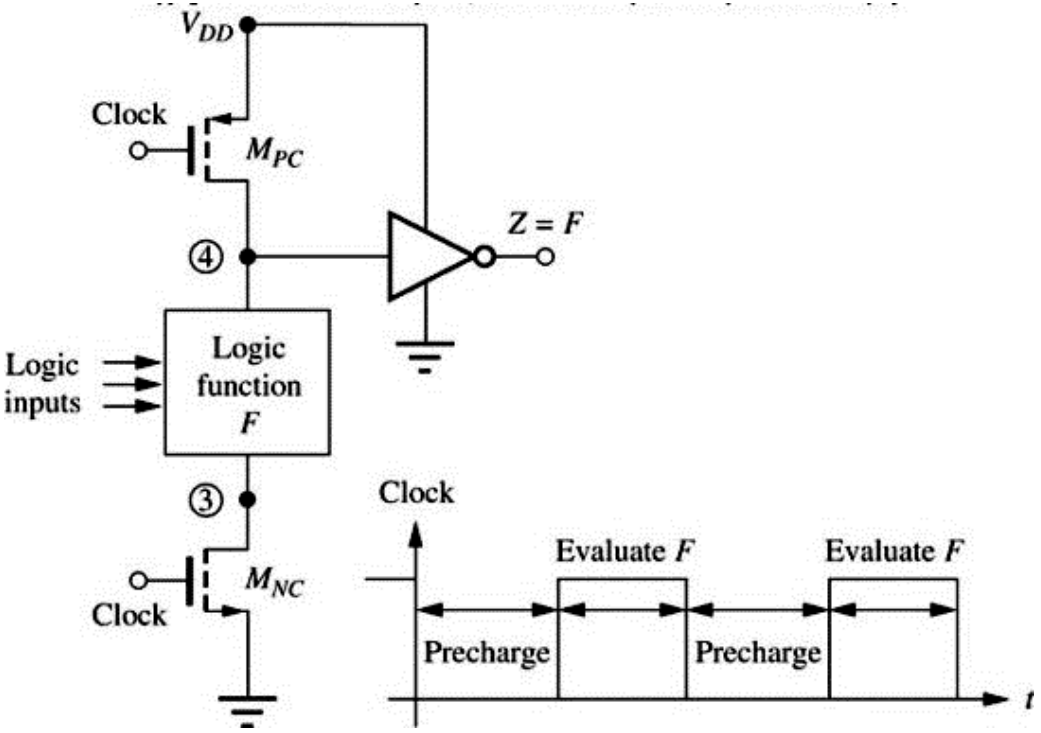
Dynamic NMOS

- Output is “1” unless discharged
- f_1 Charges Output
- f_2 Conditionally Discharges Output

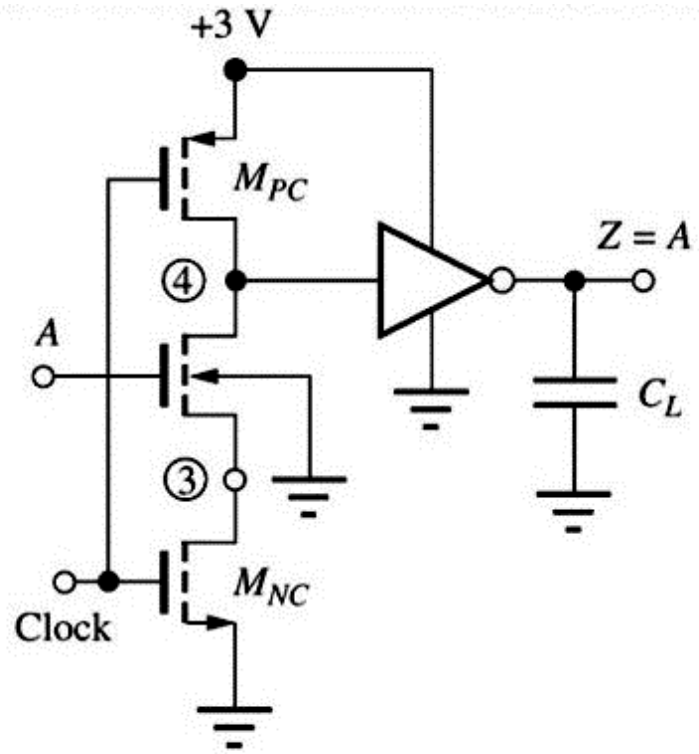


Dynamic Domino CMOS Logic

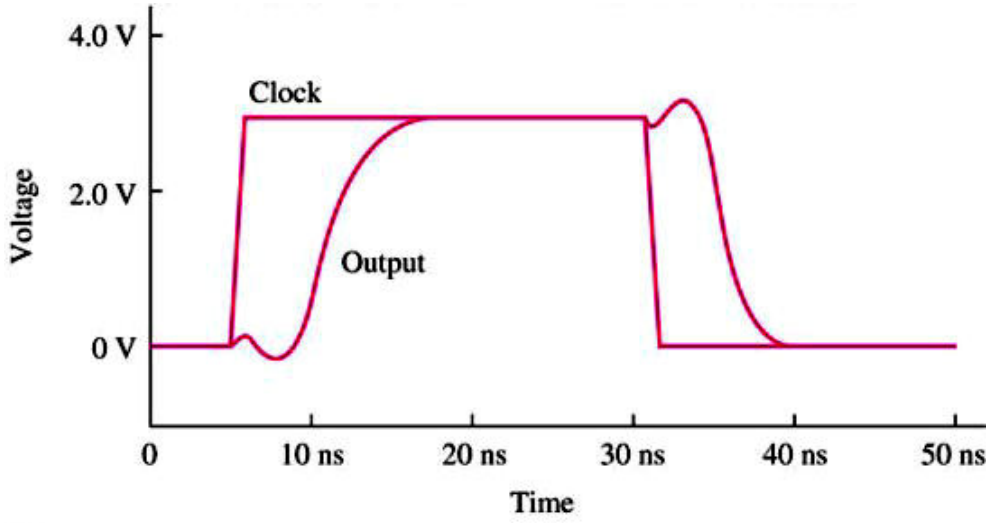
- The figure demonstrates the basic concept of domino CMOS logic operation



Simple Dynamic Domino Logic Circuit



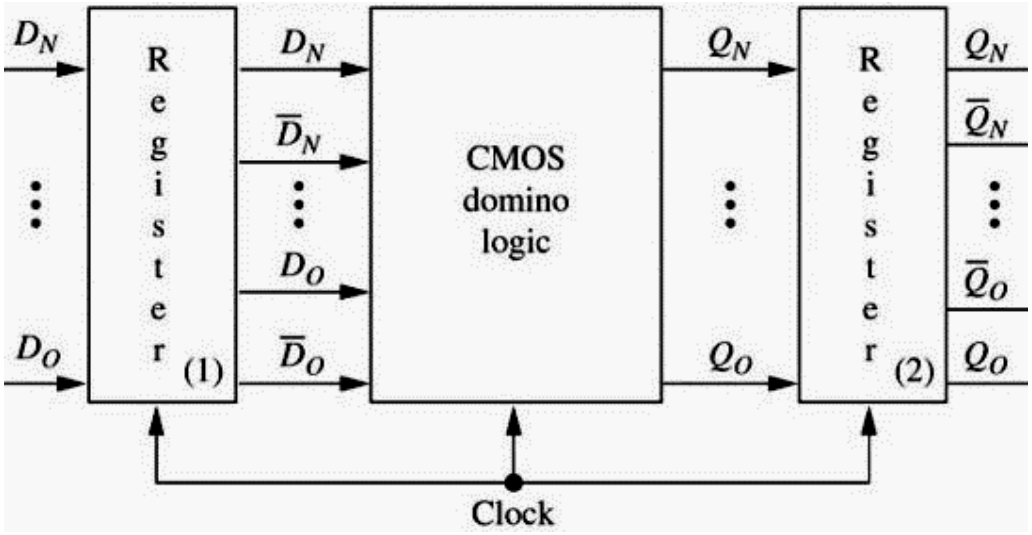
(a)



(b)

Dynamic Domino CMOS Logic

- Domino CMOS circuits only produce true logic outputs
- This can be overcome by using registers that have both true and complemented output to complete the function shown by the following circuit:

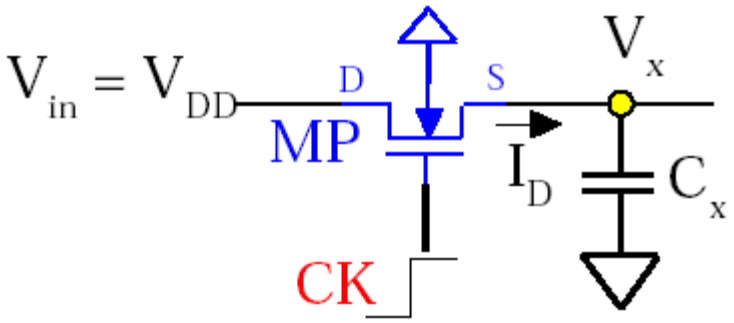


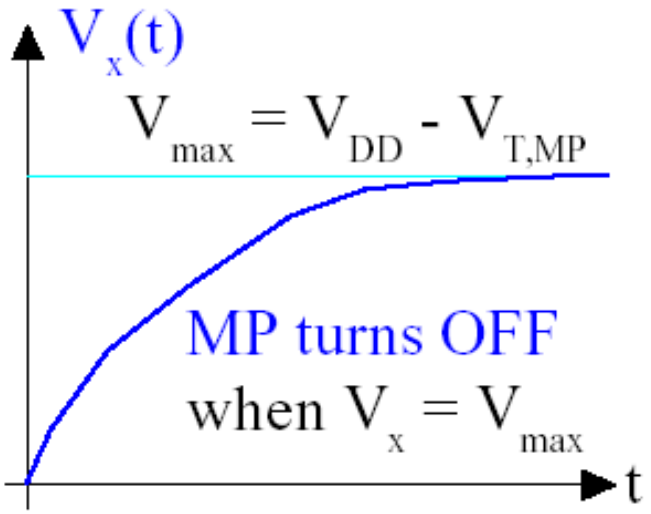
Pass Transistor Logic

Pass Transistor Logic Circuits

- **nMOS Pass transistor – transmission properties**
- Transmission Gates
- Transmission Gate Applications
  - Mux
  - XOR
  - D Latch
  - D Flip Flop
  - Clock Skew management
- Pass Transistor Logic Families

nMOS Pass Transistor – Logic '1' Transfer

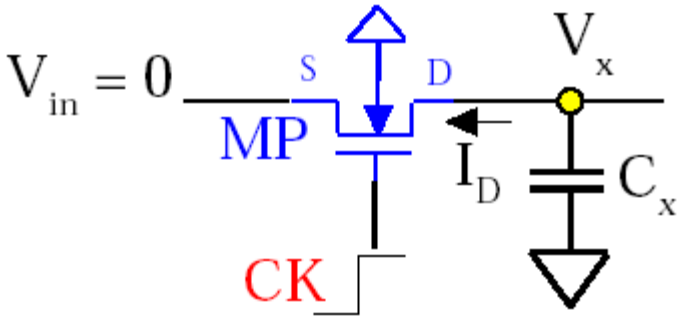


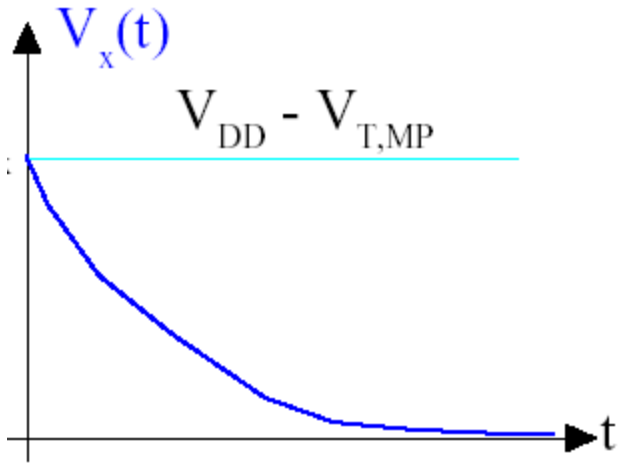


$$V_x(t) = (V_{DD} - V_{T,MP}) \frac{\frac{k_n}{2C_x}(V_{DD} - V_{T,MP})t}{1 + \left(\frac{k_n}{2C_x}(V_{DD} - V_{T,MP})\right)t}$$

$$V_{max} = V_x(t)\big|_{t=\infty} = V_{DD} - V_{T,MP}$$

nMOS Pass Transistor – Logic ‘0’ Transfer





Pass Transistor Logic

1. Very efficient in use of transistors.

2. Potentially very efficient layouts result.

3. Pass transistors can usually be minimum size devices.

4. Usually more internal node capacitance than with conventional CMOS gates.

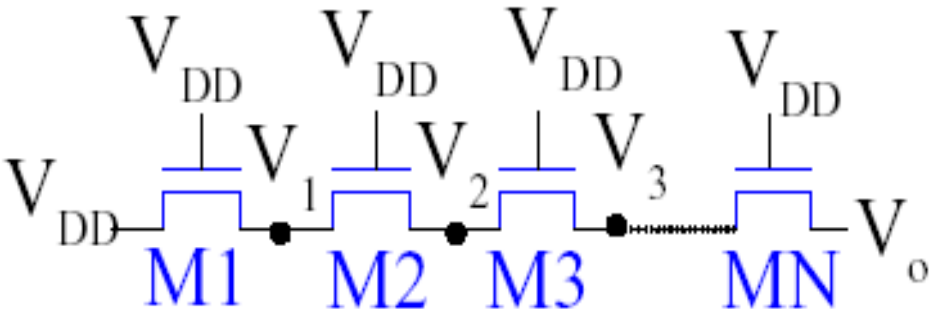
5. Propogation delays can become large in long series strings of pass transistors.

6. Use of CMOS transmission gates circumvents the V_{Tn} voltage drop of nMOS pass-transistors. It also doubles the area and interconnects.

7. Static power dissipation is uneffected.

8. Dynamic power dissipation may be decreased.

PASS TRANSISTORS IN SERIES



At t = 0: $V_{in} = V_{DD}$

$V_1 = V_2 = V_3 = .. V_o = 0$

$$V_{max1} = V_{DD} - V_{Tn1}$$

$$V_{max2} = V_{DD} - V_{Tn2}$$

$$V_{maxo} = V_{DD} - V_{TnN}$$

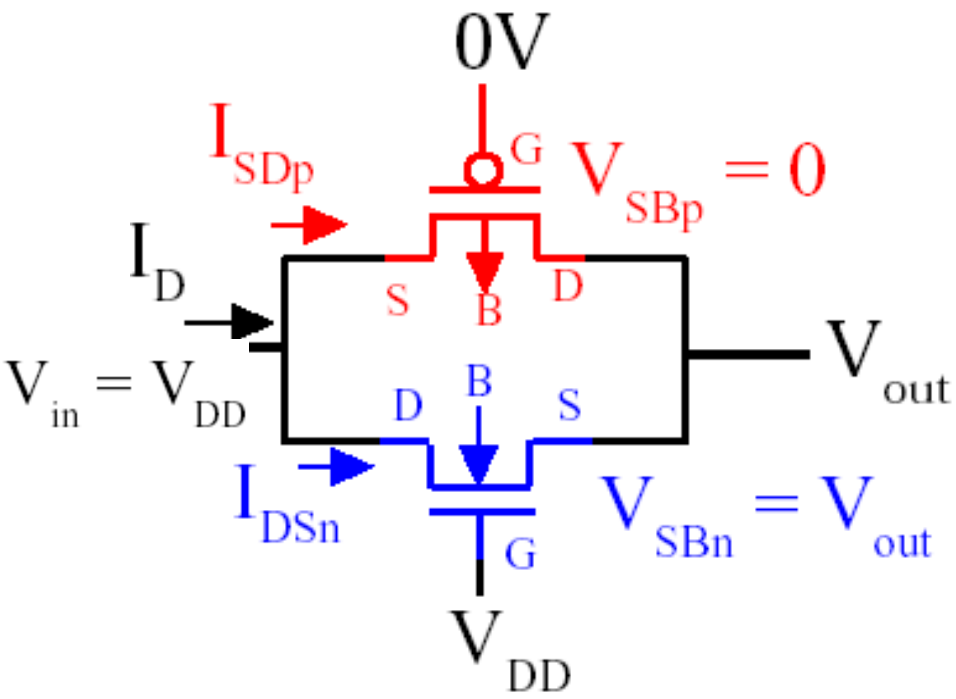
PASS TRANSISTOR LOGIC CIRCUITS

- nMOS Pass transistor – transmission properties
- **Transmission Gates**
- Transmission Gate Applications
  - Mux
  - XOR
  - D Latch
  - D Flip Flop
  - Clock Skew management
- Pass Transistor Logic Families

TRANSMISSION GATES

- NMOS pass transistor passes a ***strong*** 0 and a ***weak*** 1.
- PMOS pass transistor passes a ***strong*** 1 and a ***weak*** 0.
- Combine the two to make a CMOS pass gate which will pass a ***strong*** 0 and a ***strong*** 1.

TRANSMISSION GATE



PROBLEMS WITH TRANSMISSION GATES

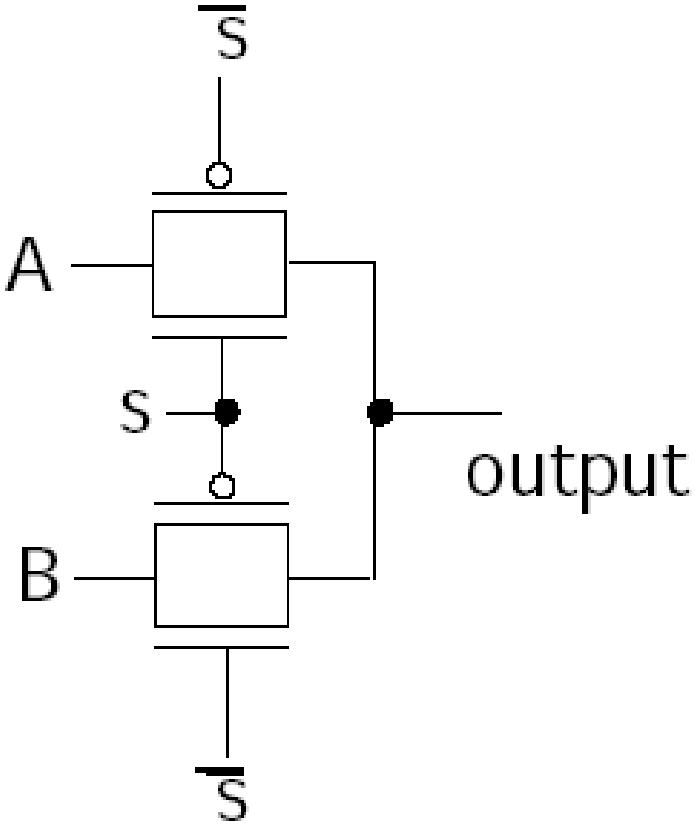
- No isolation between the input and output.
- Output progressively deteriorates as it passes through various stages.

However designs get simplified.

PASS TRANSISTOR LOGIC CIRCUITS

- nMOS Pass transistor – transmission properties
- Transmission Gates
- **Transmission Gate Applications**
  - **Mux**
  - XOR
  - D Latch
  - D Flip Flop
  - Clock Skew management
- Pass Transistor Logic Families

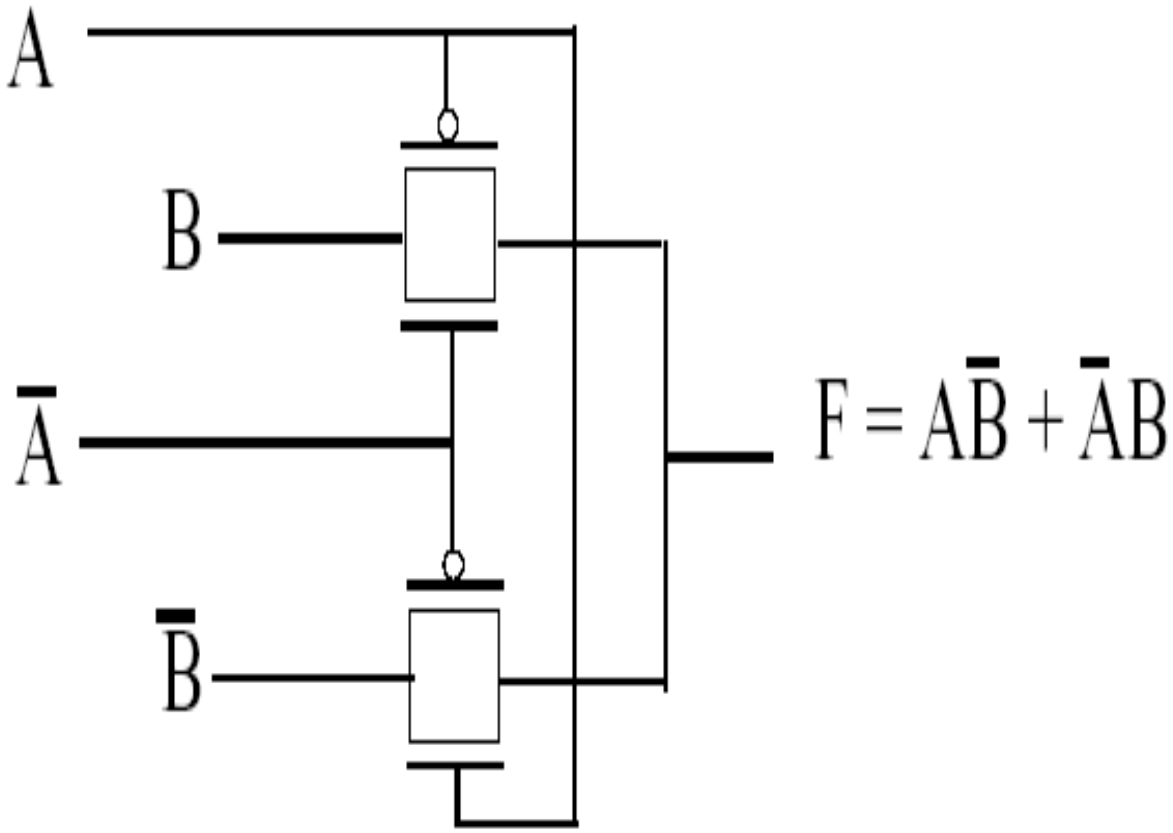
Multiplexor



$$output = A.s + B.\overline{s}$$

A	B	s	$\overline{s}$	output
x	0	0	1	0 (B)
x	1	0	1	1 (B)
0	x	1	0	0 (A)
1	x	1	0	1 (A)

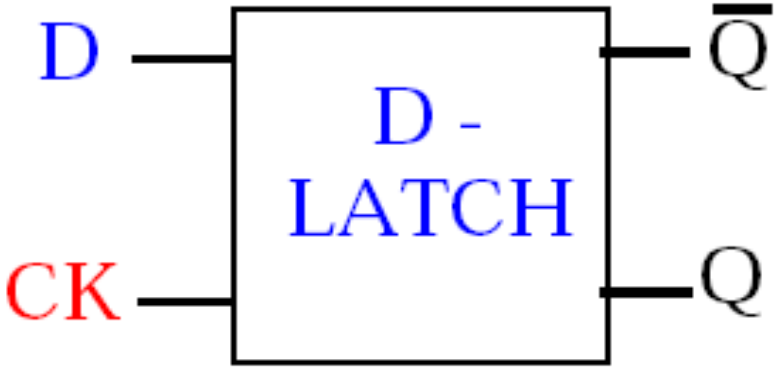
XOR gate



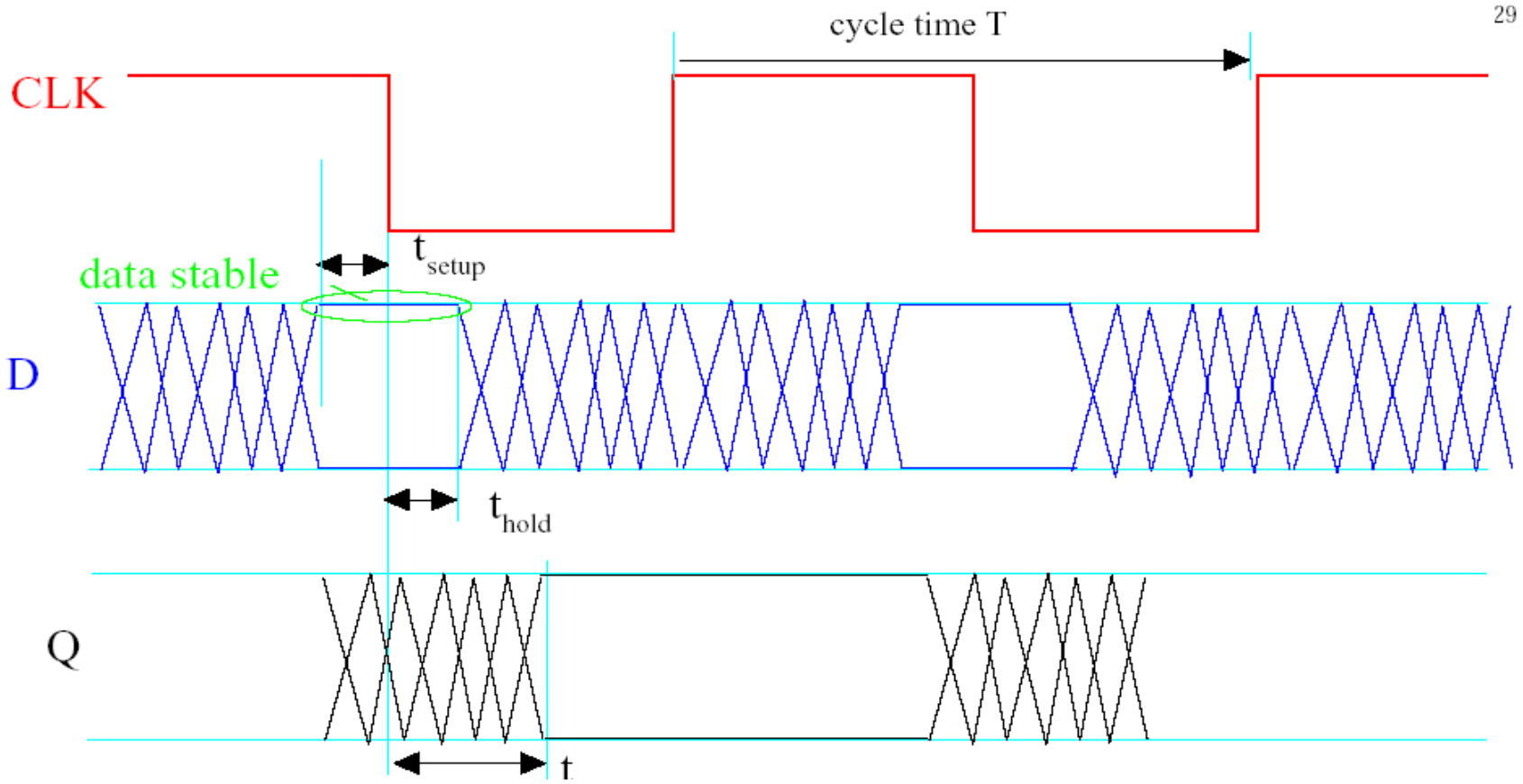
D – Latch

If CK = 1: $Q_{n+1} = D$

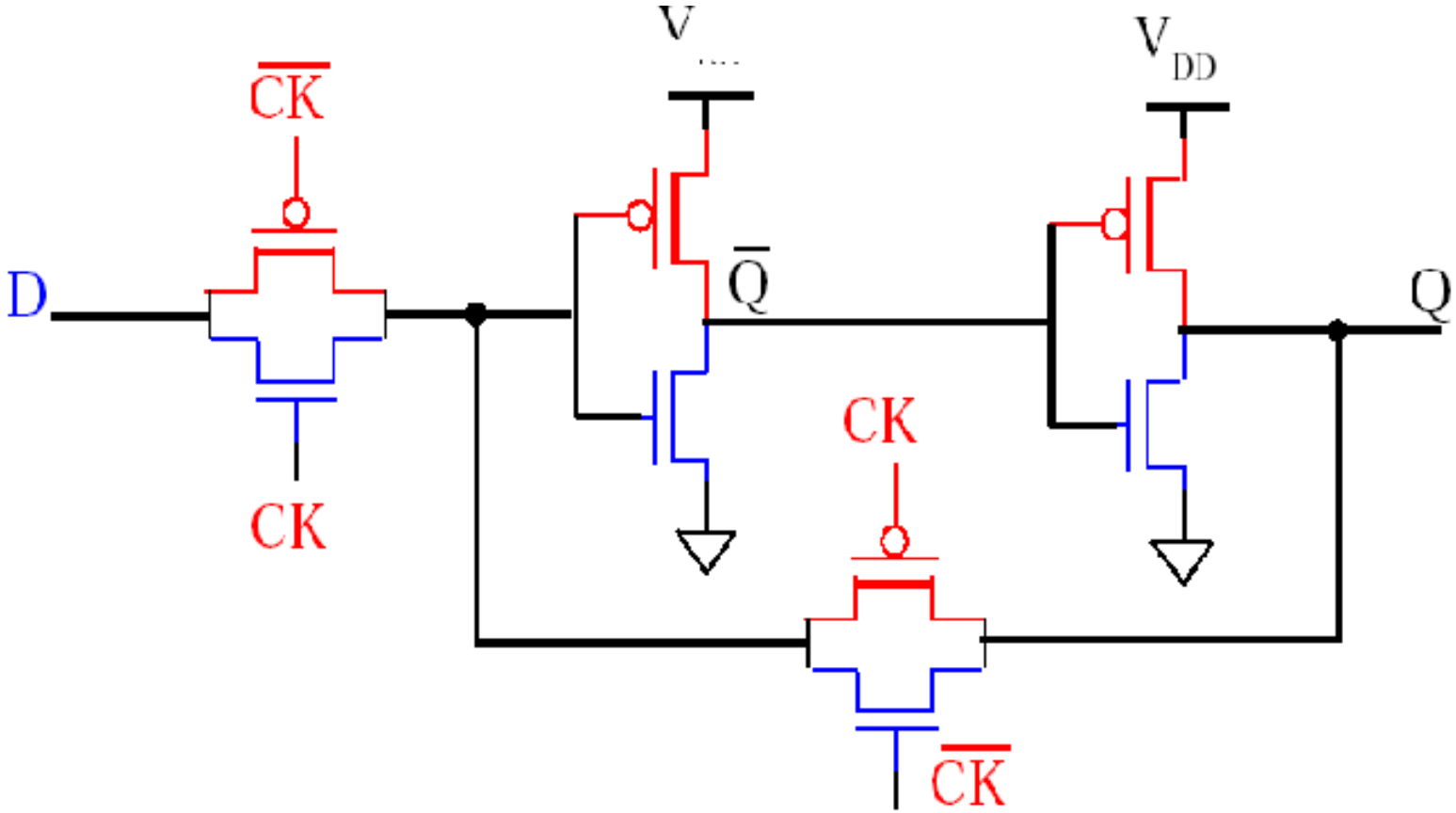
If CK = 0: $Q_{n+1} = Q_n$



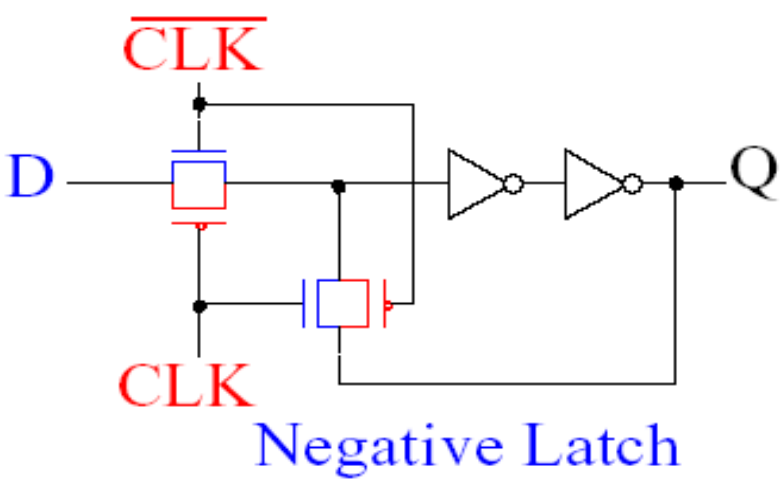
TIMING ISSUES



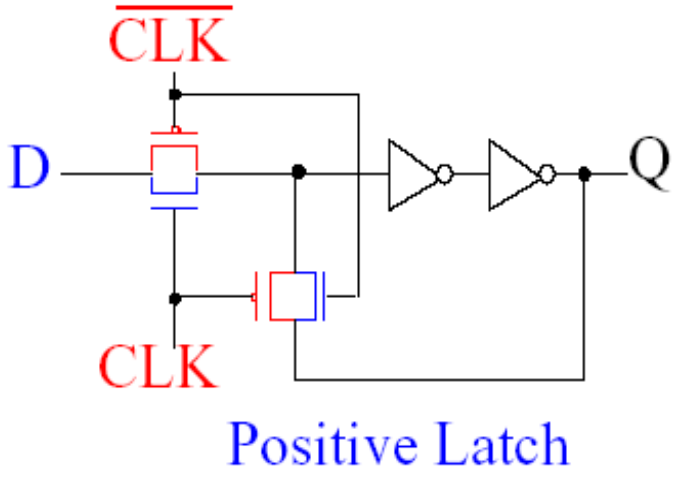
D LATCH



D - LATCH

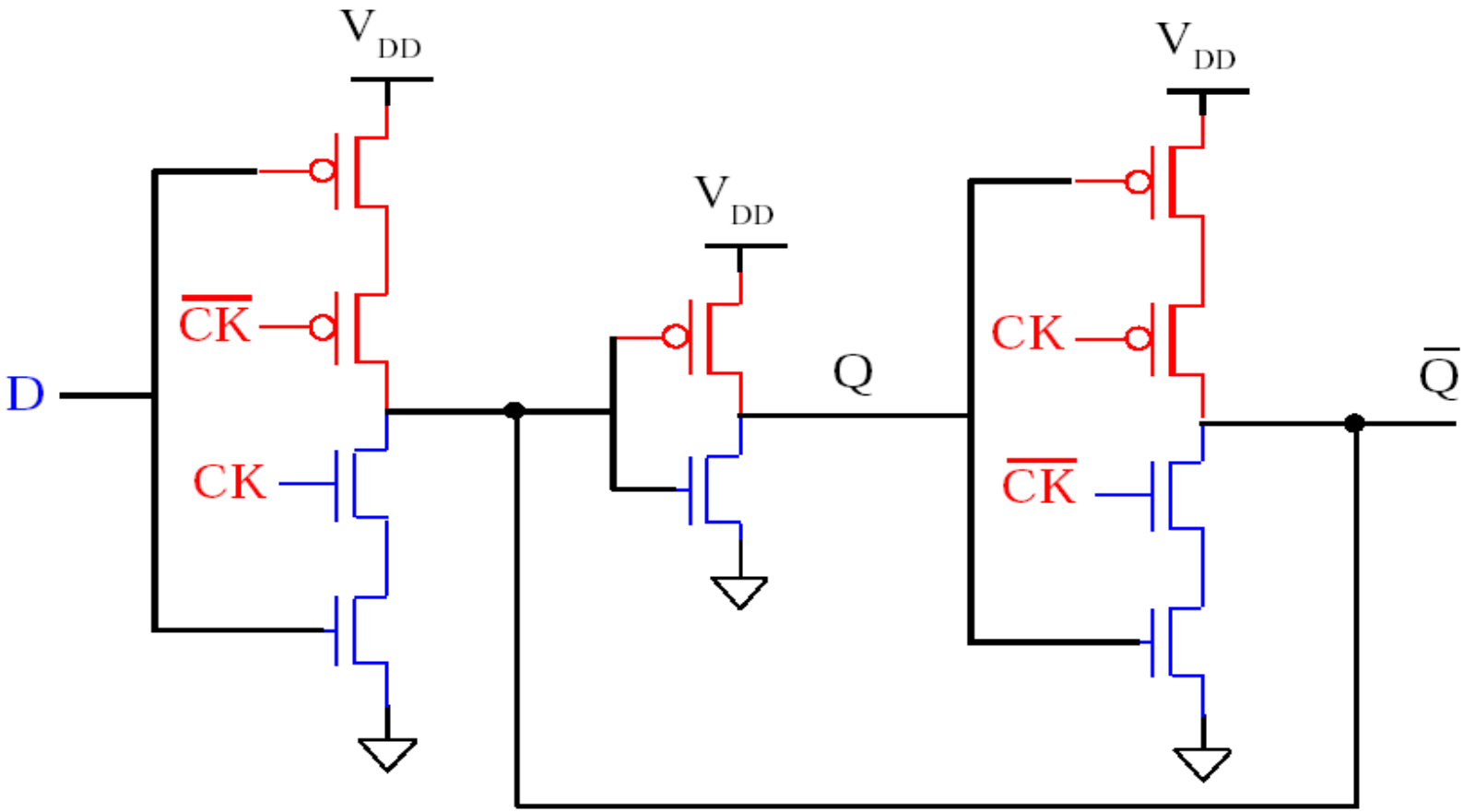


Negative Latch

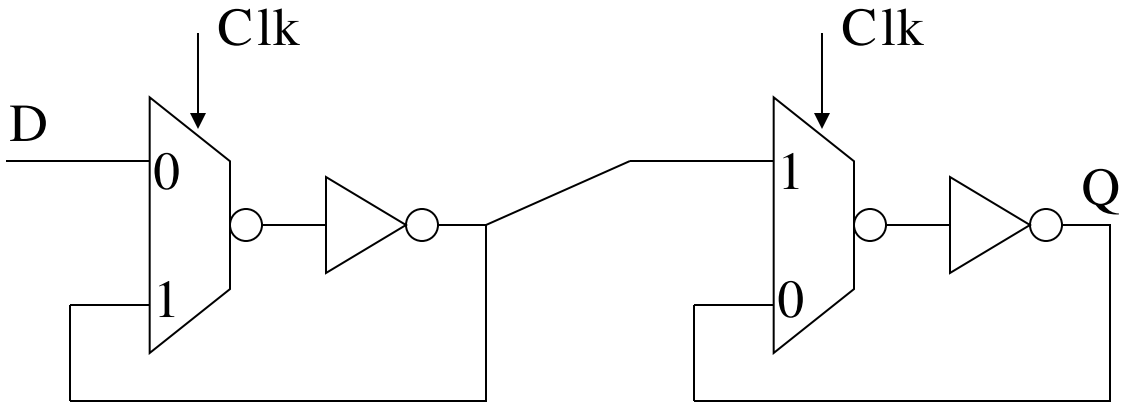


Positive Latch

D LATCH – ALTERNATE CIRCUIT TOPOLOGY



Static Flip Flop

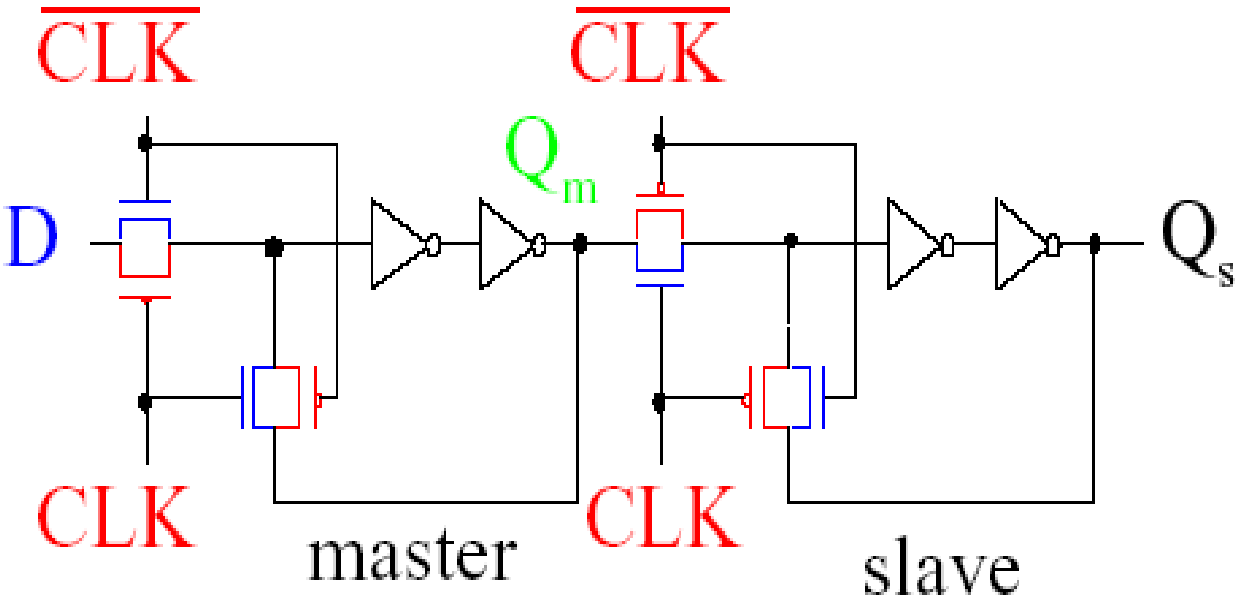


Transparent when Clk=0

Transparent when Clk=1

At Clk= 0 $\rightarrow$ 1, Q = D. Else Q is held.

D Flip Flop – Circuit Diagram



D Flip Flop - Operation

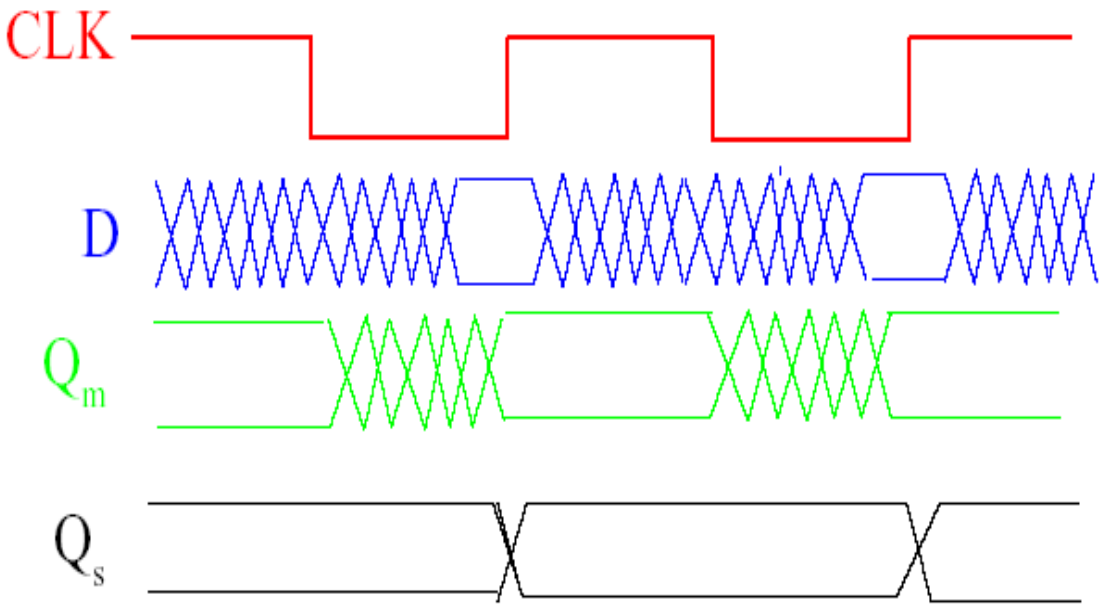
1. CLK = 0: master Q_m tracks current D; slave Q_s = previous D sample (Q_s is transparent to variations in D).

2. CLK = 0 -> 1: master stores Q_m = D (new D sample).

3. CLK = 1: master passes Q_m = D to slave output Q_s (Q_m and Q_s are transparent to variations in D).

4. CLK = 1 -> 0: slave locks in new D, and master Q_m begins tracking D.

D Flip Flop - Waveforms

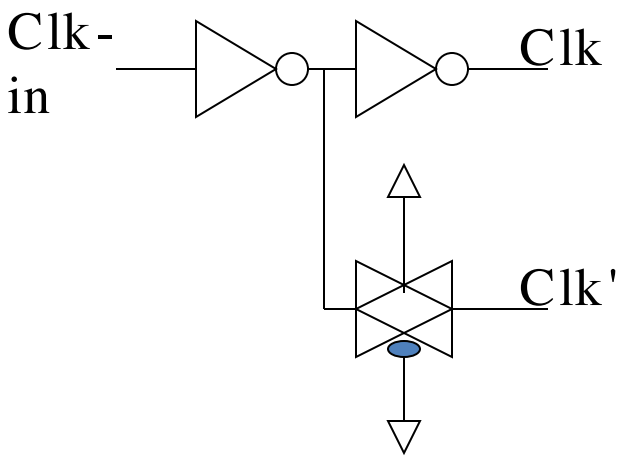


Q_s stored when CLK high and available when CLK high and low

Pass Transistor Logic Circuits

- nMOS Pass transistor – transmission properties
- Transmission Gates
- **Transmission Gate Applications**
  - Mux
  - XOR
  - D Latch
  - D Flip Flop
  - **Clock Skew management**
- Pass Transistor Logic Families

Handling Clock Skew



Pass Transistor Logic Families

- Complementary Pass Transistor Logic Family
- Dual Pass Transistor Logic Family
- Swing Restored Pass Transistor Logic Family