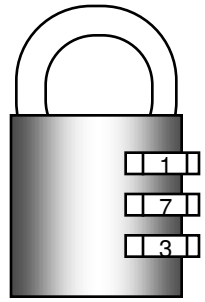
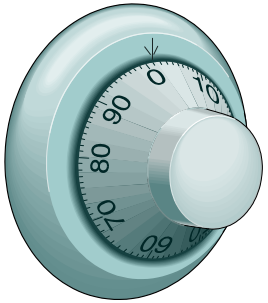
Unit 3
Combinational MOS Logic Circuits

SR LATCH

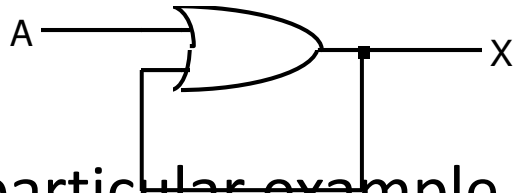
Sequential Logic Circuits



- So far we have only considered circuits where the output is purely a function of the inputs



- With sequential circuits the output is a function of the values of past and present inputs



$X = X + A$

This particular example is not very useful

Sequential Circuits - Aims

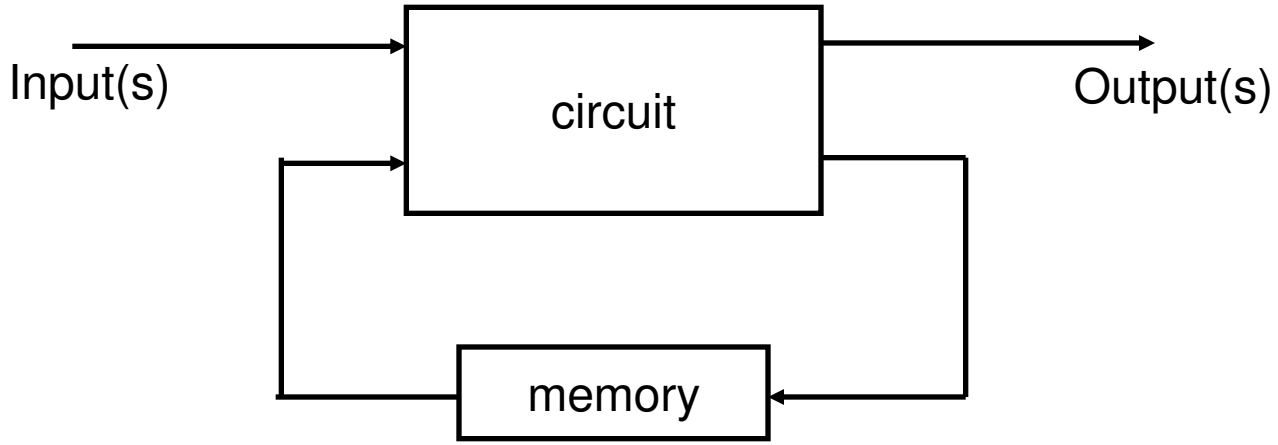
- To be able to differentiate between the various types of bistable circuits (and know when it is appropriate to use one type or another)
- To describe the structure and operation of simple registers, shift registers and binary counters
- To sketch and explain the features of a timing diagram for an n-bit register
- To be able to connect an IC (integrated circuit) counter to create a modulo-n counter or to cascade several counters to extend the range
- To generate a state transition diagram from the description of a problem, or to follow the flow of a given state transition diagram
- To apply the general sequential machine design method to sequential circuits such as counters

Latches and Flip Flops

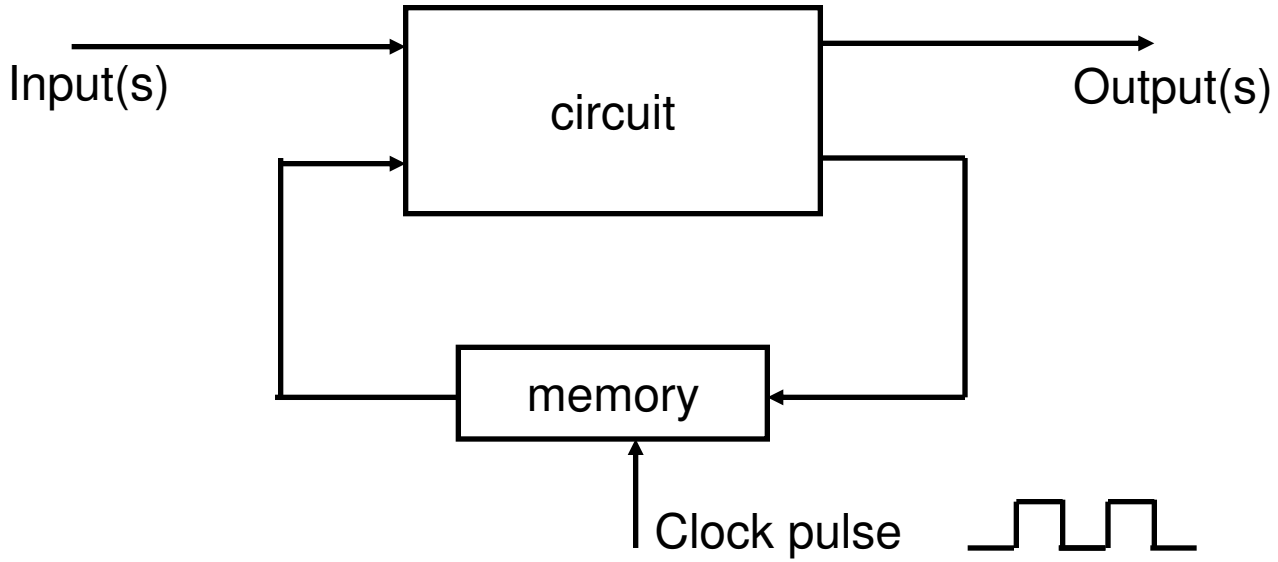
- Latches
  - SR latch
  - Clocked SR latch
  - D Latch
- Flip flops
  - Master-slave
  - Edge triggered
  - JK

Sequential circuit concepts

•The addition of a memory device to a combinational circuit allows the output to be fed back into the input:



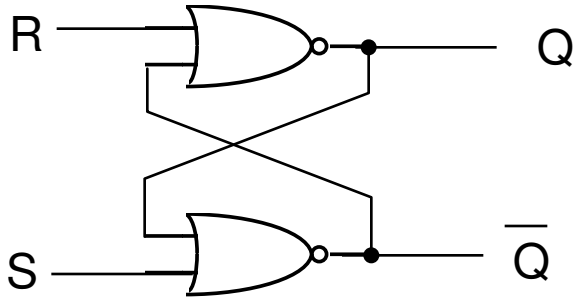
Synchronous and Asynchronous



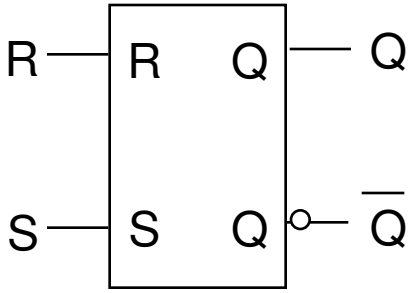
- With synchronous circuits a clock pulse is used to regulate the feedback, input signal only enabled when clock pulse is high – acts like a “gate” being opened.

Latches

- The SR Latch
  - Consider the following circuit



Circuit



Symbol

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	?

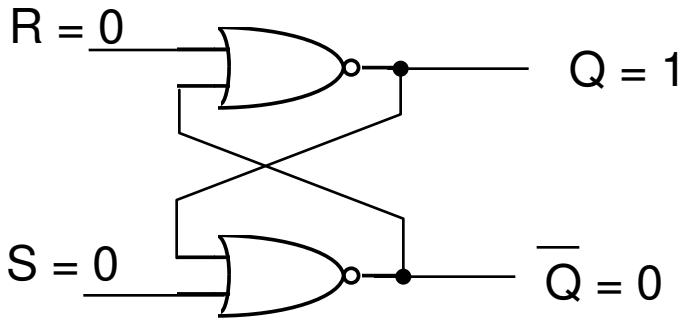
Function Table

n+1 represents output at some future time

n represents current output.

SR Latch operation

- Assume some previous operation has Q as a 1
- Assume R and S are initially inactive



Circuit

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	?

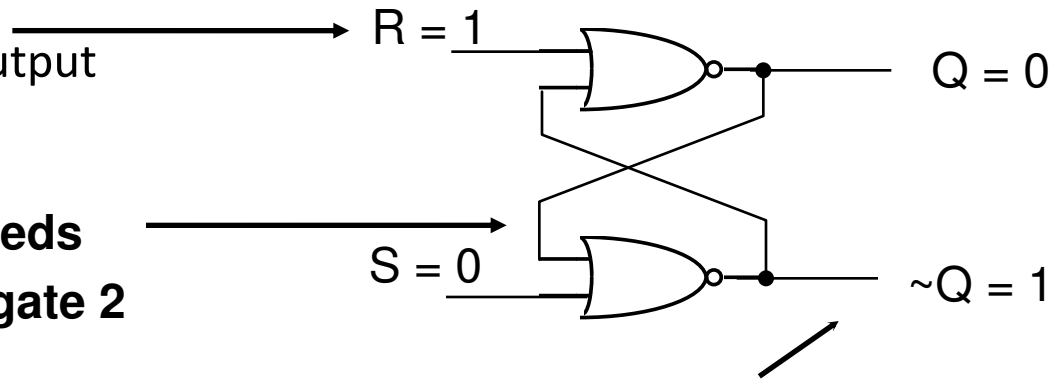
Indicates a stable state at some future time (n+ = now plus)

~Q = $\overline{Q}$, ie is the complement of Q.

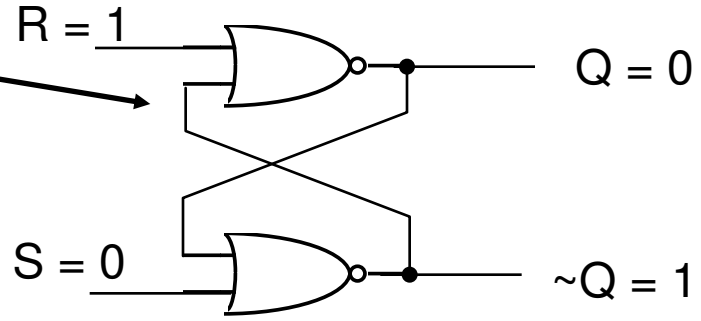
Now assume R goes first to 1 then returns to 0, what happens:

Reset goes active

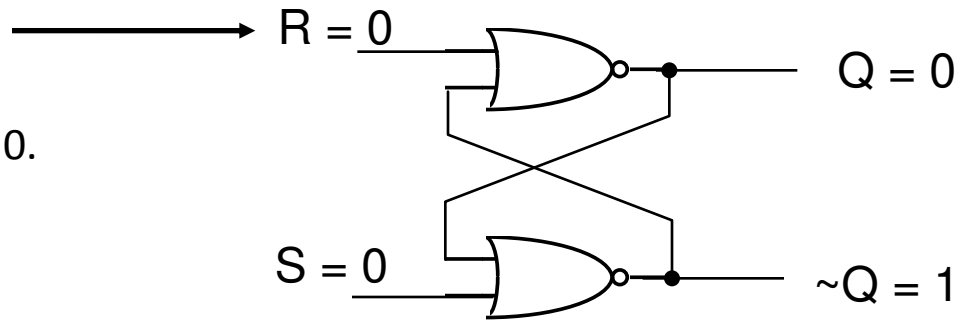
•When R goes active 1, the output from the first gate must be 0.



The output ~Q is fed back to gate 1, both inputs being 1 the output Q stays at 0.



Reset goes in-active



•When R now goes in-active 0, the feedback from ~Q (still 1), holds Q at 0.

The "pulse" in R has changed the output as shown in the function table:

We went from here → **To here** →

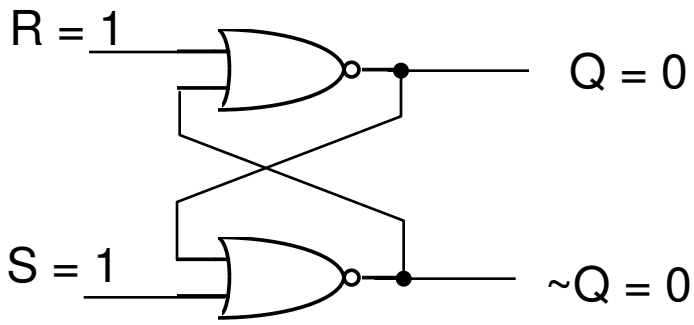
R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	?

And back again

In that process, Q changed from 1 to 0. Further signals on R will have no effect.

Set the latch

- Similar sequences can be followed to show that setting S to 1 then 0 – activating S – will set Q to a 1 stable state.
- When R and S are activated simultaneously both outputs will go to a 0



When R and S now go inactive 0, both inputs at both gates are 0 and both gates output a 1.

This 1 fedback to the inputs drives the outputs to 0, again both inputs are 0 and so on and so on and so on and so on.

Metastable state

- In a perfect world of perfect electronic circuits the oscillation continues indefinitely.

- However, delays will not be consistent in both gates so the circuit will collapse into one stable state or another.

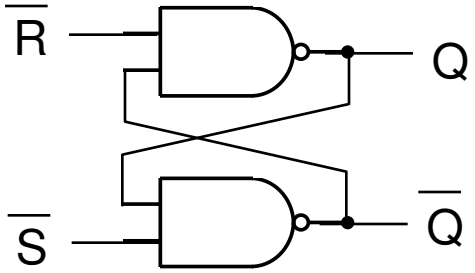
This collapse is unpredictable.

Thus our function table:

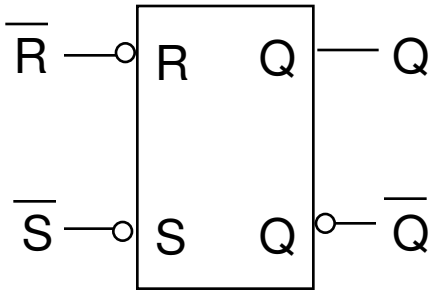
R	S	Q_{n+1}	
0	0	Q_n	Future output = present output
0	1	1	Set the latch
1	0	0	Reset the latch
1	1	?	Don't know

Latches

- The SR Latch
  - NAND Form produces similar result from inverted inputs



Circuit



Symbol

$\overline{R}$	$\overline{S}$	Q_{n+1}
0	0	?
0	1	0
1	0	1
1	1	Q_n

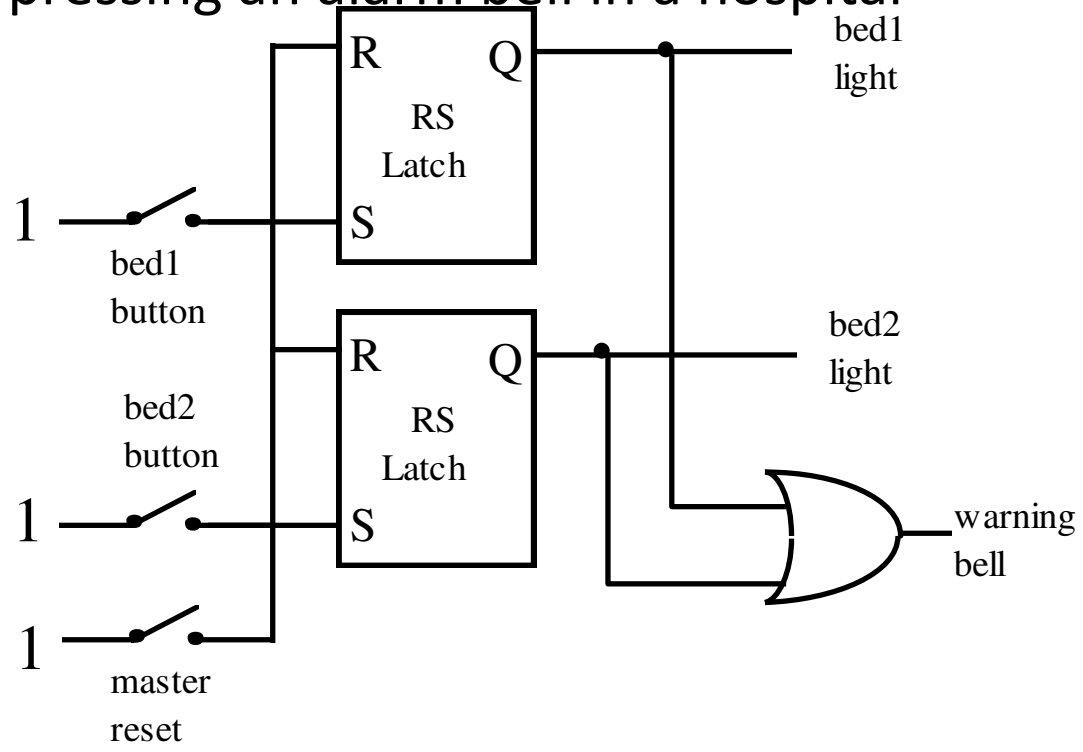
Function Table

You ought to be able to figure this one out yourself!

Application of the SR Latch

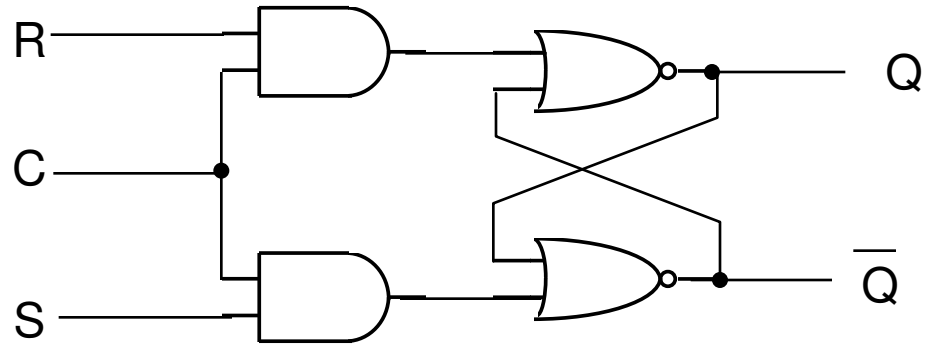
– An important application of SR latches is for recording short lived events

  • e.g. pressing an alarm bell in a hospital

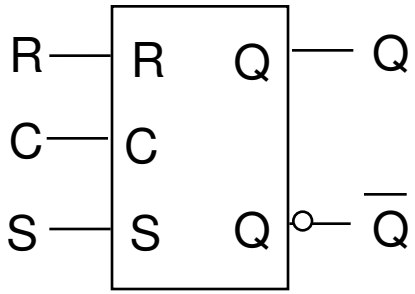


The Clocked SR Latch

- In some cases it is necessary to disable the inputs to a latch
- This can be achieved by adding a **control** or **clock** input to the latch
  - When C = 0 R and S inputs cannot reach the latch
    - Holds its stored value
  - When C = 1 R and S inputs connected to the latch
    - Functions as before



Clocked SR Latch



R	S	C	Q_{n+1}	
X	X	0	Q_n	Hold
0	0	1	Q_n	Hold
0	1	1	1	Set
1	0	1	0	Reset
1	1	1	?	Unused

Propagation Delay, set-up and hold (for transparent circuits)

- Propagation delay:
- Time taken for any change at inputs to affect outputs (change on D to change on Q).

- Setup time:
- Data on inputs D must be held steady for at least this time before the clock changes.

- Hold time:
- Data on inputs D must be held steady for at least this time after the clock changes.

Latches - Summary

- Two cross-coupled NOR gates form an SR (set and reset) latch
- A clocked SR latch has an additional input that controls when setting and resetting can take place
- A D latch has a single data input
  - the output is held when the clock input is a zero
  - the input is copied to the output when the clock input is a one
- The output of the clocked latches is transparent
- The output of the clocked D latch can be represented by the following behaviour

D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set