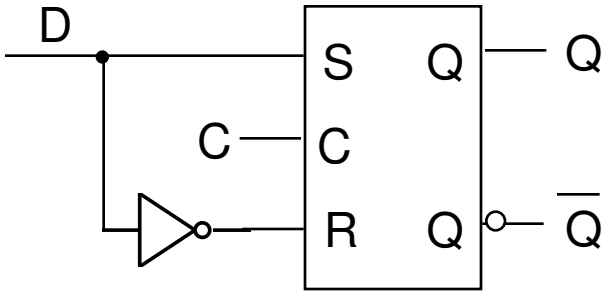
Unit 3
Combinational MOS Logic Circuits

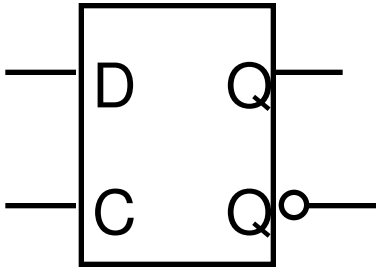
D LATCH

D Latch

- It removes the undefined behaviour of the SR latch
- Often used as a basic memory element for the short term storage of a binary digit applied to its input
- Symbols are often labeled data and enable/clock (D and C)



Circuit



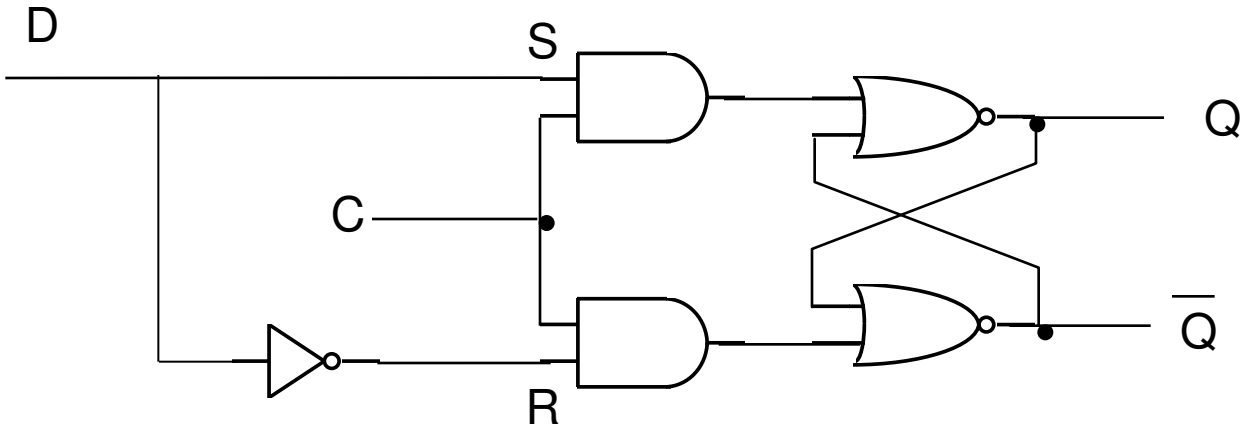
Symbol

D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set

Function Table

Clocked D Latch

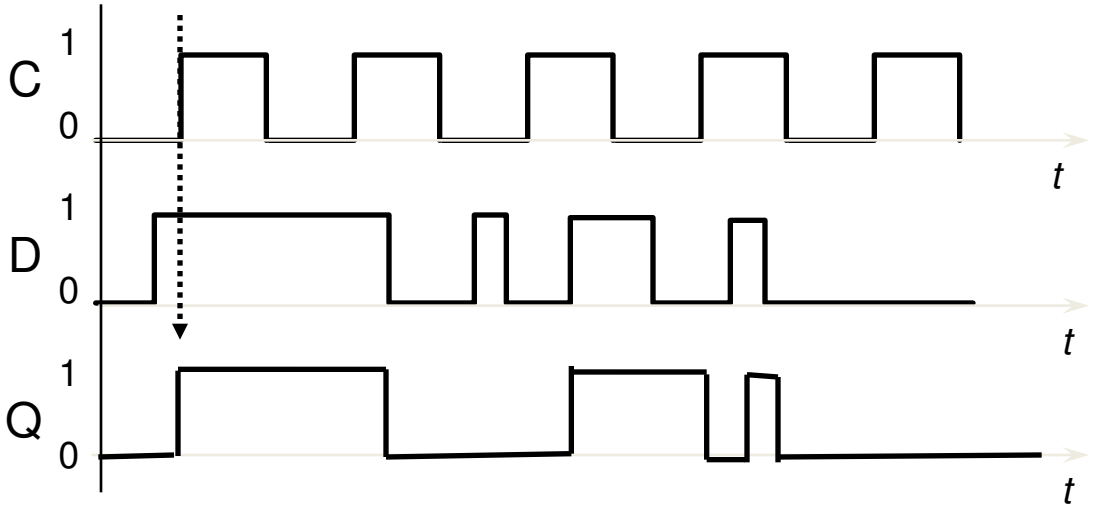
- Simplest clocked latch of practical importance is the Clocked **D latch**



  - It means that both active 1 inputs at R and S can't occur.
  - Notice we've reversed S and R so when D is 1 Q is 1.

Transparency

– The devices that we have looked so far are transparent
  - That is when C = 1 the output follows the input
  - There will be a slight lag between them



When the clock "gate" opens, changes in input take effect at outputs – transparency. Also known as "level-triggered".

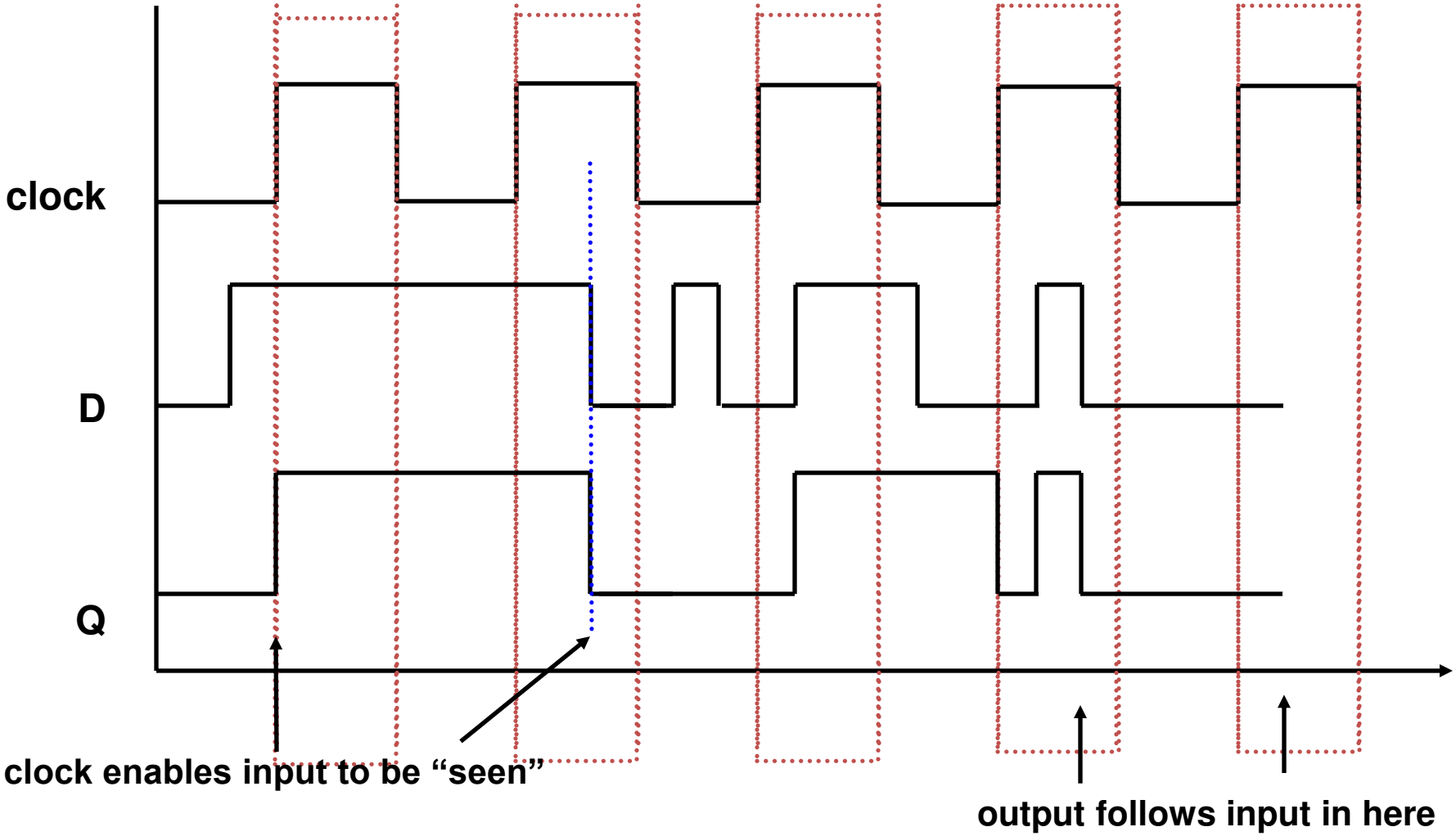
Propagation Delay, set-up and hold (for transparent circuits)

- Propagation delay:
- Time taken for any change at inputs to affect outputs (change on D to change on Q).

- Setup time:
- Data on inputs D must be held steady for at least this time before the clock changes.

- Hold time:
- Data on inputs D must be held steady for at least this time after the clock changes.

Clocked D Latch – Timing Diagram



Latches - Summary

- Two cross-coupled NOR gates form an SR (set and reset) latch
- A clocked SR latch has an additional input that controls when setting and resetting can take place
- A D latch has a single data input
  - the output is held when the clock input is a zero
  - the input is copied to the output when the clock input is a one
- The output of the clocked latches is transparent
- The output of the clocked D latch can be represented by the following behaviour

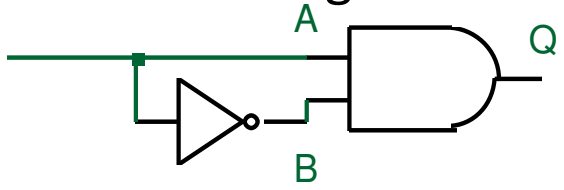
D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set

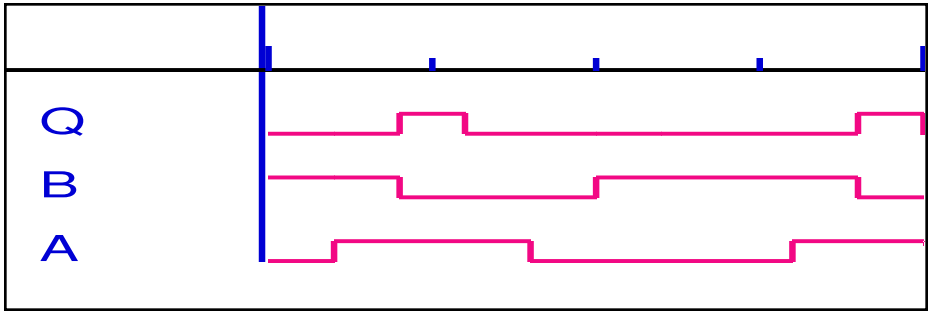
Latches and Flip Flops

- Terms are sometimes used confusingly:
- A latch is not clocked whereas a flip-flop is clocked.
- A clocked latch can therefore equally be referred to as a flip flop (SR flip flop, D flip flop).
- However, as we shall see, all practical flip flops are edge-triggered on the clock pulse.
- Sometimes latches are included within flip flops as a sub-type.

Flip-flops

- Propagation Delay
  - Will the output of the following circuit ever be a 1?



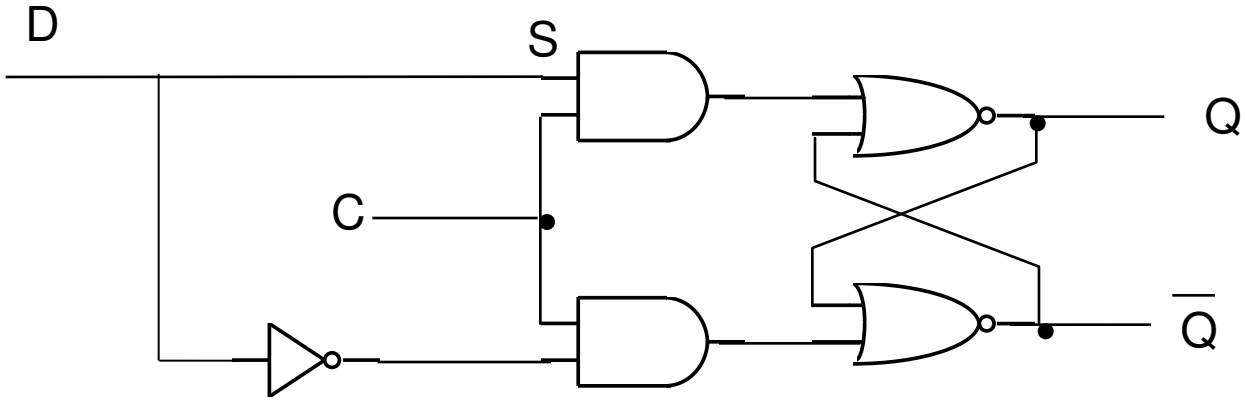


  - The brief pulse or **glitch** in the output is caused by the propagation delay of the signals through the gates

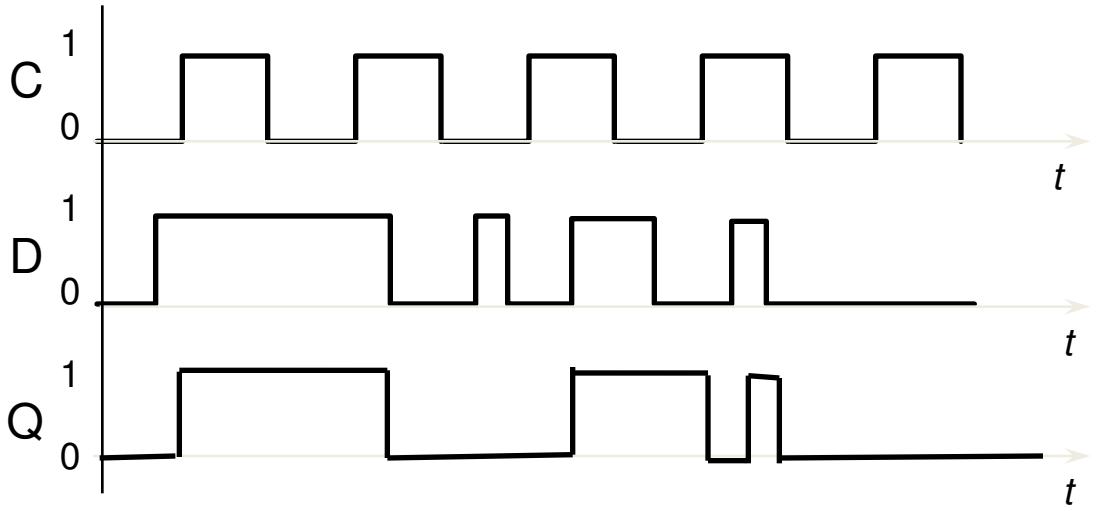
Latches and Flip Flops

- Clocked latches are level triggered. While the clock is high, inputs and thus outputs can change.
- This is not always desirable.
- A Flip Flop is edge-triggered – either by the leading or falling edge of the clock pulse.
- Ideally, it responds to the inputs only at a particular instant in time.
- It is not transparent.

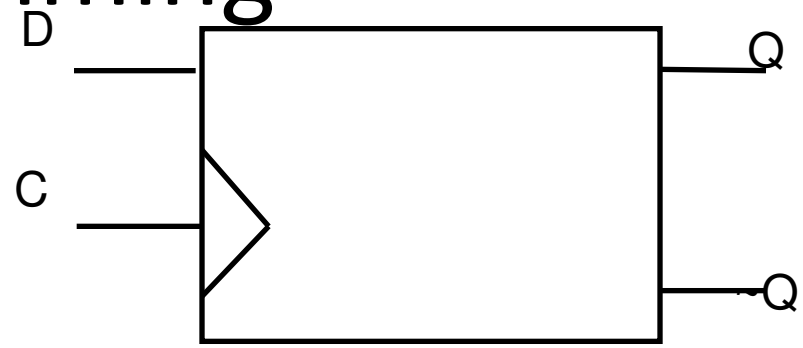
D-type Latch – Timing Review

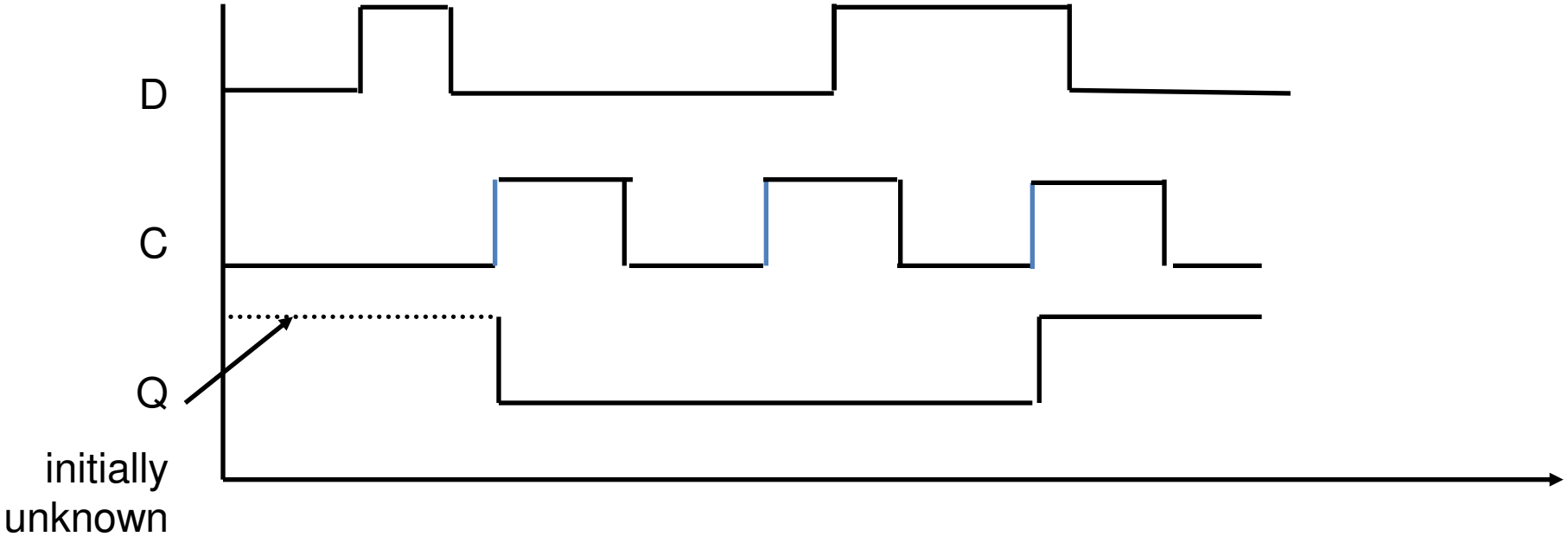


- The high part represents active 1, the low part active 0.



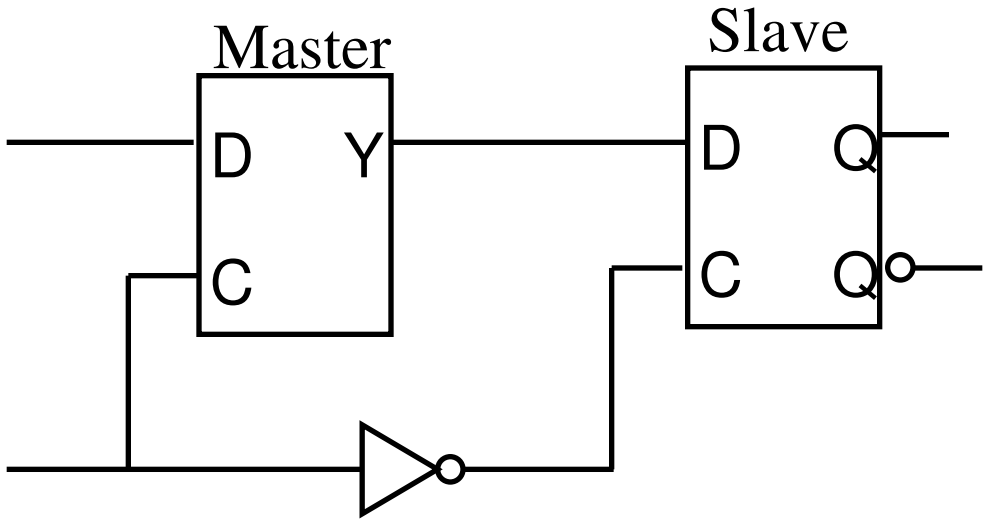
Positive edge-triggered D Flip-flop Timing





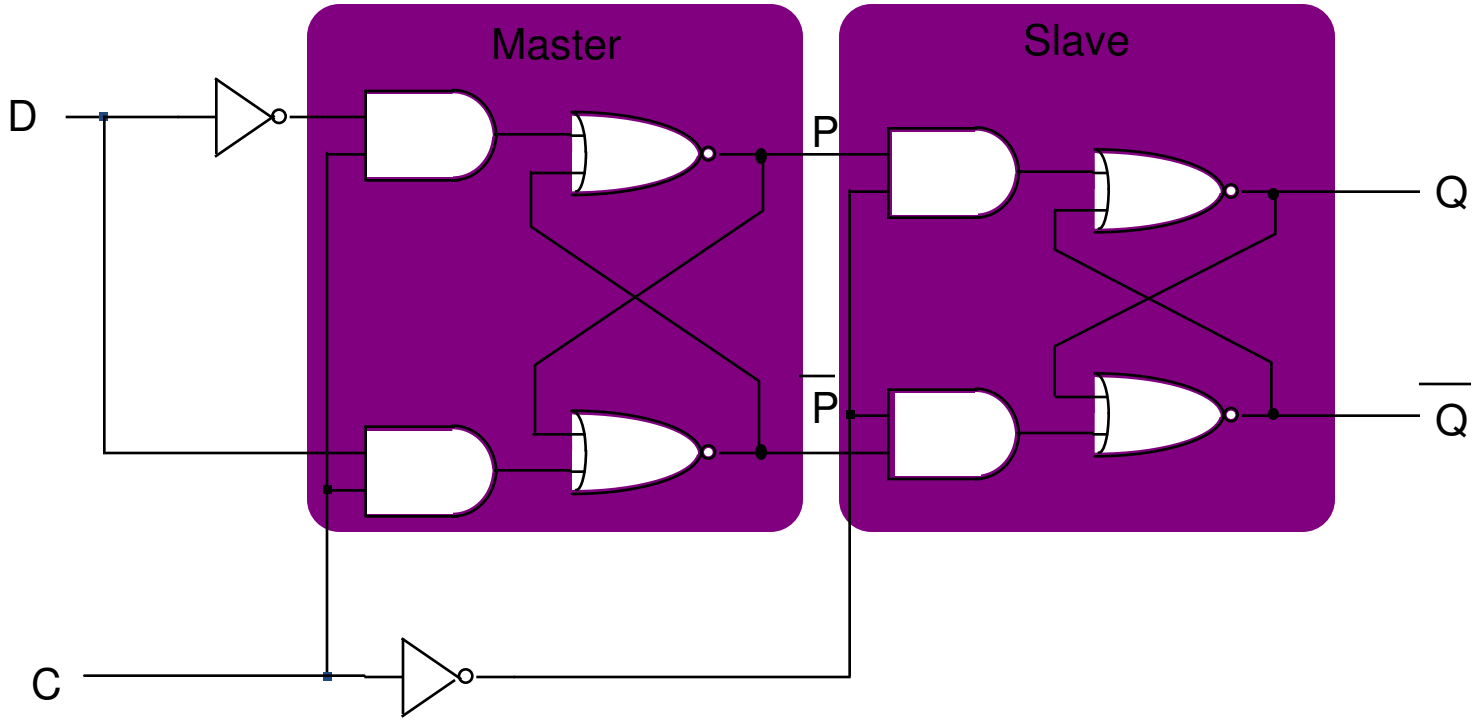
Master Slave D Flip-flop

- A negative edge triggered flip-flop



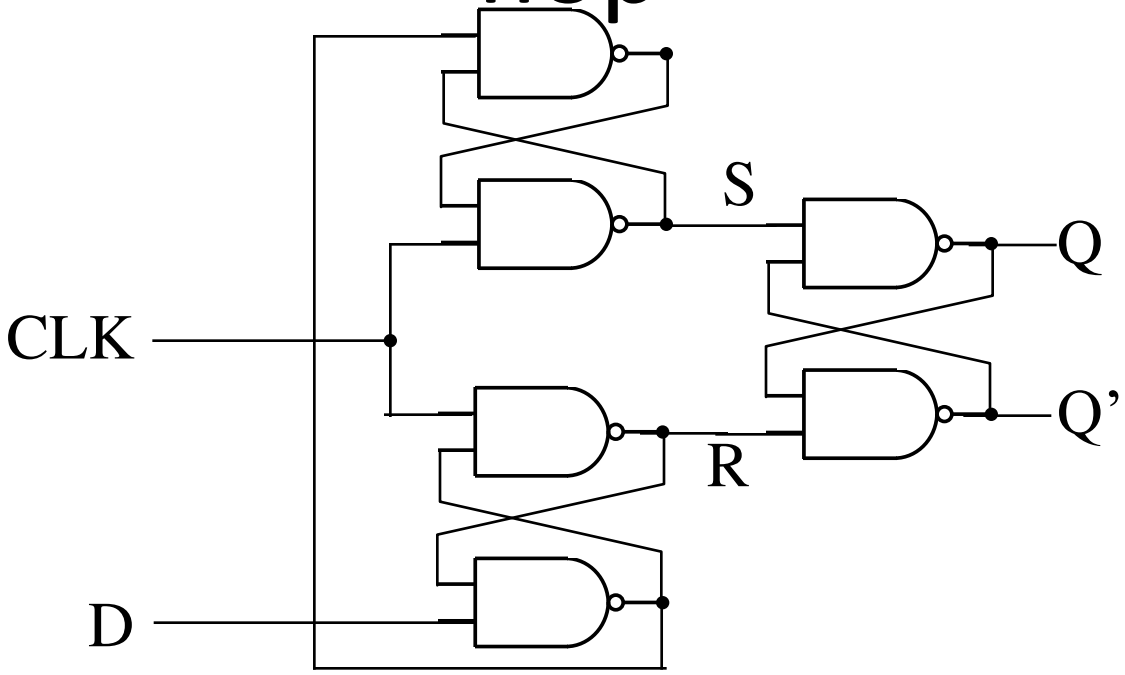
  - On the negative edge of the clock, the master captures the D input and the slave outputs it.

The master-slave Flip-flop



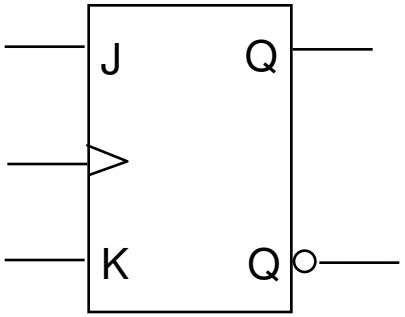
No matter how long the clock pulse, both circuits cannot be active at the same time.

D-type Positive Edge Triggered Flip-flop



- The most economical flip-flop - uses fewest gates

JK Flip-flop

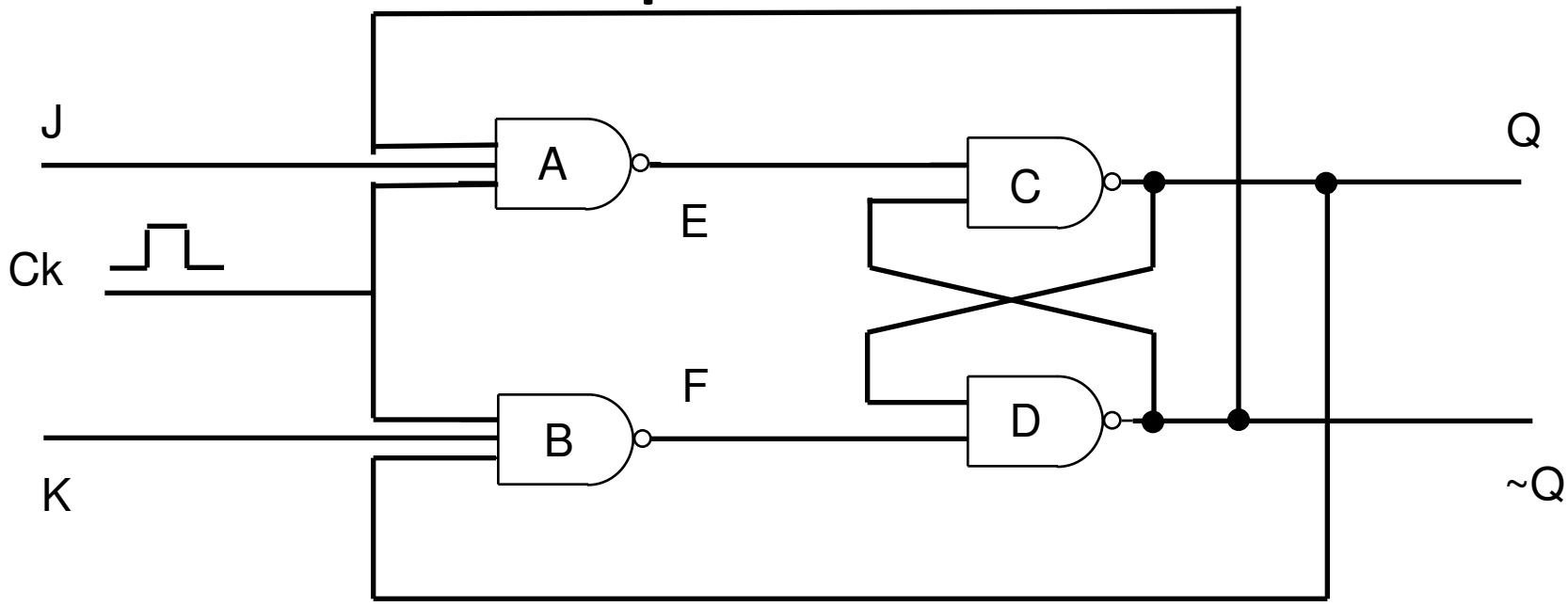


- The most versatile of the flip-flops
- Has two data inputs (J and K)
- Do not have an undefined state like SR flip-flops
  - When J & K both equal 1 the output toggles on the active clock edge
- Most JK flip-flops based on the edge-triggered principle
  - The C column indicates +ve edge triggering (usually omitted)

+ve edge triggered JK flip-flop

J	K	C	Q_{n+1}	
0	0		Q_n	Hold
0	1		0	Reset
1	0		1	Set
1	1		$\overline{Q_n}$	Toggle
X	X	X	Q_n	Hold

Example JK circuit

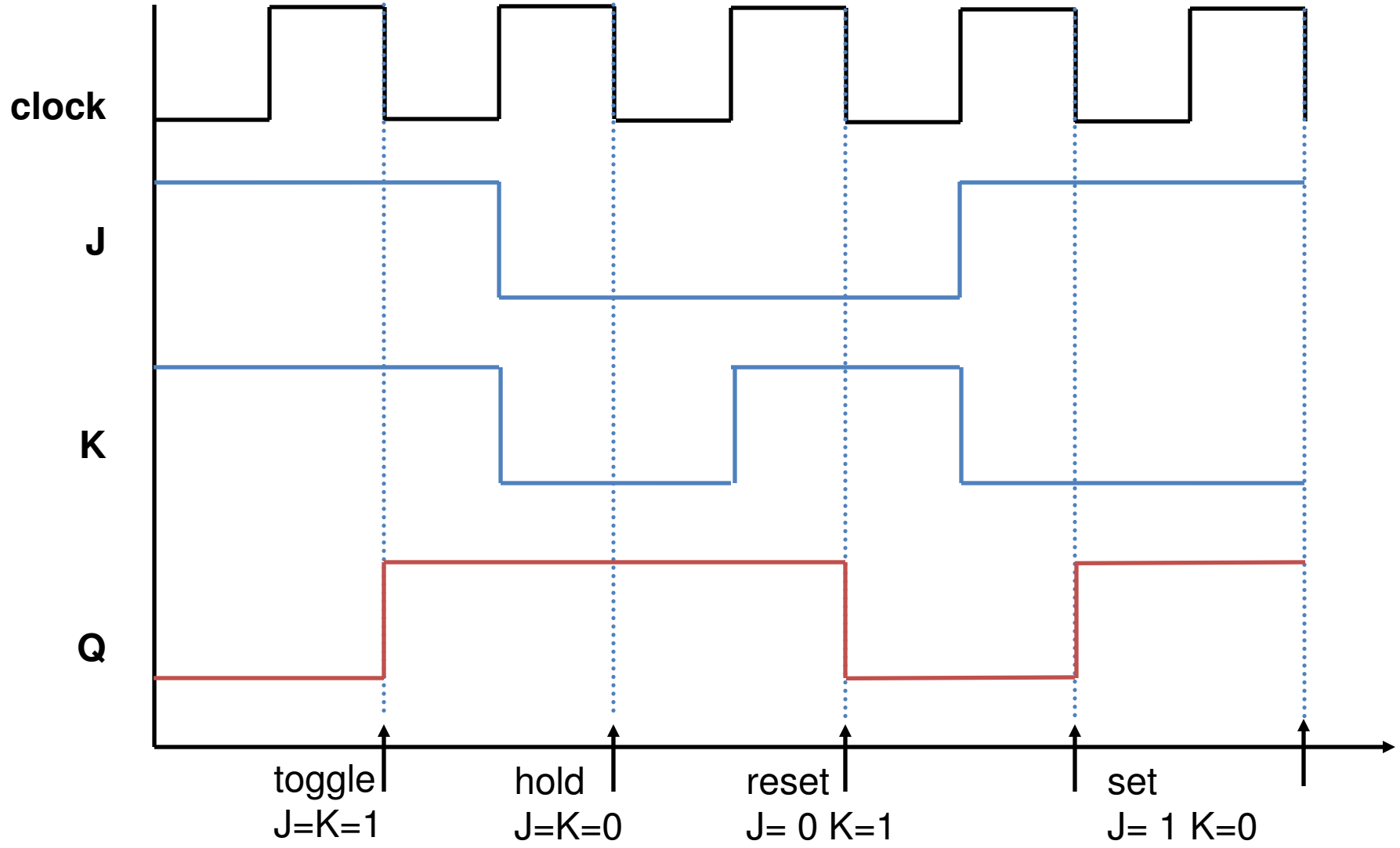


- Assume Q = 0, ~Q = 1, K = 1
- Gate B is disabled (Q = 0, F = 1)
- Make J = 1 to change circuit, when Ck = 1, all inputs to A = 1, E goes to 0, makes Q = 1
- Now Q and F are both 1 so ~Q = 0 and the circuit has toggled.

J	K	C	Q_{n+1}	
0	0		Q_n	Hold
0	1		0	Reset
1	0		1	Set
1	1		$\overline{Q_n}$	Toggle
X	X	X	Q_n	Hold

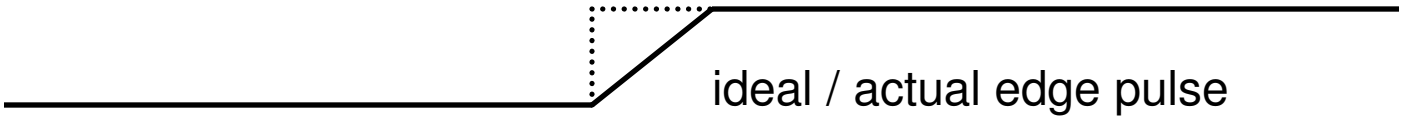
Timing diagram for JK Flip-flop

Negative Edge Triggered

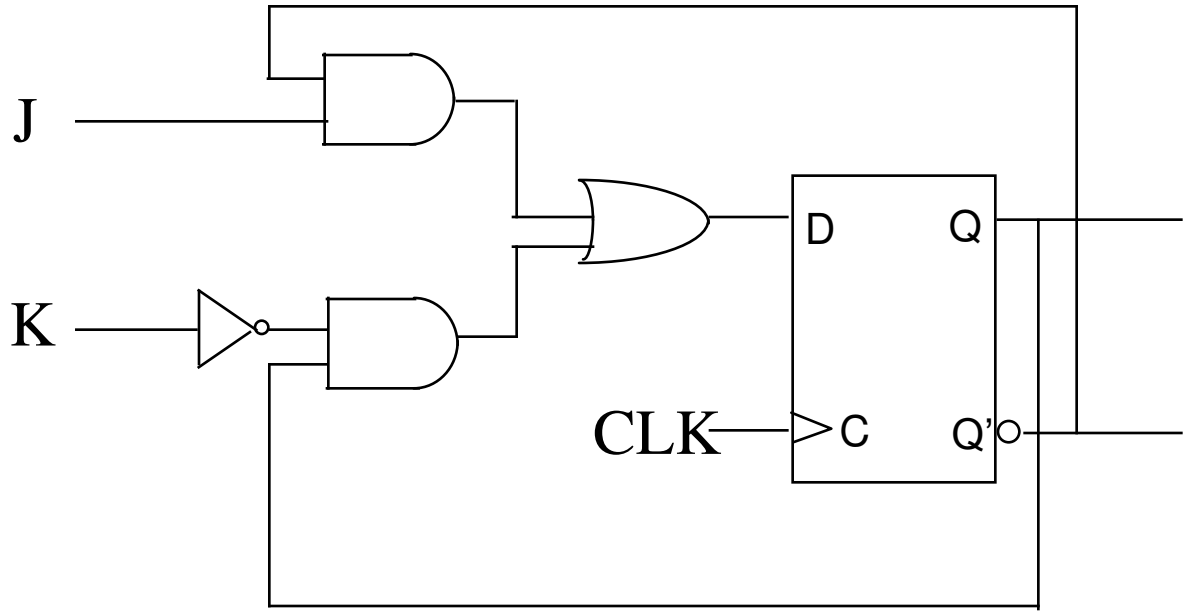


Clock Pulse

- The JK flip flop seems to solve all the problems associated with both inputs at 1.
- However the clock rise/fall is of finite duration.
- If the clock pulse takes long enough, the circuit can toggle.
- For the JK flip flop it is assumed the pulse is quick enough for the circuit to change only once.



JK from D Flip-flop



Summary

- Flip flops are circuits controlled by a clock.
- Triggered on the edge of the pulse to avoid races with both inputs at 1 during the clock pulse.
- Because modern ic's have a small propagation delay races can still occur.
- The master-slave configuration solves this problem by having only master or slave active at any one time.

What you should be able to do

- Explain the difference between combinational and sequential circuits
- Explain the basic operation of SR and D latches.
- Explain the operation of SR and JK flip flops.
- Explain the operation of master-slave flip flops.
- Draw simple timing diagrams for clocked latches and edge-triggered flip flops.
- Define setup and hold times for a transparent latch.