UNIT 4: Dynamic logic circuits

Introduction

- Wide range of static combinational and sequential logic circuits was introduced in the previous chapters.
- Static logic circuits allow versatile implementation of logic functions based on static, or steady-state, behavior of simple nMOS or CMOS structures.
- In other words, all valid output levels in static gates are associated with steady-state operating points of the circuit in question.
- Hence, a typical static logic gate generates its output corresponding to the applied input voltages after a certain time delay, and it can preserve its output level (or state) as long as the power supply is provided.
- This approach, however, may require a large number of transistors to implement a function, and may cause a considerable time delay.

- In high-density, high-performance digital implementations where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits offer several significant advantages over static logic circuits.
- The operation of all dynamic logic gates depends on temporary (transient) storage of charge in parasitic node capacitances, instead of relying on steady-state circuit behavior.
- This operational property necessitates periodic updating of internal node voltage levels, since stored charge in a capacitor cannot be retained indefinitely.
- Consequently, dynamic logic circuits require periodic clock signals in order to control charge refreshing.

- The capability of temporarily storing a state, i.e., a voltage level, at a capacitive node allows us to implement very simple sequential circuits with memory functions.
- The use of common clock signals throughout the system enables us to synchronize the operations of various circuit blocks.
- Dynamic circuit techniques lend themselves well to synchronous logic design.
- Finally, the dynamic logic implementation of complex functions generally requires a smaller silicon area than does the static logic implementation.

 As for the power consumption which increases with the parasitic capacitances, the dynamic circuit implementation in a smaller area will, in many cases, consume less power than the static counterpart, despite its use of clock signals. This simple circuit illustrate most of the basic operational concepts involved in dynamic circuit design



The input pass transistor is being driven by the external periodic clock signal, as follows:

* When the clock is high (CK = 1), the pass transistor turns on. The capacitor *C*, is either charged up, or charged down through the pass transistor MP, depending on the input (D) voltage level. The output (Q) assumes the same logic level as the input.

* When the clock is low (CK = 0), the pass transistor MP turns off, and the capacitor C is isolated from the input D. Since there is no current path from the intermediate node X to either VDD or ground, the amount of charge stored in C during the previous cycle determines the output voltage level Q.

Basic Principles of Pass Transistor Circuits

 The fundamental building block of nMOS dynamic logic circuits, consisting of an Nmos pass transistor driving the gate of another nMOS transistor,



Logic "1" Transfer

- Assume that the soft node voltage is equal to 0 initially, i.e., *Vx(t = 0) = 0 V. A logic " 1"* level is applied to the input terminal, which corresponds to Vin = VOH = VDD.
- Now, the clock signal at the gate of the pass transistor goes from 0 to VDD at t = 0.
- It can be seen that the pass transistor MP starts to conduct as soon as the clock signal becomes active and that MP will operate in saturation throughout this cycle since VDS = VGS.
- Consequently, VD > VGS VT. The circuit to be analyzed for the logic 1 " transfer event can be simplified into an equivalent circuit as shown in Fig.



Fig. Equivalent circuit for the logic "1" transfer event

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Fig. Variation of V as a function of time during logic "I" transfer.

Logic "0" Transfer

- Assume that the soft-node voltage V is equal to a logic "1" level initially, i.e., V(t = 0) = Vm = (VDD- VTn).
- A logic "" level is applied to the input terminal, which corresponds to V.n = 0 V. Now, the clock signal at the gate of the pass transistor goes from 0 to VDD at t = 0.
- The pass transistor MP starts to conduct as soon as the clock signal becomes active, and the direction of drain current flow through MP will be opposite to that during the charge-up (logic " 1 " transfer) event.
- This means that the intermediate node X will now correspond to the drain terminal of MP and that the input node will correspond to its source terminal.
- With VGS = VDD and VDS = Vmax, it can be seen that the pass transistor operates in the linear region throughout this cycle, since VDS < VGS VTn.

- The circuit to be analyzed for the logic "0" transfer event can be simplified into an equivalent circuit as shown in Fig.
- As in the logic "1" transfer case, the depletion load nMOS inverter does not affect this event.



Equivalent circuit for the logic "0" transfer event.



Fig. Variation of Vx as a function of time during logic "0" transfer.



Fig. Charge leakage from the soft node.