UNIT 4:
Dynamic logic circuits

Domino CMOS logic

- Consider the generalized circuit diagram of a domino CMOS logic gate shown in Fig.
- A dynamic CMOS logic stage, such as the one shown in Fig., is cascaded with a static CMOS inverter stage.
- The addition of the inverter allows us to operate a number of such structures in cascade, as explained in the following.

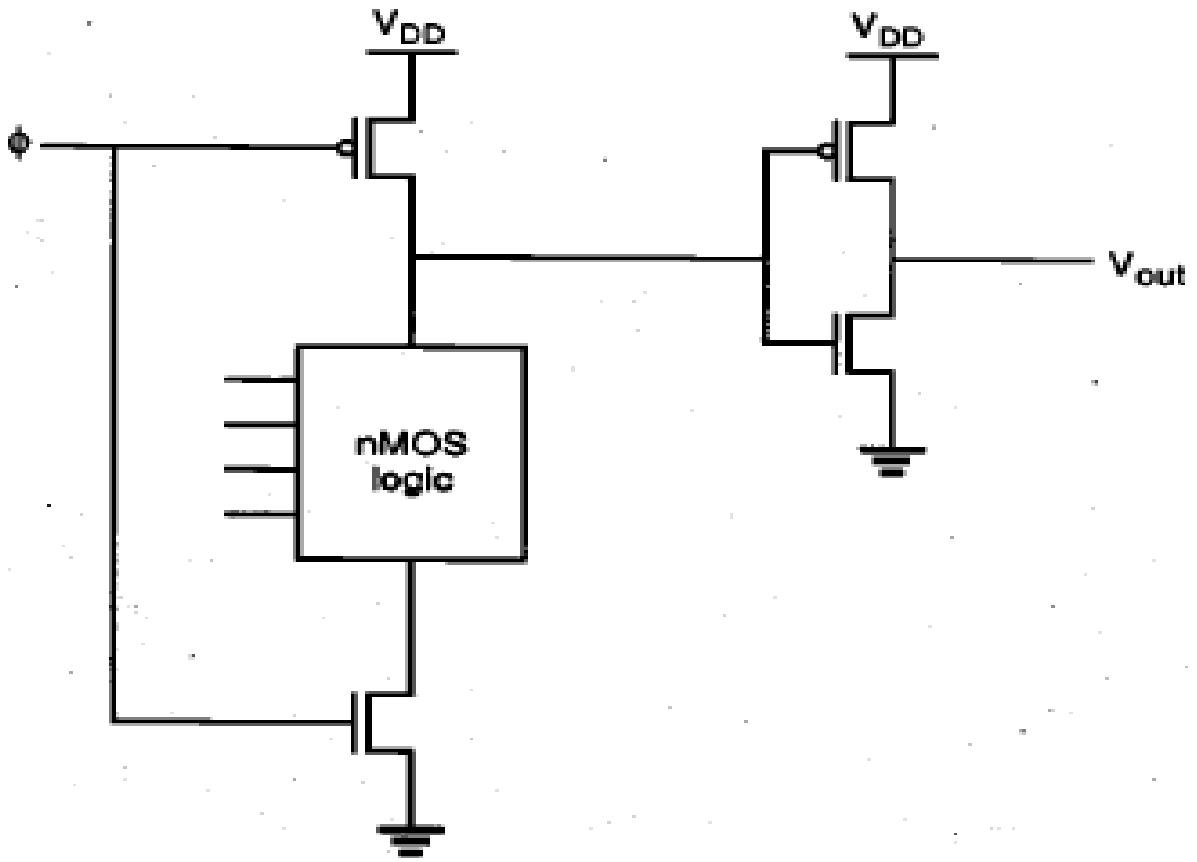

Fig. Generalized circuit diagram of a domino CMOS logic gate

- During the precharge phase (when CK = 0), the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low.

- When the clock signal rises at the beginning of the evaluation phase, there are two possibilities:

- The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry (1 to 0 transition), or it remains high.
- Consequently, the inverter output voltage can also make at most one transition during the
- evaluation phase, from 0 to 1. Regardless of the input voltages applied to the dynamic
- CMOS stage, it is not possible for the buffer output to make a 1 to 0 transition during the
- evaluation phase.

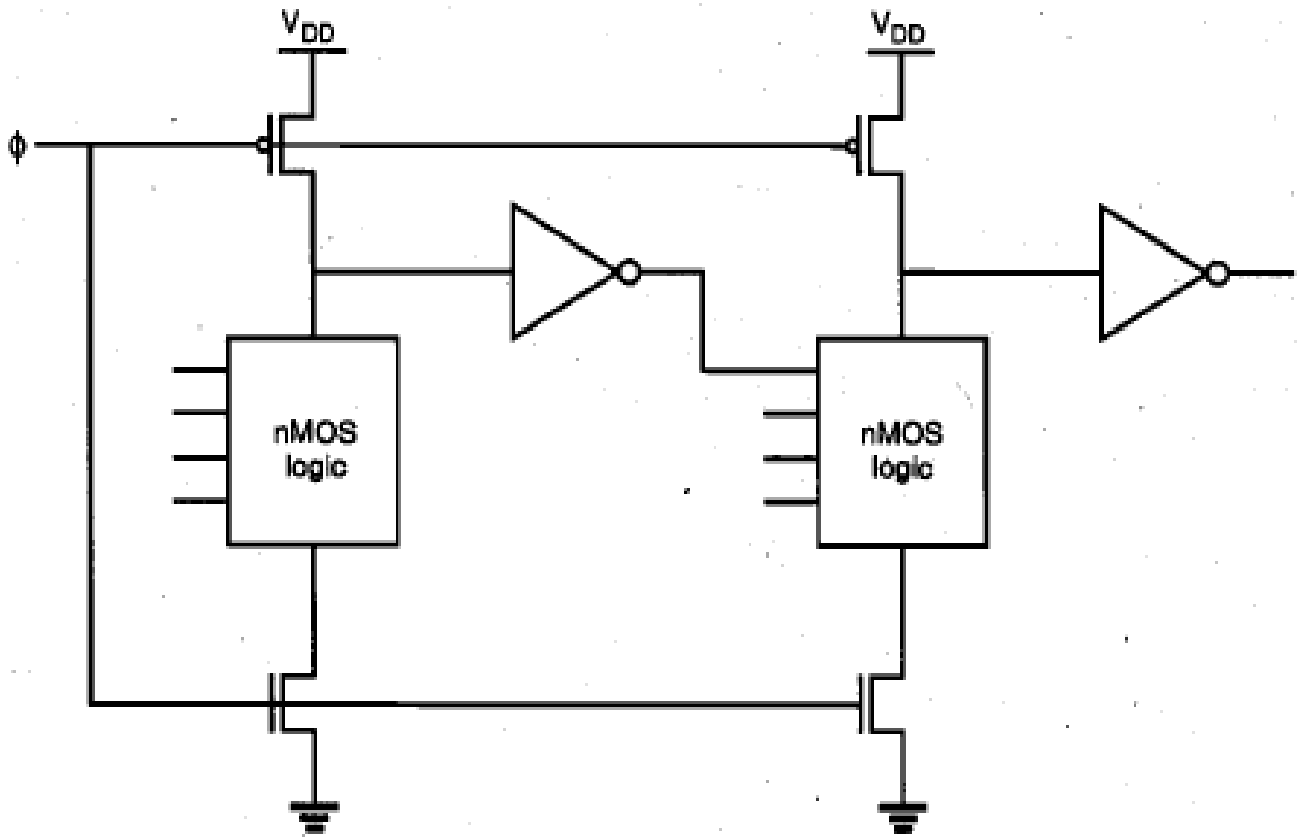

Fig. Cascaded domino CMOS logic gates.

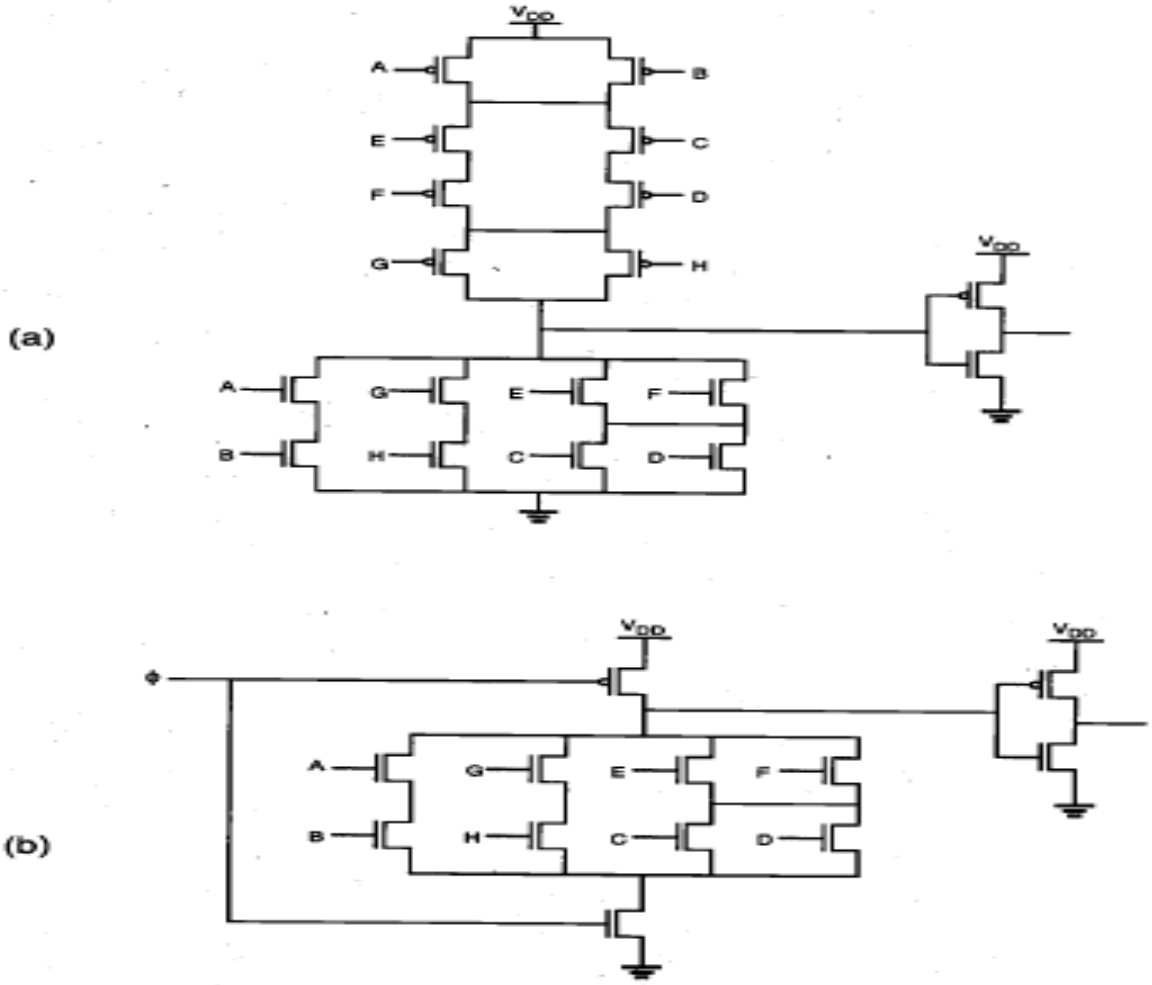

Fig. (a) An 8-input complex logic gate, realized using conventional CMOS logic and (b) domino CMOS logic.

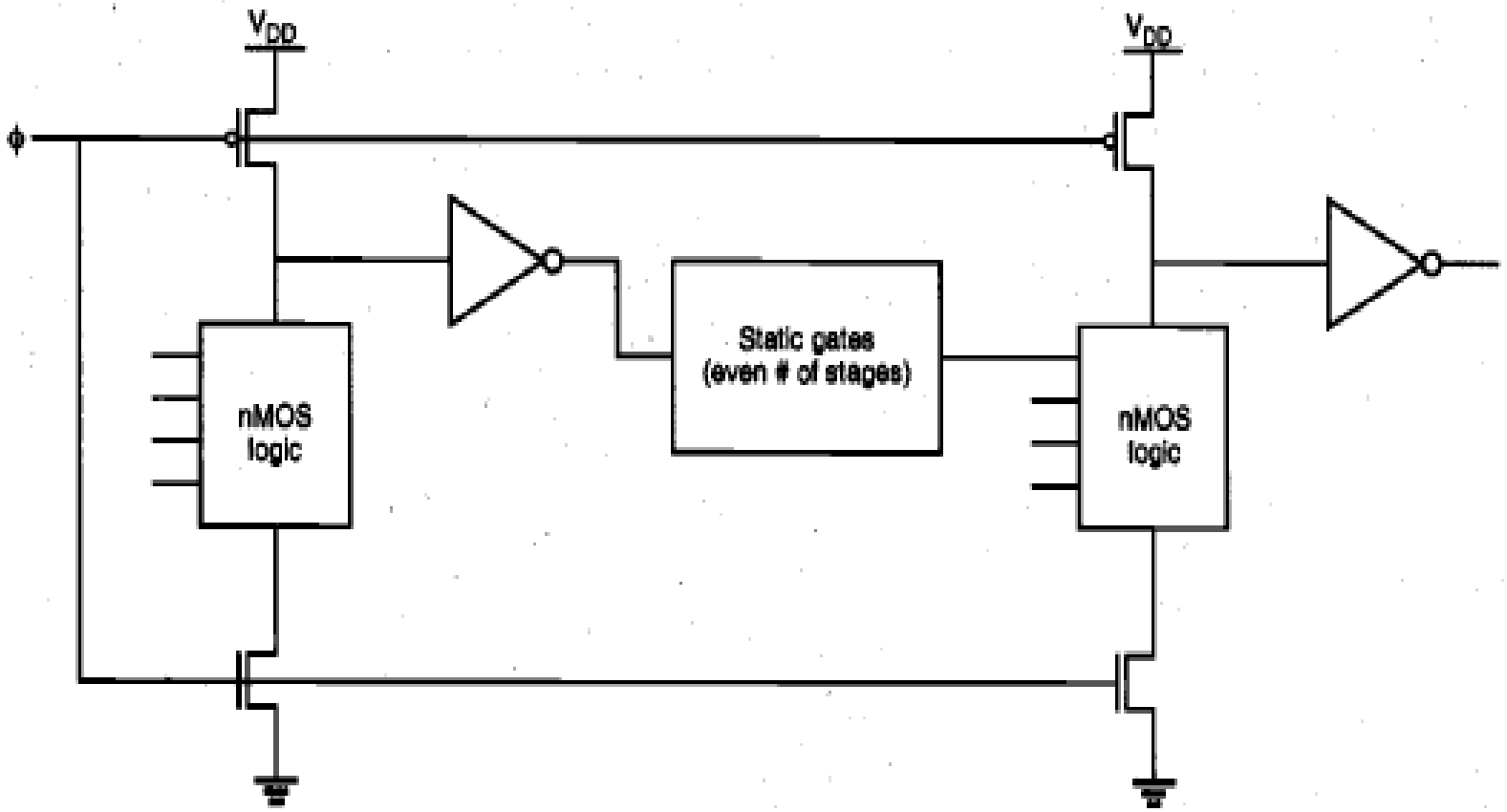

Fig. Cascading domino CMOS logic gates with static CMOS logic gates

- Domino CMOS logic gates allow a significant reduction in the number of transistors required to realize any complex Boolean function.

- The implementation of the 8-input Boolean function, Z = *AB + (C + D)(C + D) + GH, using standard CMOS and domino* CMOS, is shown in Fig., where the reduction of circuit complexity is obvious.

- The distribution of the clock signal within the system is quite straightforward, since a single clock can be used to precharge and evaluate any number of cascaded stages, as long as the signal propagation delay from the first stage to the last stage does not exceed the time span of the evaluation phase.

- The limitation is that the number of inverting static logic stages in cascade must be even, so that the inputs of the next domino CMOS stage experience only 0 to 1 transitions during the evaluation.

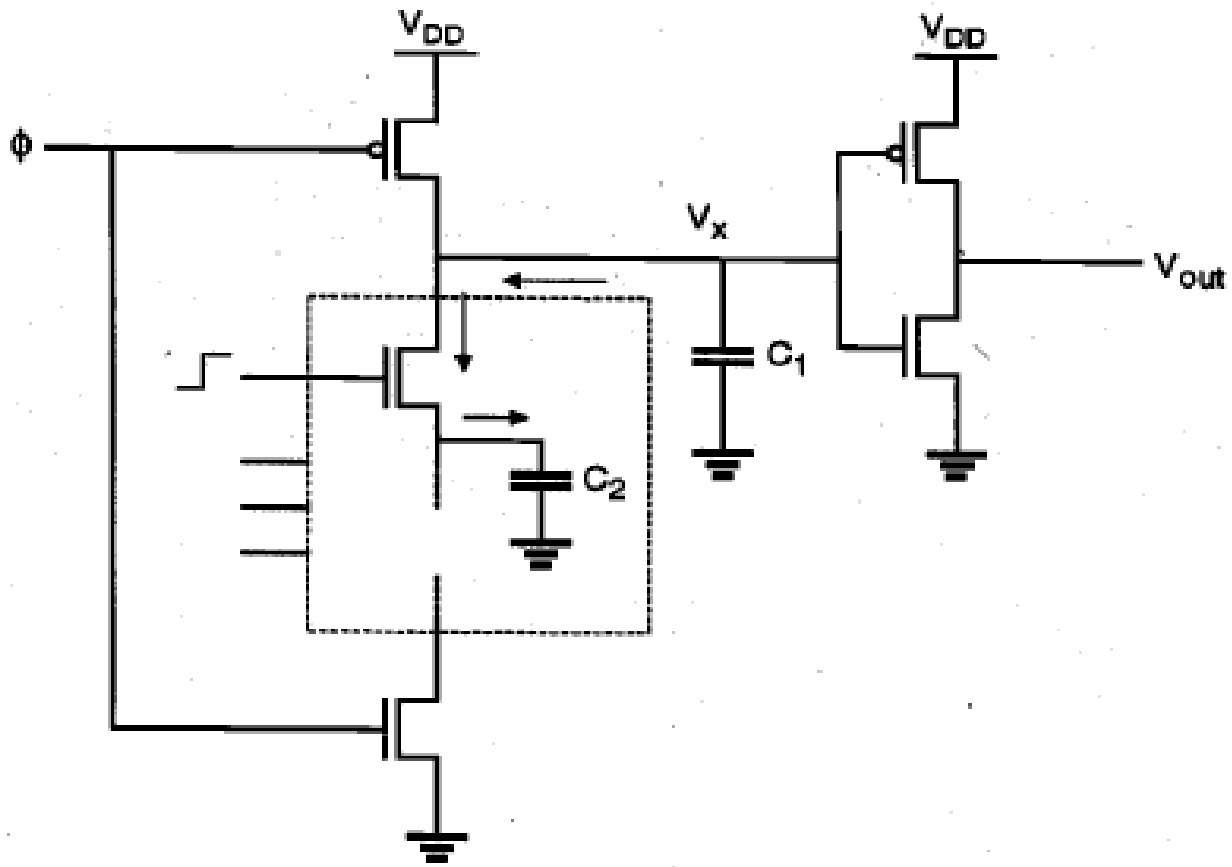

Fig. Charge sharing between the output capacitance C and an intermediate node capacitance C2 during the evaluation cycle may reduce the output voltage level.

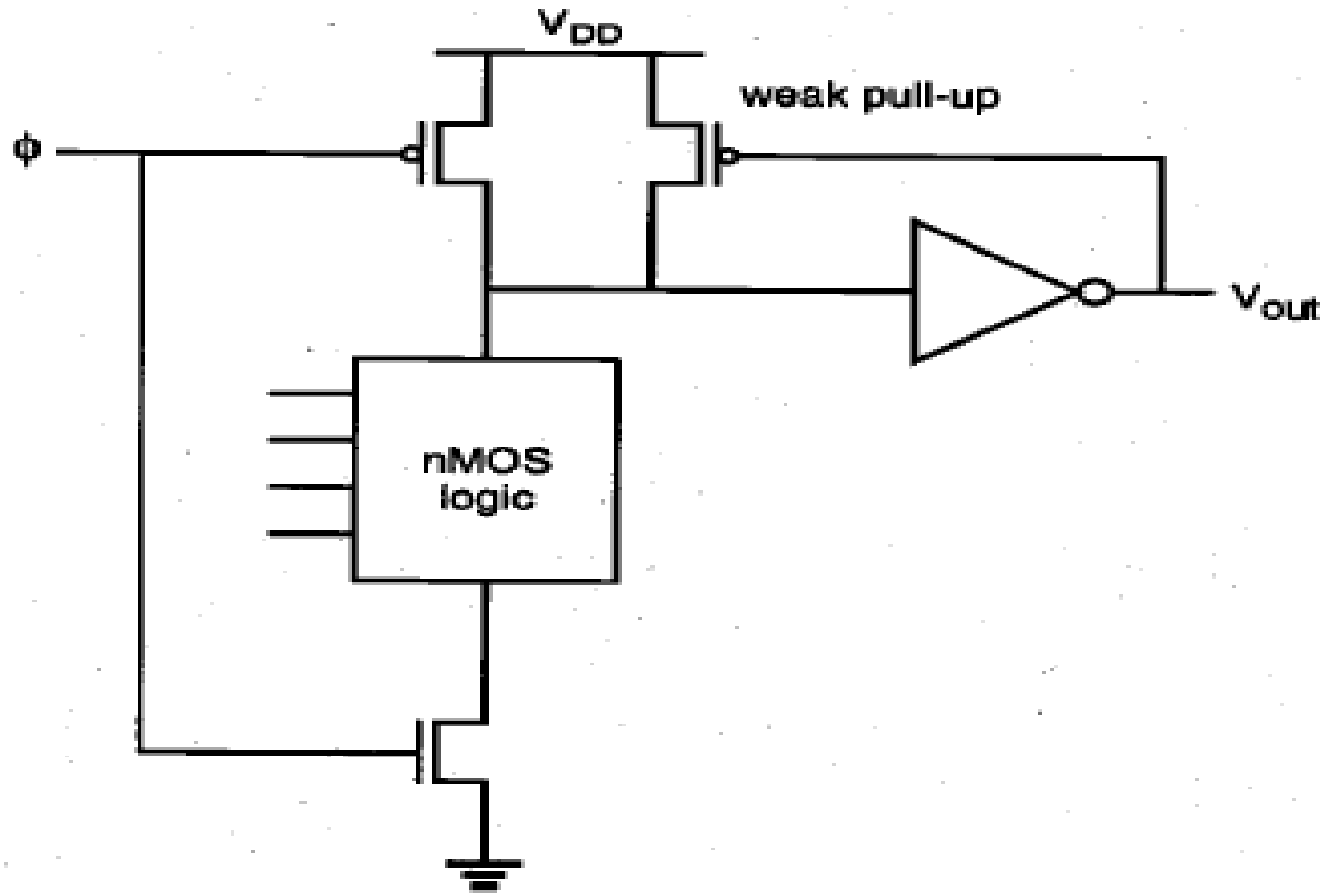

Fig. A weak pMOS pull-up device in a feedback loop can be used to prevent the loss of output voltage level due to charge sharing.