UNIT 4:
Dynamic logic circuits

Semiconductor memories: Introduction

- Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems.

- The amount of memory required in a particular system depends on the type of application, but, in general, the number of transistors utilized for the information (data) storage function is much larger than the number of transistors used in logic operations and for other purposes.

- The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities.

- Thus, the maximum realizable data storage capacity of single-chip semiconductor memory arrays approximately doubles every two years.
- On-chip memory arrays have become widely used subsystems in many VLSI circuits, and commercially available single-chip read/write memory capacity has reached 64 megabits.

- This trend toward higher memory density and larger storage capacity will continue to push the leading edge of digital system design.

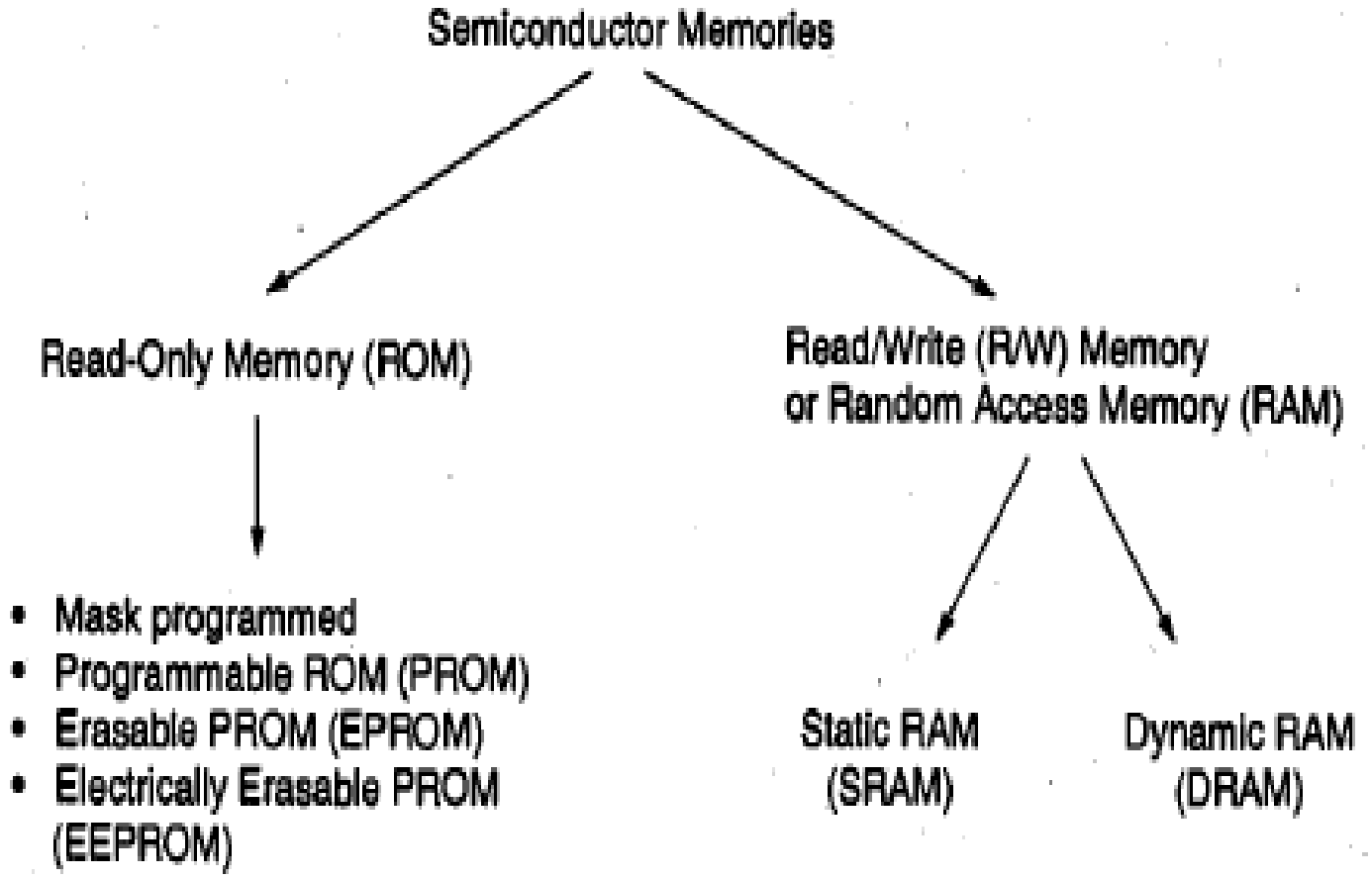
- The area efficiency of the memory array, i.e., the number of stored data bits per unit area, is one of the key design criteria that determine the overall storage capacity and, hence, the memory *cost per bit. Another important issue is the memory access time, i.e.,* the time required to store and/or retrieve a particular data bit in the memory array.

- Memory circuits are generally classified according to the type of data storage and the type of data access. *Read-Only Memory (ROM) circuits allow, as the name implies, only* the retrieval of previously stored data and do not permit modifications of the stored information contents during normal operation.

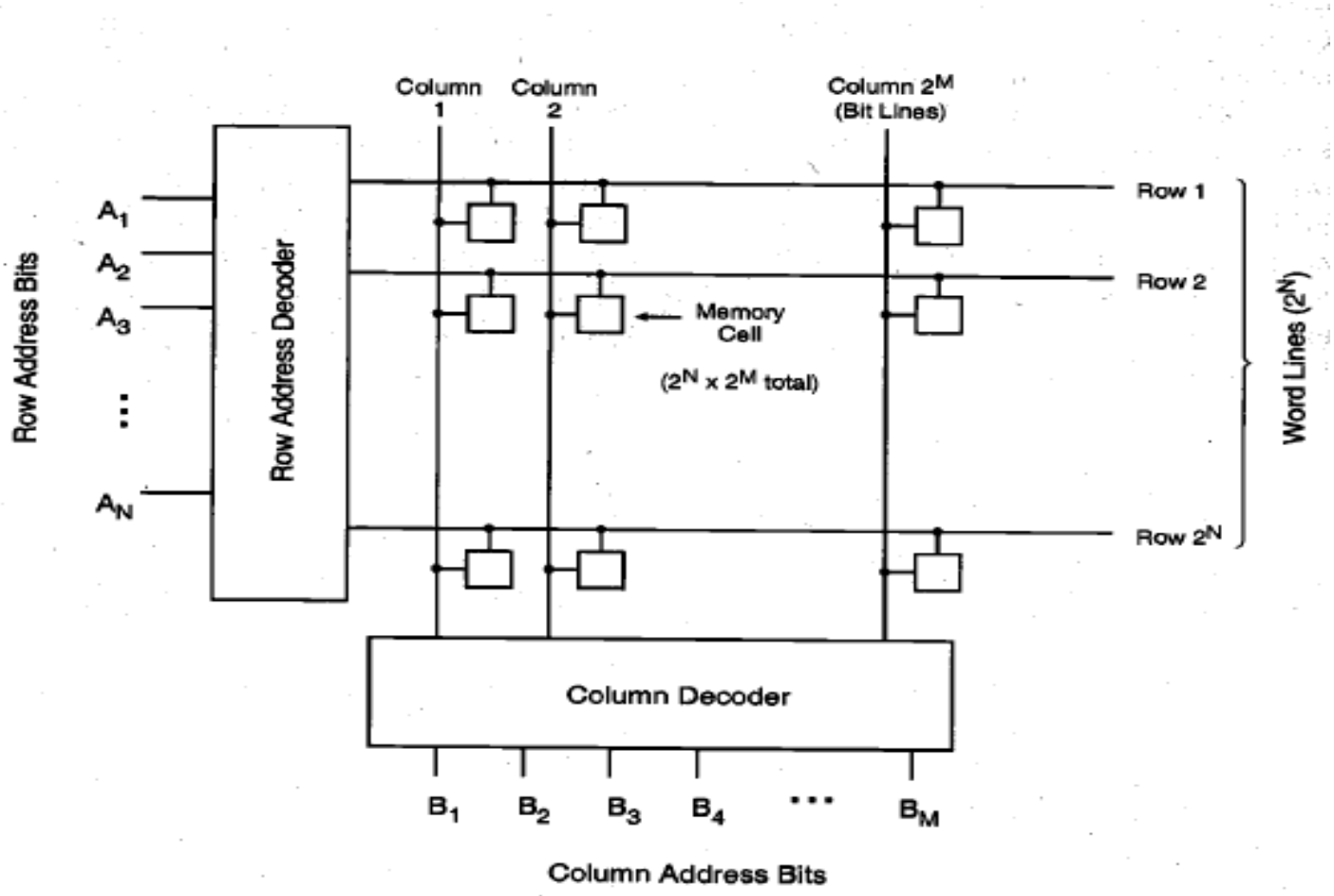
- ROMs are *non-volatile memories, i.e., the* data storage function is not lost even when the power supply voltage is off.

- Depending on the type of data storage (data write) method, ROMs are classified as mask-programmed ROMs, Programmable ROMs (PROM), Erasable PROMs (EPROM), and Electrically Erasable PROMs (EEPROM).

Overview of semiconductor memory



Typical random-access memory array organization



- To access a particular memory cell, i.e., a particular data bit in this array, the corresponding bit line and the corresponding word line must be activated (selected).

- The row and column selection operations are accomplished by row and column *decoders,* respectively.

- The row decoder circuit selects one out of 2N word lines according to an *Nbit* row address, while the column decoder circuit selects one out of 2M bit lines according to an M-bit column address.

- Once a memory cell or a group of memory cells are selected in this fashion, a data read and/or a data write operation may be performed on the selected single bit or multiple bits on a particular row.

- The column decoder circuit serves the double duties of selecting the particular columns and routing the corresponding data content in a selected row to the output.

- We can see from this simple discussion that individual memory cells can be accessed for data read and/or data write operations in random order, independent of their physical locations in the memory array.

- Thus, the array organization examined here is called a *Random Access Memory (RAM) structure.*

- *Notice that this organization can be used for* both read-write memory arrays and read-only memory arrays.

- In the following sections, however, we will use the acronym RAM specifically for read-write memories, because it is the universally accepted abbreviation for this particular type of memory array.