UNIT 4:
Dynamic logic circuits

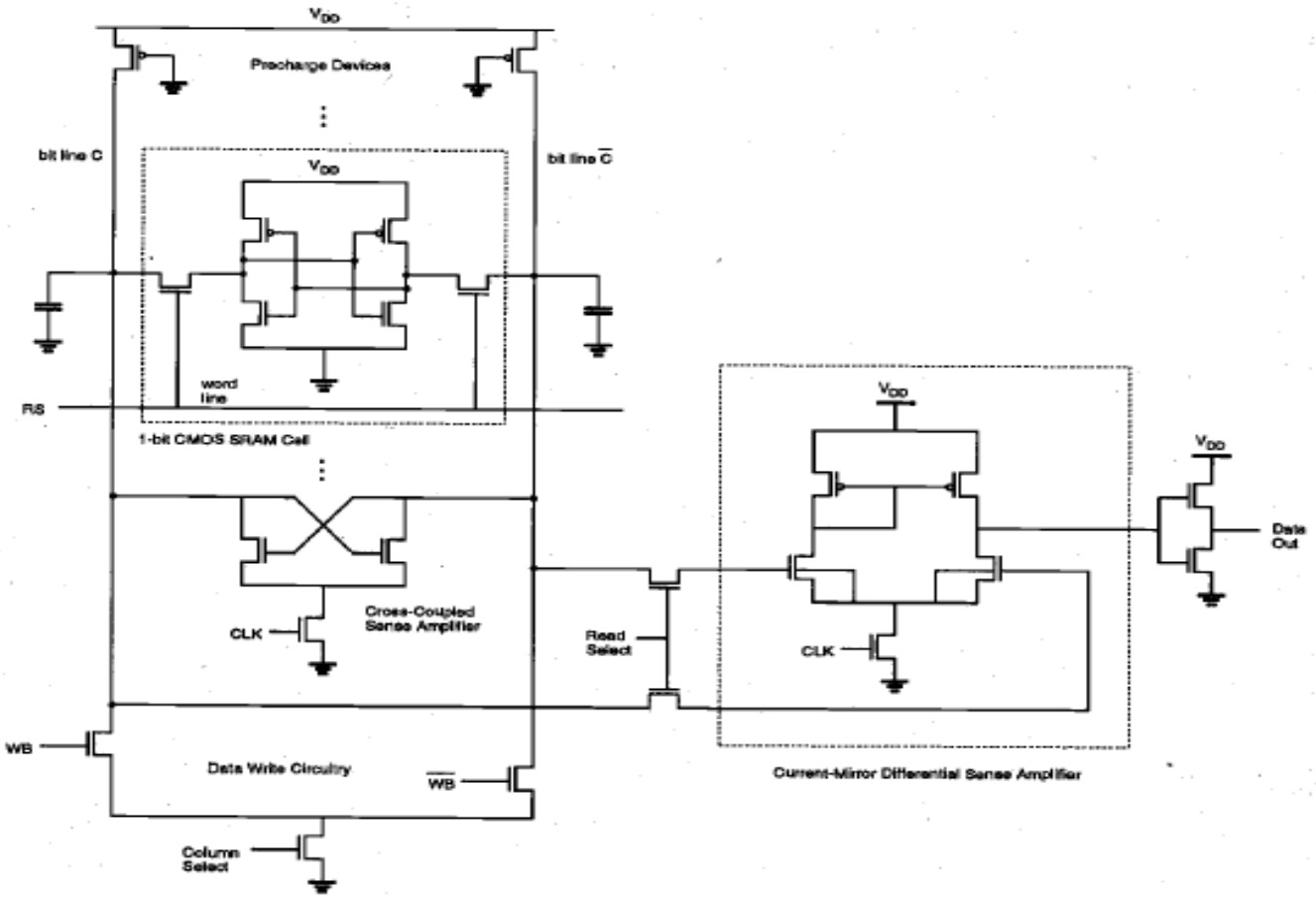
DRAM

- All of the static RAM cells examined in the previous section consist of a two-inverter latch circuit, which is accessed for "read" and "write" operations via two pass transistors.

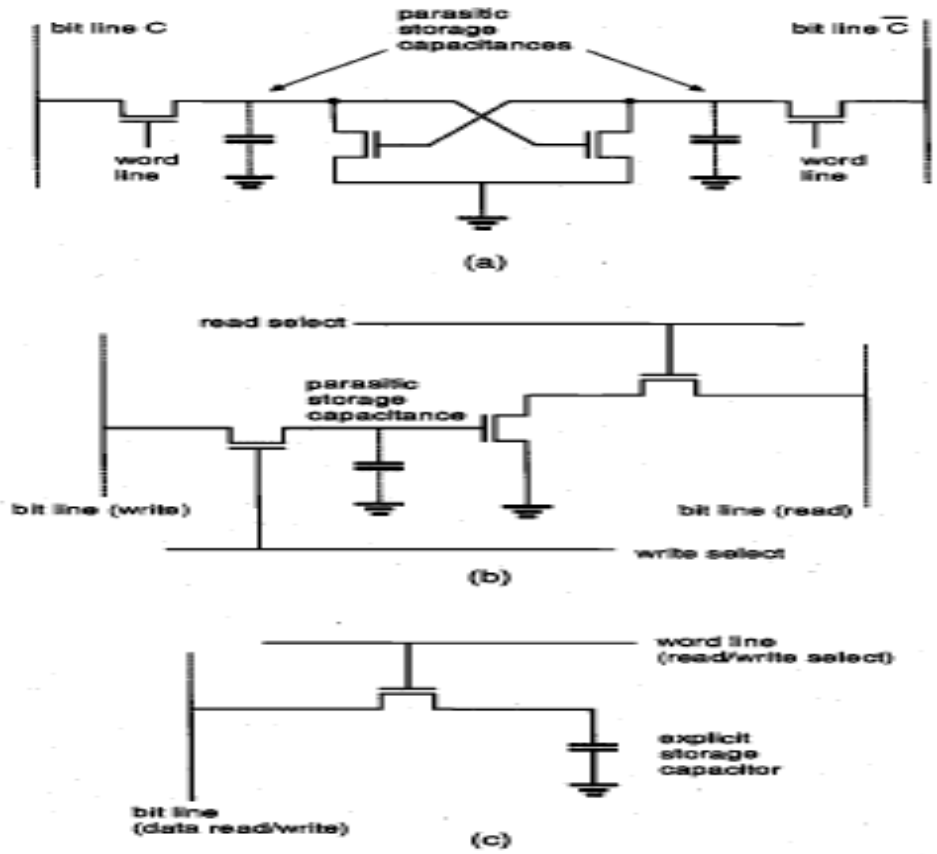
- Consequently, the SRAM cells require four to six transistors per bit, and four to five lines connecting to each cell, including the power and ground connections. To satisfy these requirements, a substantial silicon area must be reserved for each memory cell.

- In addition, most SRAM cells have non-negligible standby (static) power dissipation, with the exception of the full CMOS SRAM cell.

Complete circuit diagram of a CMOS static RAM column with data write and data read circuitry



- Figure shows some of the steps in the historical evolution of the DRAM cell.
- The four-transistor cell shown in Fig. is the simplest and one of the earliest dynamic memory cells.
- This cell is derived from the six-transistor static RAM cell by removing the load devices.
- The cell has in fact two storage nodes, i.e., the parasitic oxide and diffusion capacitances of the nodes indicated in the circuit diagram.
- Since no current path is provided to the storage nodes for restoring the charge being lost to leakage, the cell must be refreshed periodically.
- It is obvious that the four-transistor dynamic RAM cell can have only a marginal area advantage over the six-transistor SRAM cell.



Various configurations of the dynamic RAM cell. (a) Four-transistor DRAM cell with two storage nodes. (b) Three-transistor DRAM cell with two bit lines and two word lines. (c) One-transistor DRAM cell with one bit line and one word line.

Three-Transistor DRAM Cell

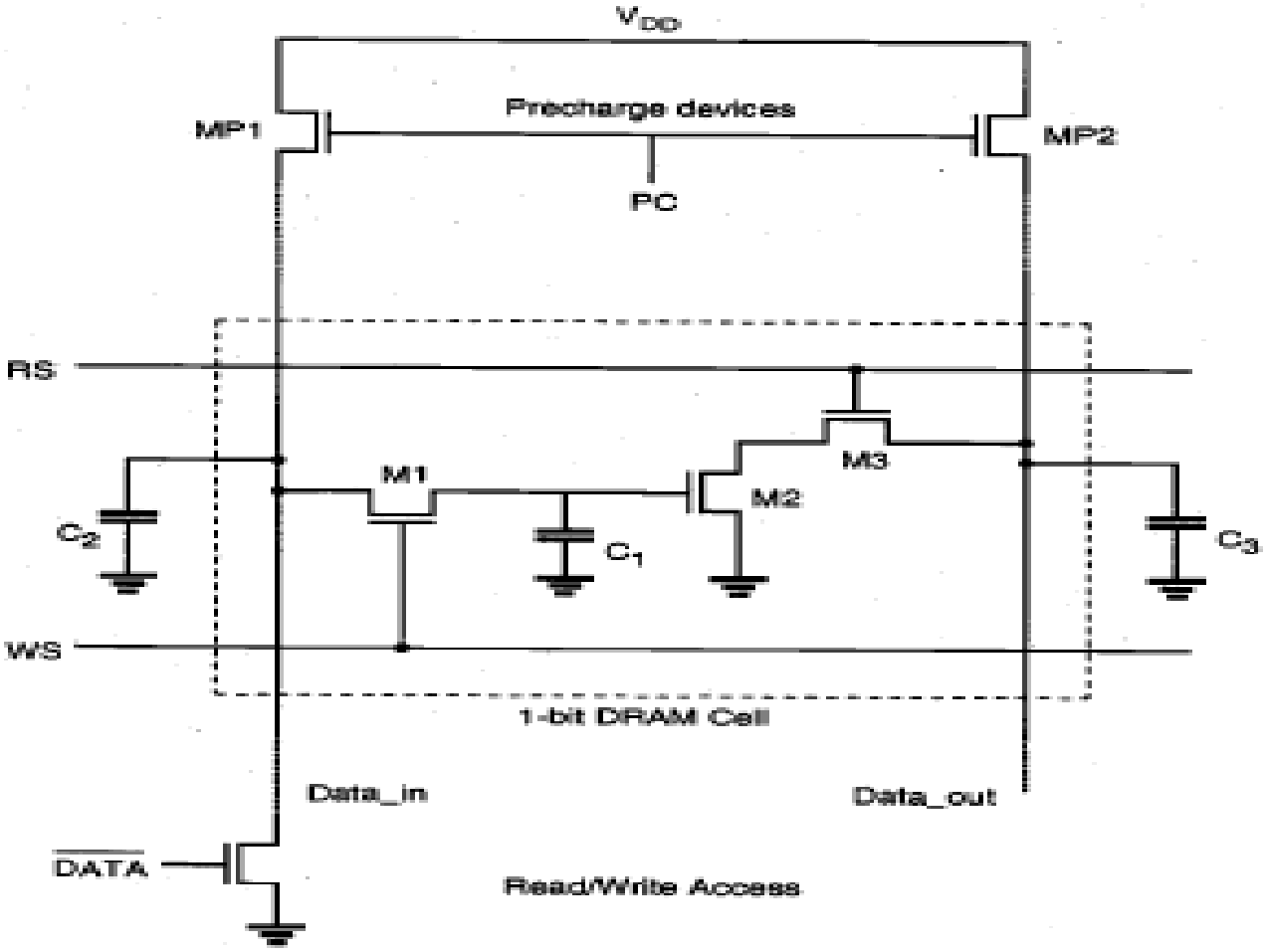
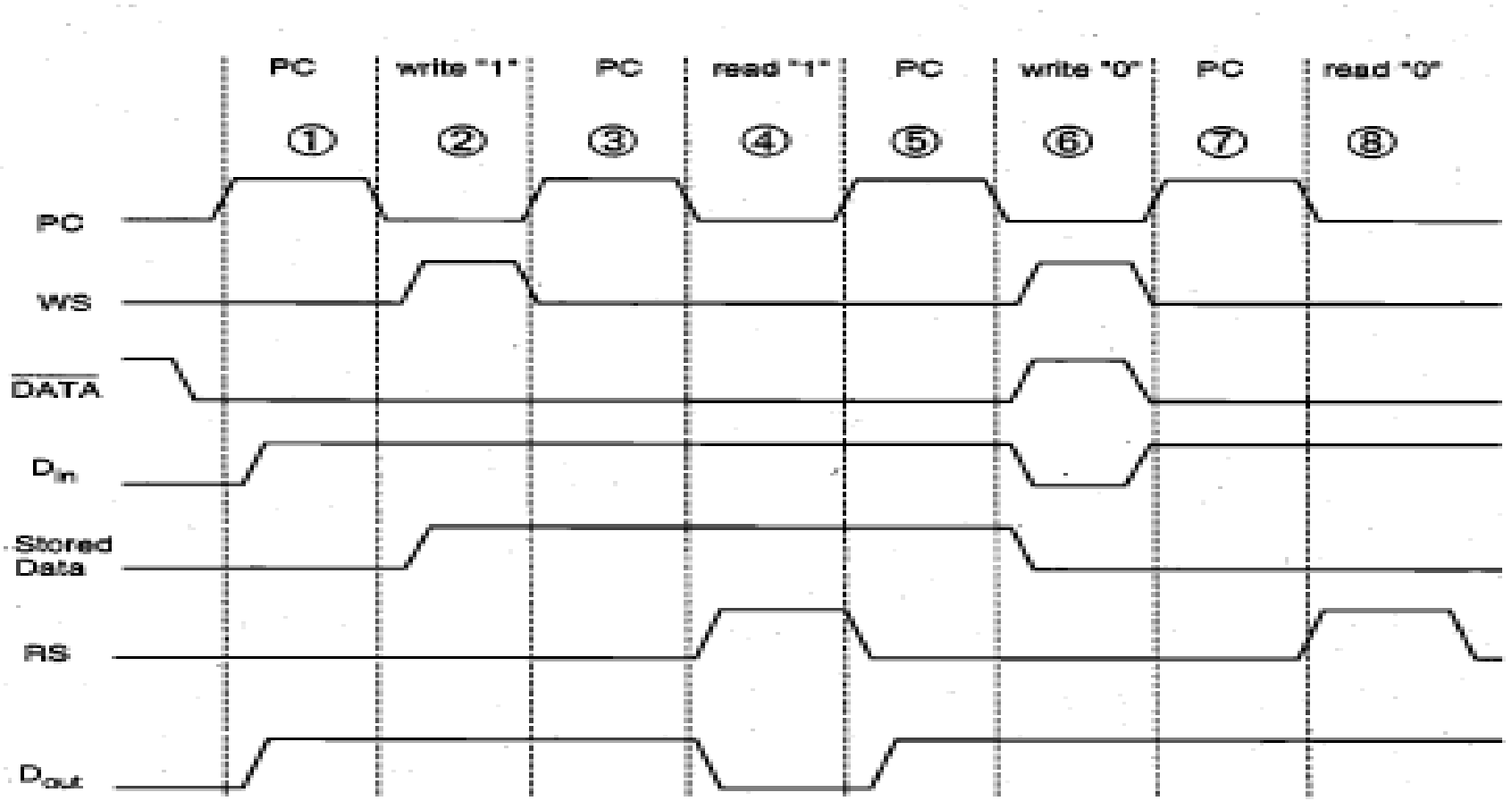


Fig. Typical voltage waveforms associated with the 3-T DRAM cell during four consecutive operations: write "1," read "1," write "0," and read "O."



SRAM

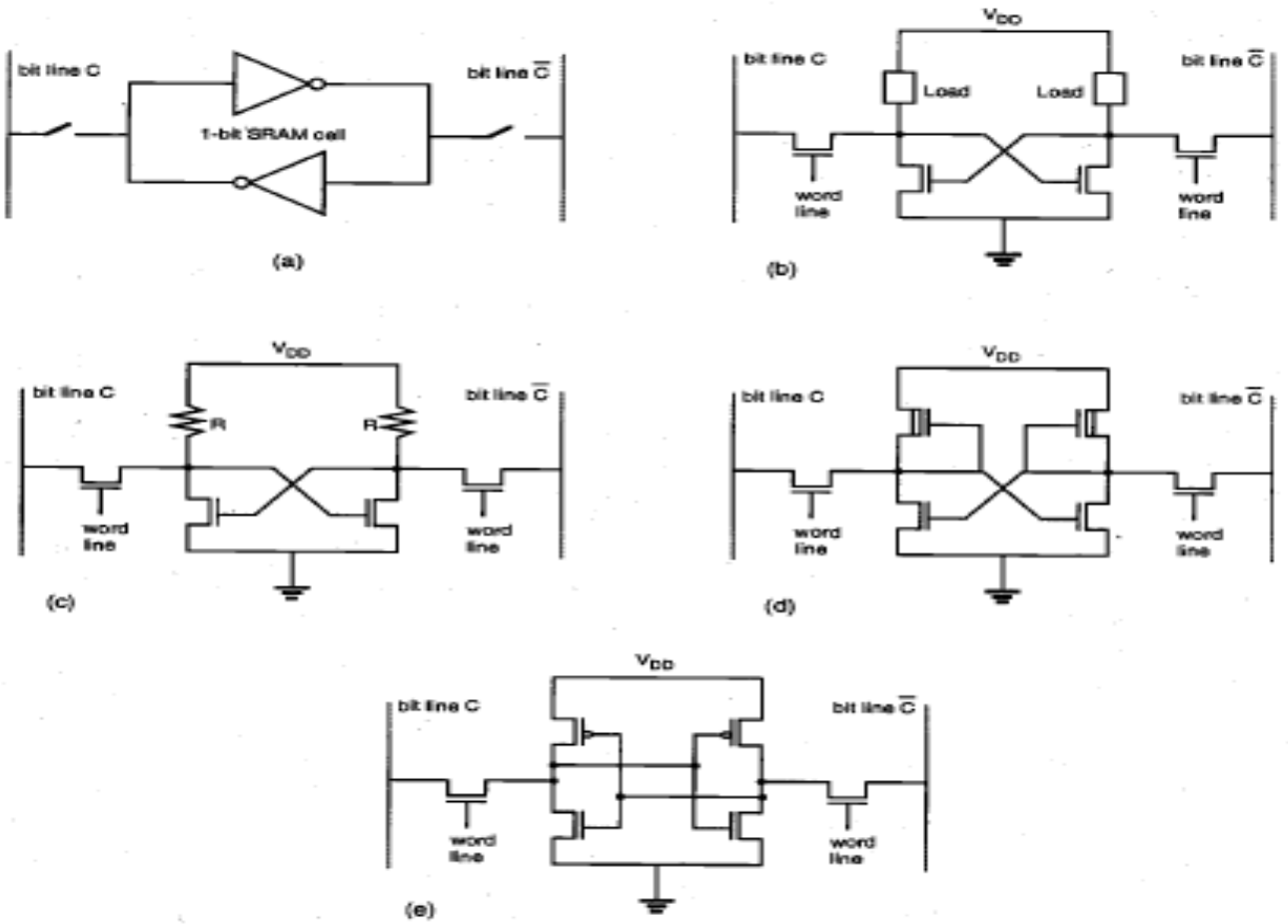
- Read-write (R/W) memory circuits are designed to permit the modification (writing) of data bits to be stored in the memory array, as well as their retrieval (reading) on demand.

- The memory circuit is said to be *static if the stored* data can be retained indefinitely (as long as a sufficient power supply voltage is provided), without any need for a periodic refresh operation.

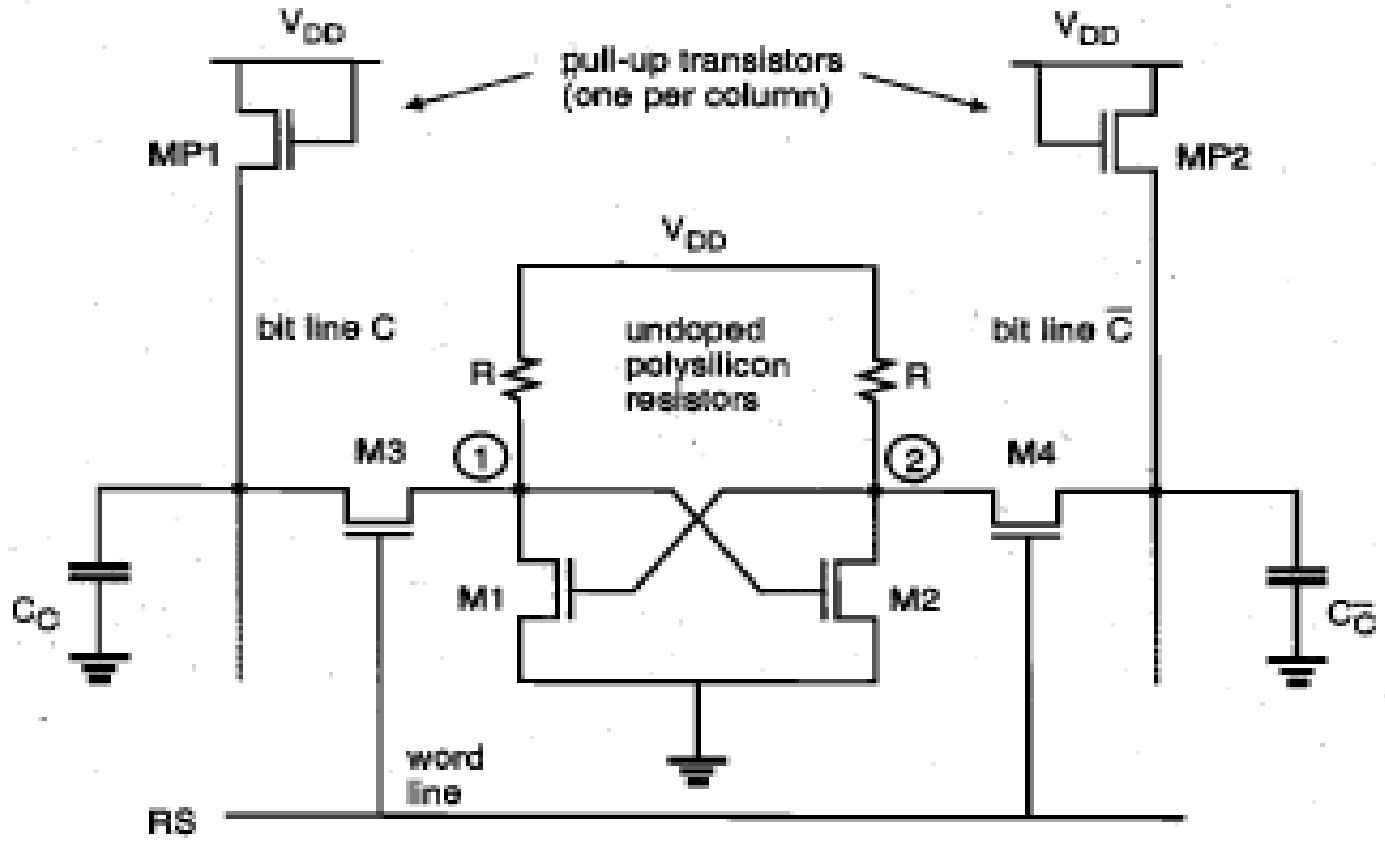
- The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states).

- Depending on the preserved state of the two-inverter latch circuit, the data being held in the memory cell

Various configurations of the static RAM cell. (a) Symbolic representation of the two-inverter latch circuit with access switches. (b) Generic circuit topology of the MOS static RAM cell. (c) Resistive-load SRAM cell. (d) Depletion-load nMOS SRAM cell. (e) Full CMOS SRAM cell.



SRAM Operation Principles



Circuit topology of the CMOS SRAM cell