UNIT 4:
Dynamic logic circuits

ROM

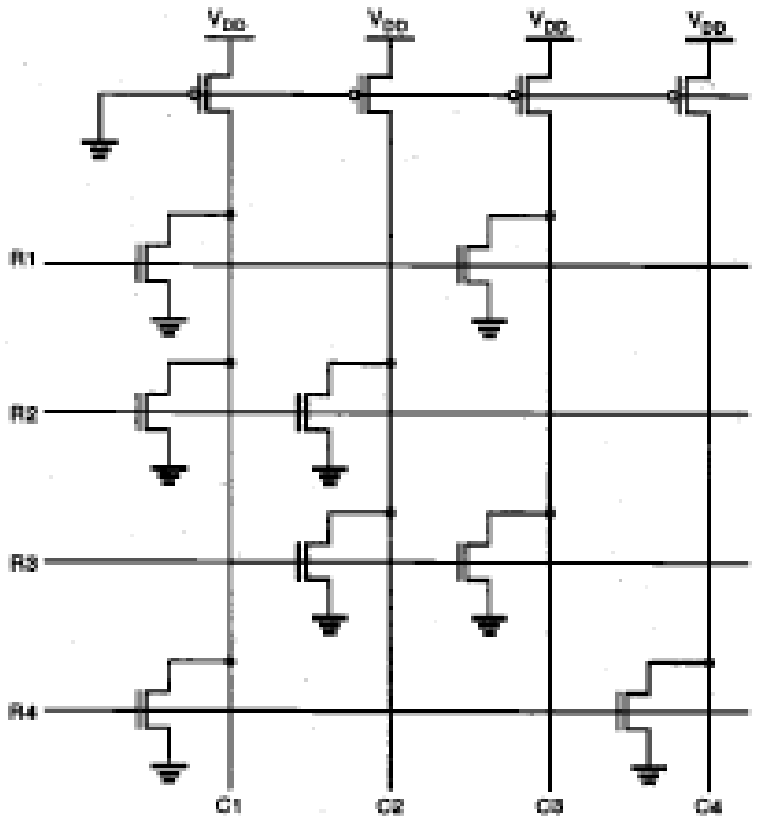
- The read-only memory array can also be seen as a simple combinational Boolean network which produces a specified output value for each input combination,i.e., for each address.

- Storing binary information at a particular address location can be achieved by the presence or absence of a data path from the selected row (word line) to the selected column (bit line), which is equivalent to the presence or absence of a device at that particular location.

- In the following, we will examine two different implementations for MOS ROM arrays.

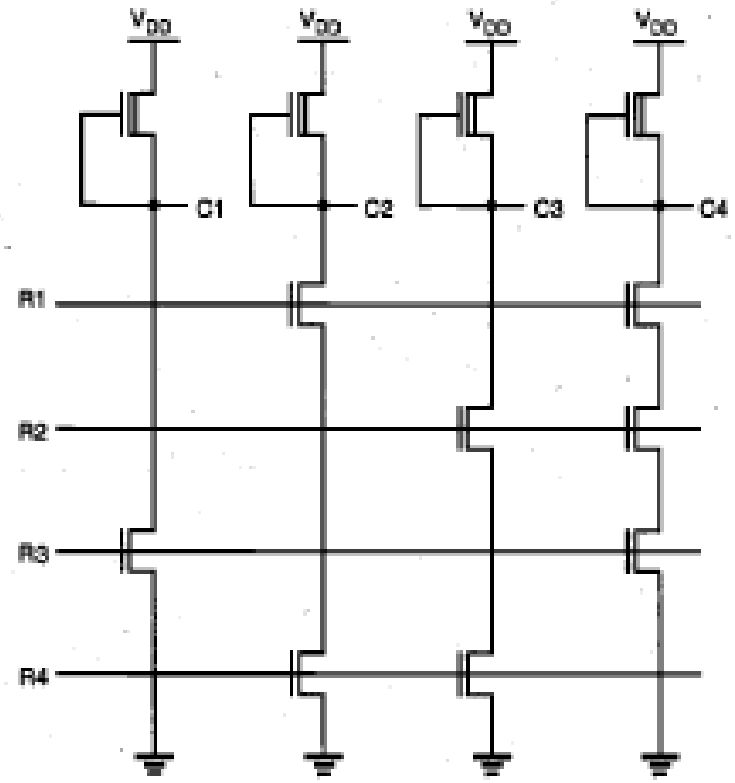
- In fig. the 4-bit x4-bit memory array is shown. Here, each column consists of a pseudo-nMOS NOR gate driven by some of the row signals, i.e., the word lines.

Example of a 4-bit x 4-bit NOR-based ROM array



R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

A 4-bit x 4-bit NAND-based ROM array.



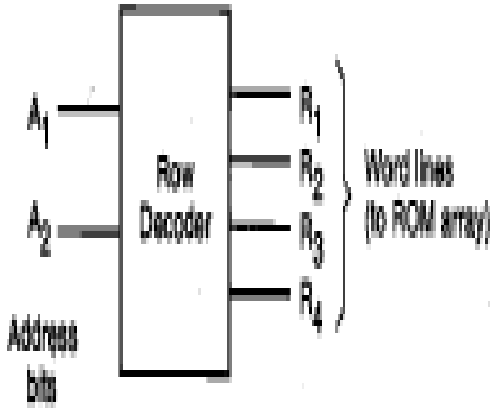
R1	R2	R3	R4	C1	C2	C3	C4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0

Design of Row and Column Decoders

- A row decoder designed to drive a NOR ROM array must, by definition, select one of the *2^N word lines by raising its voltage to VOH.*

- *As an example,*consider the simple row address decoder shown in Fig, which decodes a two-bit row address and selects one out of four word lines by raising its level.

Fig. Row address decoder example for 2 address bits and 4 word lines



A_1	A_2	R_1	R_2	R_3	R_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- A most straightforward implementation of this decoder is another NOR array, consisting of 4 rows (outputs) and 4 columns (two address bits and their complements).
- NOR-based decoder array can be built just like the NOR ROM array, using the same selective programming approach.
- The ROM array and its row decoder can thus be fabricated as two adjacent NOR arrays, as shown in Fig. 10.12.

NOR-based row decoder circuit for 2 address bits and 4 word lines.