UNIT 5:
Low – Power CMOS Logic Circuits

INTRODUCTION

- The VLSI low power design problems can be broadly classified into two:

1) *Analysis*
2) *Optimization*

- *Analysis problems are concerned about the accurate estimation of the* power or energy dissipation at different phases of the design process.

- The purpose is to increase confidence of the design with the assurance that the power consumption specifications are not violated.

- Analysis techniques differ in their accuracy and efficiency.

Overview of Power Consumption

- The accuracy of analysis depends on the availability of design information.
- In early design phases, the emphasis is to obtain power dissipation estimates rapidly with very little available information on the design.
- In these phases, less accurate analysis results are expected and tolerated.
- As the design proceeds to reveal more lower-level details, a more accurate analysis can be performed.
- Here, better accuracy is demanded and longer analysis time is allowed.

Needs for Low Power VLSI Chips

- Power dissipation of VLSI chips is traditionally a neglected subject.
- In the past, the device density and operating frequency were low enough that it was not a constraining factor in the chips.
- As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip.
- This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation.

Overview of Power Consumption

- There are two types of power dissipation in CMOS circuits:

  1) Dynamic

  2) Static

- **Dynamic power dissipation** is caused by switching activities of the circuits. A higher operating frequency leads to more frequent switching activities in the circuits and results in increased power dissipation.

- **Static power dissipation** is related to the *logical states of the circuits rather than switching activities.*

- *In CMOS logic, leakage current* is the only source of static power dissipation.

- The most significant source of dynamic power dissipation in CMOS circuits is the charging and discharging of capacitance.
- The capacitance forms due to parasitic effects of interconnection wires and transistors.
- Such parasitic capacitance cannot be avoided and it has a significant impact on the power dissipation of the circuits.

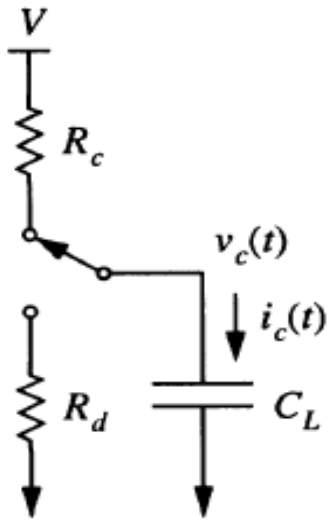


FIGURE 1.1 Equivalent circuit for charging and discharging a capacitor.

$$i_c(t) = C_L \frac{dv_c(t)}{dt} \tag{1.1}$$

During the charging cycle from time t_0 to t_1, the energy E_s drawn from the voltage source is

$$E_s = \int_{t_0}^{t_1} V\, i_c(t)\, dt \tag{1.2}$$

Initially the capacitor contains no charge and the voltage across its terminals is zero, i.e., $v_c(t_0) = 0$. Assume that the capacitor is *fully charged* at the end of the charging cycle, we have $v_c(t_1) = V$. Substituting Equation (1.1) into (1.2), we have

$$E_s = C_L V \int_{t_0}^{t_1} \frac{dv_c(t)}{dt}\, dt = C_L V \int_0^V dv_c = C_L V^2 \tag{1.3}$$

Part of the electrical energy E_s drawn from the voltage source is stored in the capacitor and the rest is dissipated as heat energy in the resistor R_c. The energy E_{cap} stored in the capacitor at the end of the charging cycle is

$$E_{cap} = \int_{t_0}^{t_1} v_c(t)\, i_c(t)\, dt = C_L \int_{t_0}^{t_1} v_c(t) \frac{dv_c(t)}{dt} dt$$

$$= C_L \int_0^V v_c\, dv_c = \frac{1}{2} C_L V^2 \tag{1.4}$$

From Equations (1.3) and (1.4), the energy E_c dissipated at R_c during charging is therefore

$$E_c = E_s - E_{cap} = \frac{1}{2} C_L V^2 \tag{1.5}$$

Now consider the discharging cycle from t_1 to t_2, we assume that the capacitor is *fully discharged*, i.e., $v_c(t_1) = V$ and $v_c(t_2) = 0$. The energy E_d dissipated in the discharge resistor R_d is

$$E_d = -\int_{t_1}^{t_2} v_c(t)\, i_c(t)\, dt = -C_L \int_V^0 v_c(t)\, dv_c = \frac{1}{2} C_L V^2 \tag{1.6}$$

E_d is exactly equal to the energy stored in the capacitance at the beginning of the discharging cycle. If we charge and discharge the capacitance at the frequency of f cycles per seconds, the power dissipation of the system is

$$P = E_s f = C_L V^2 f \tag{1.7}$$

- We now discuss the generality and applicability of the **P = C L V^2f** *equation by* reviewing the derivation procedure.
- **During charging**,
- C *L V^2 energy is* drawn from the energy source, half of which is dissipated in the charging resistance *Rc and the other half is stored in the capacitor.*
- **During discharge***,*
- The energy stored in the capacitor is dissipated as heat in the discharging resistor Rd.
- Only a few assumptions are made in our derivation:

  1. The capacitance C *L is constant.*
  2. The voltage *V is constant.*
  3. The capacitor is fully charged and discharged, i.e., *v/to) = 0, v /t]) = V, v c(t2) = 0.*

Equation (1.7) is only the power dissipation caused by a single capacitor C_L. In general, the total power should be summed over each capacitance C_i in a circuit yielding

$$P = \sum_i C_i V_i^2 f_i \tag{1.8}$$

where V_i is the voltage swing across the capacitor C_i switching at frequency f_i. For CMOS circuits, V is typically the same for all capacitance C_i. One simple approximation is to assume that f_i is constant, for example, by taking the average of all f_i's. This allows us to write

$$P = V^2 f \sum_i C_i = C_{total} V^2 f \tag{1.9}$$

in which C_{total} is the sum of all capacitance, f is the average frequency and V is the voltage swing.

Short-circuit Current in CMOS Circuit

- Another component of power dissipation also caused by signal switching called *short-circuit power.*

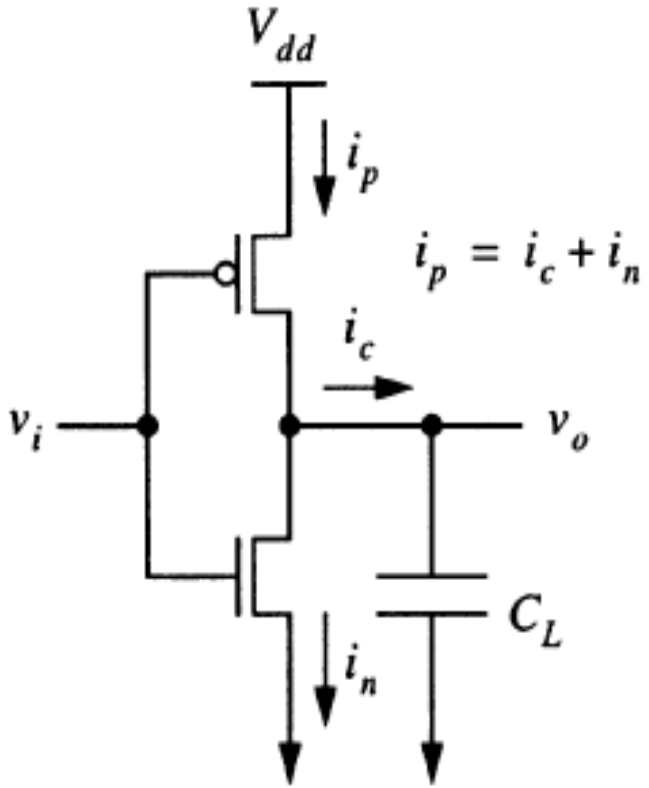
1)Short-circuit Current of an Inverter

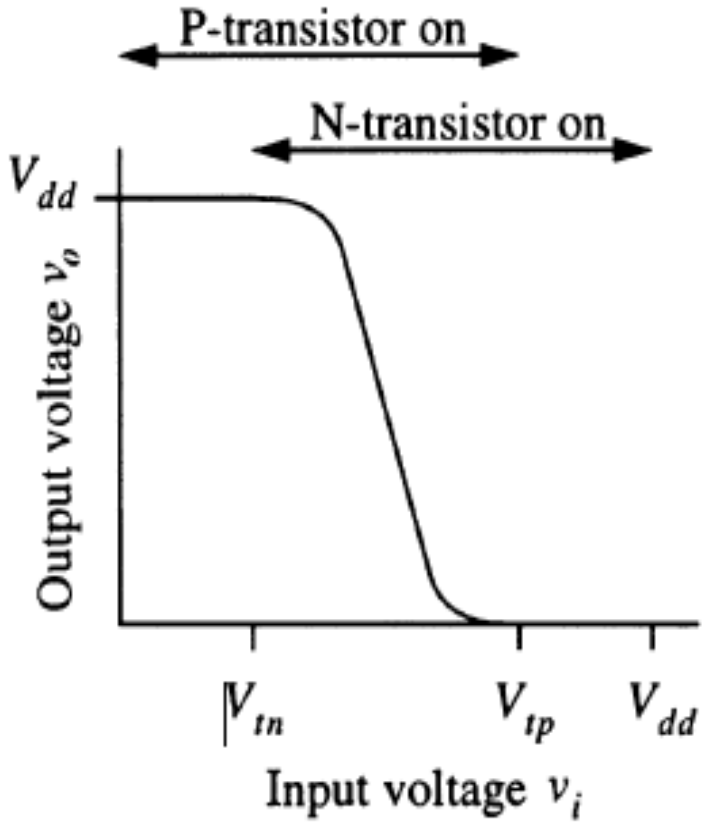
- When the input signal level is above *Vtn' the N-transistor is turned on. Similarly, when the signal level is* below *Vtp' the P-transistor is turned on.*

- *When the input signal Vi switches, there is a* short duration in which the input level is between *V tn and Vtp and both transistors are* turned on. This causes a short-circuit current from *Vdd to ground and dissipates* power.

- The electrical energy drawn from the source is dissipated as heat in the P and N -transistors.

A CMOS inverter and its transfer curve



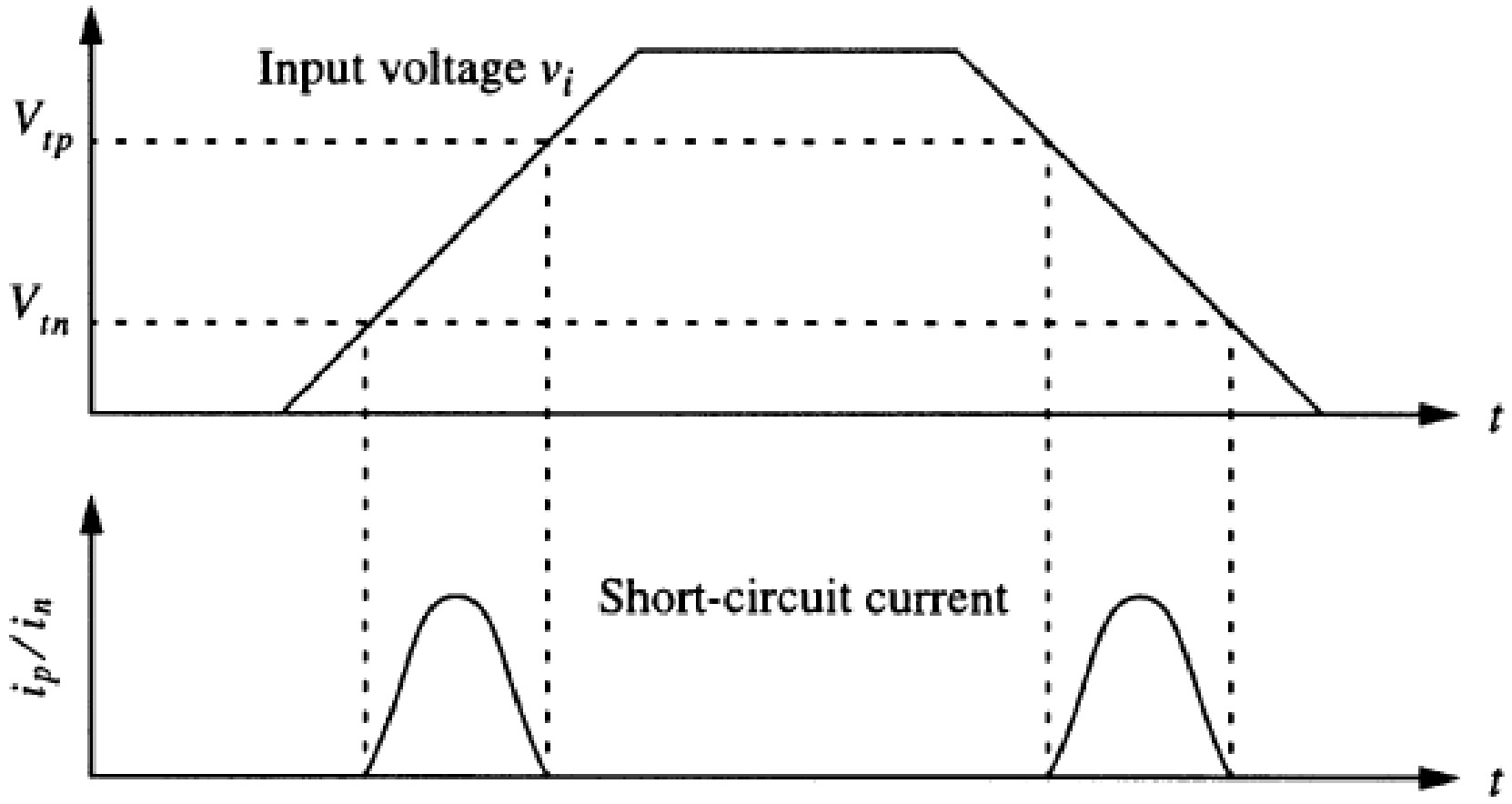


The shape of the short-circuit current curve is dependent on several factors:

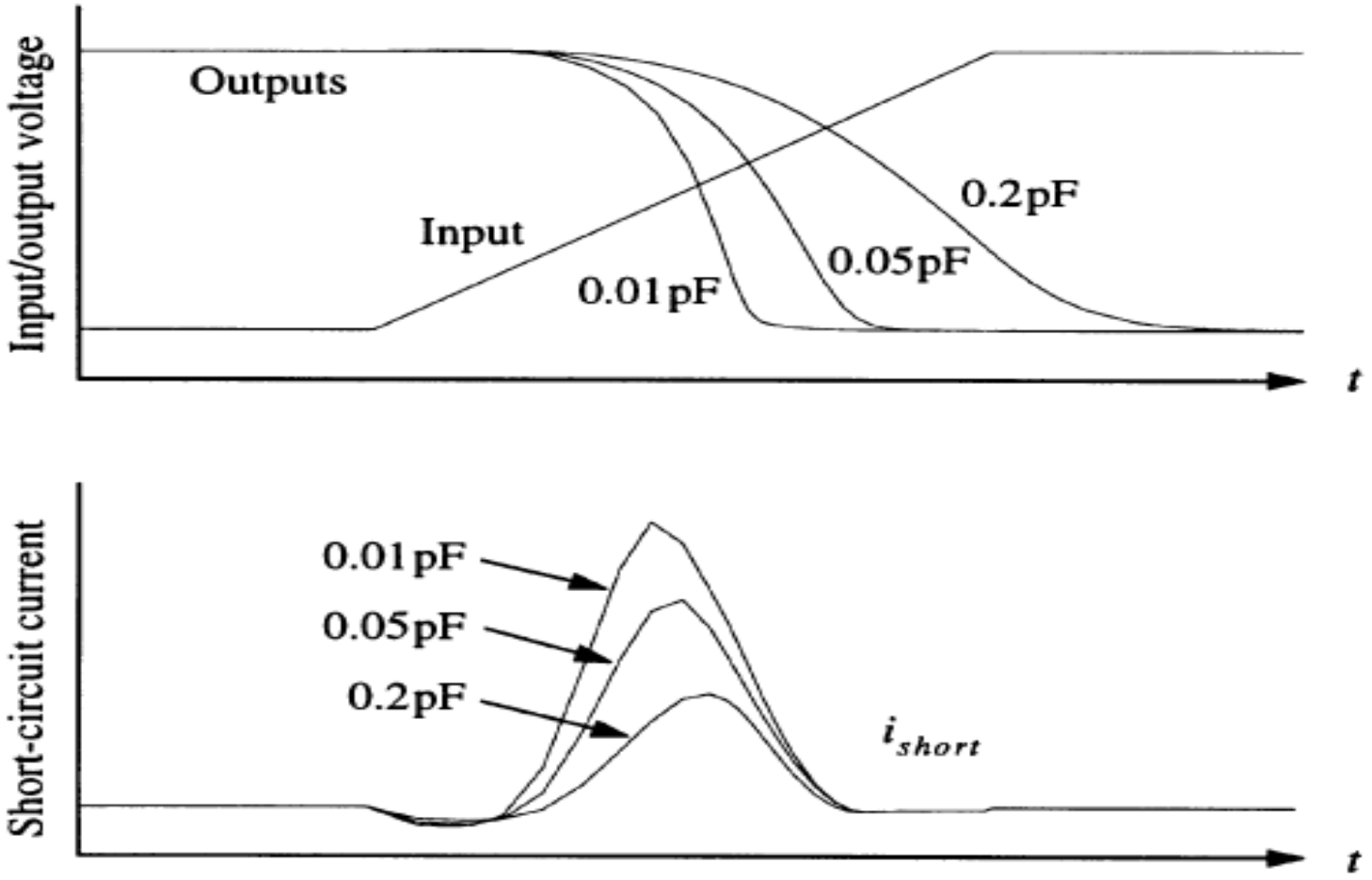
1. The duration and slope of the input signal.
2. The I-V curves of the P and N transistors, which depend on their sizes, process technology, temperature, etc.
3. The output loading capacitance of the inverter.

$$E_{short} = \frac{\beta}{12}\tau (V_{tp} - V_{tn})^3$$

Short-circuit current of a CMOS inverter during input transition



Short-circuit Current Variation with Output Load



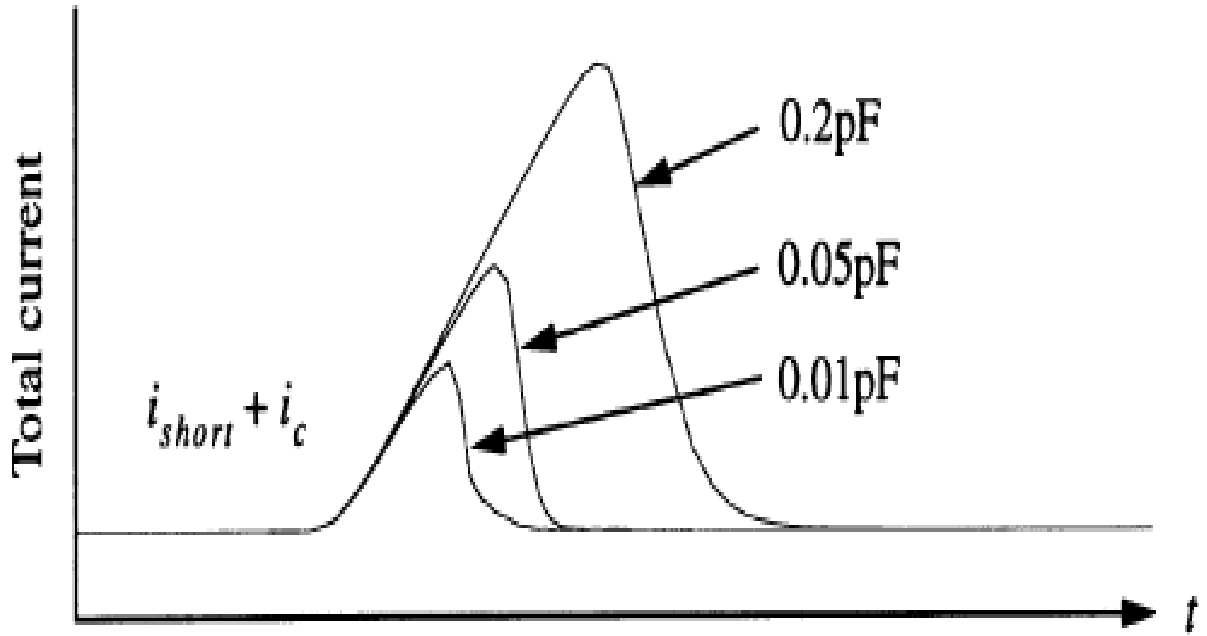
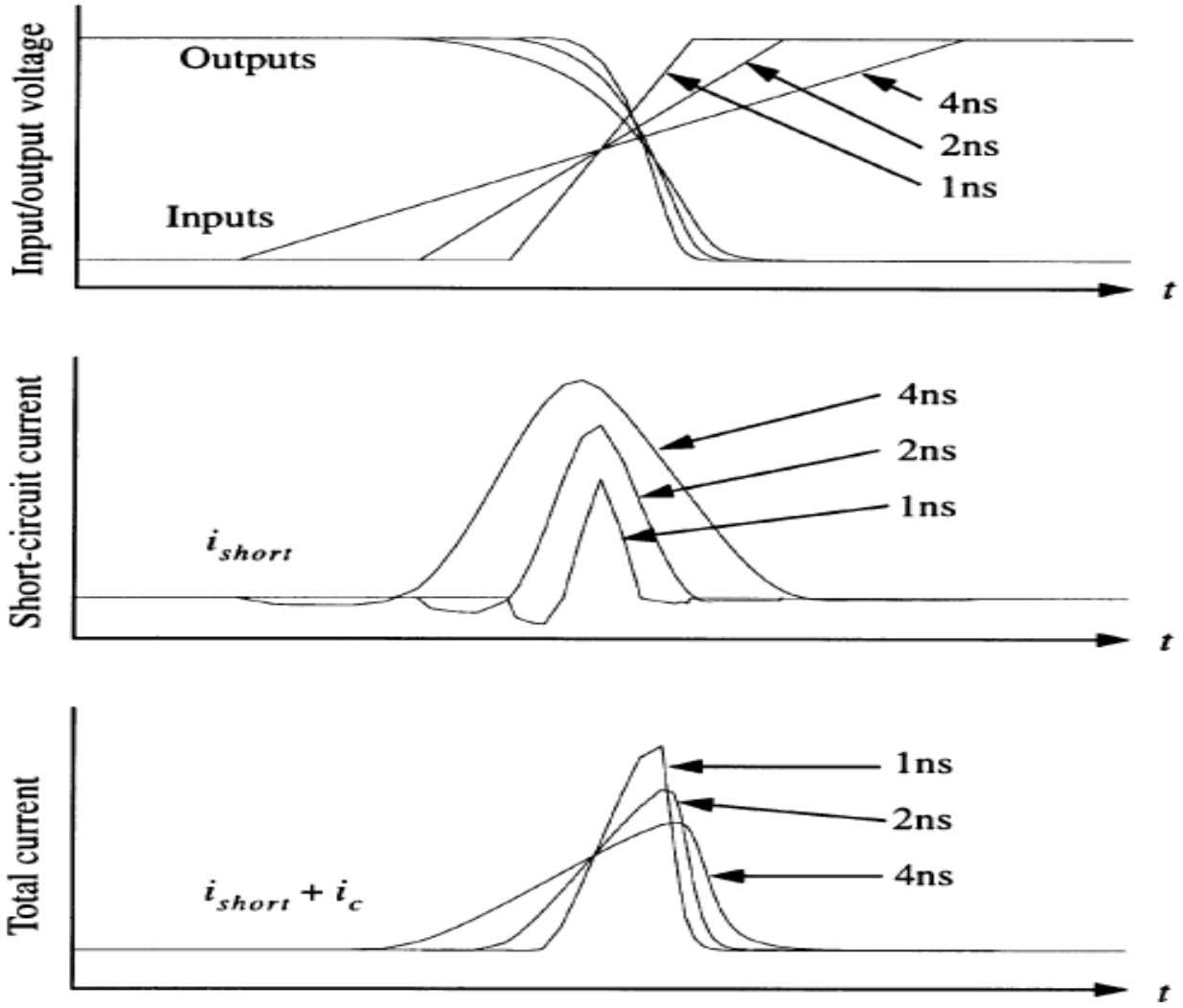


Fig. Total current under varying output capacitance

Effects of increasing output loading capacitance

Current envelope	Width	Peak	Integration
i_{short}	unchanged	decrease	decrease
i_c	increase	increase	increase
$i_{short} + i_c$	increase	increase	increase

Short-circuit Current Variation with Input Signal Slope



CMOS Leakage Current

- **Reverse Biased PN-junction**
- The first source of leakage current occurs when the source or drain of an N-transistor (P-transistor) is at *Vdd (Gnd}.*

- *PN-junctions are fonned at the source or drain of transistors* because of a parasitic effect of the bulk CMOS device structure.

- **Subthreshold Channel Leakage**
- The second source of leakage current is the subthreshold leakage through a MOS device channel. Even though a transistor is logically turned off, there is a non-zero leakage current through the channel at the microscopic level.

- This current is known as the *subthreshold leakage because it occurs when* the gate voltage is below its threshold voltage.

Static Current

- CMOS circuits are not supposed to consume static power from constant static current flow. All non-leakage current in CMOS circuits should only occur in transient when signals are switching.
- However, there are times when deviations from CMOS style circuit design are necessary.

- Pseudo NMOS circuit is not used on random logic.
- For special circuits such as PLAs or Register Files, it may be useful due to its efficient area usage.
- In such a circuit, there is a constant current flow from *Vdd to Gnd which dissipates power.*
- This is an example where power is traded for area efficiency.