UNIT 5:
Low – Power CMOS Logic Circuits

Low – Power Design through voltage scaling

- The dynamic power of digital chips expressed by given Equation is generally the largest portion of power dissipation.

- The ***P = CV^2f*** *equation consists of three terms:*
- **voltage, capacitance and frequency**

- Due to the quadratic effect of the voltage term, reducing the switching voltage can achieve dramatic savings.

- The easiest method to achieve this is to reduce the operating voltage of the CMOS circuit.

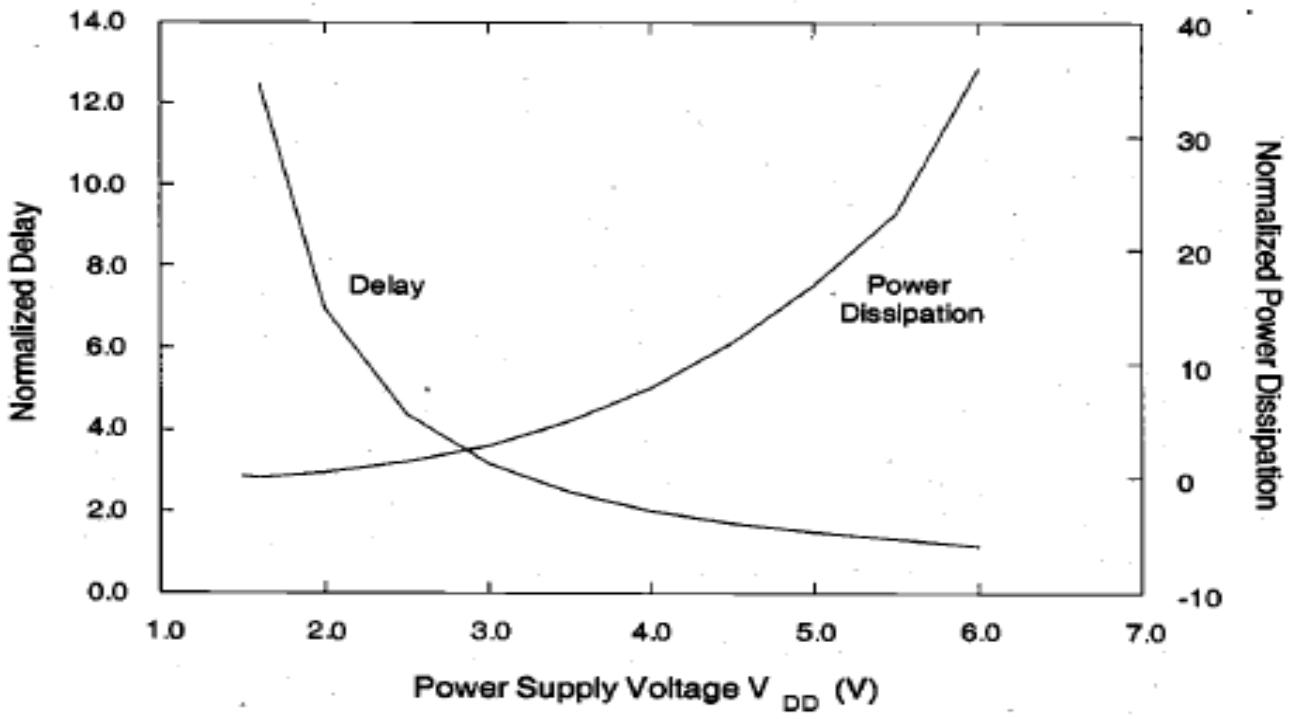
- Other methods seek to reduce voltage swing by using well-known circuit techniques such as charge sharing, transistor threshold voltage, etc.

- There are many trade-offs to be considered in voltage reduction.
- Performance is lost because MOS transistors become slower at lower operating voltages.
- The main reason is that the threshold voltages of the transistors do not scale accordingly with the operating voltage to avoid excessive leakage current.
- Noise immunity is also a concern at low voltage swing.
- Special level converters are required to interface low swing signals to the full-swing ones.

Influence of Voltage Scaling on Power and Delay

- Although the reduction of power supply voltage significantly reduces the dynamic power dissipation, the inevitable design trade-off is the increase of delay.

Normalized propagation delay and average switching power dissipation of a CMOS inverter, as a function of the power supply voltage *VDD.*



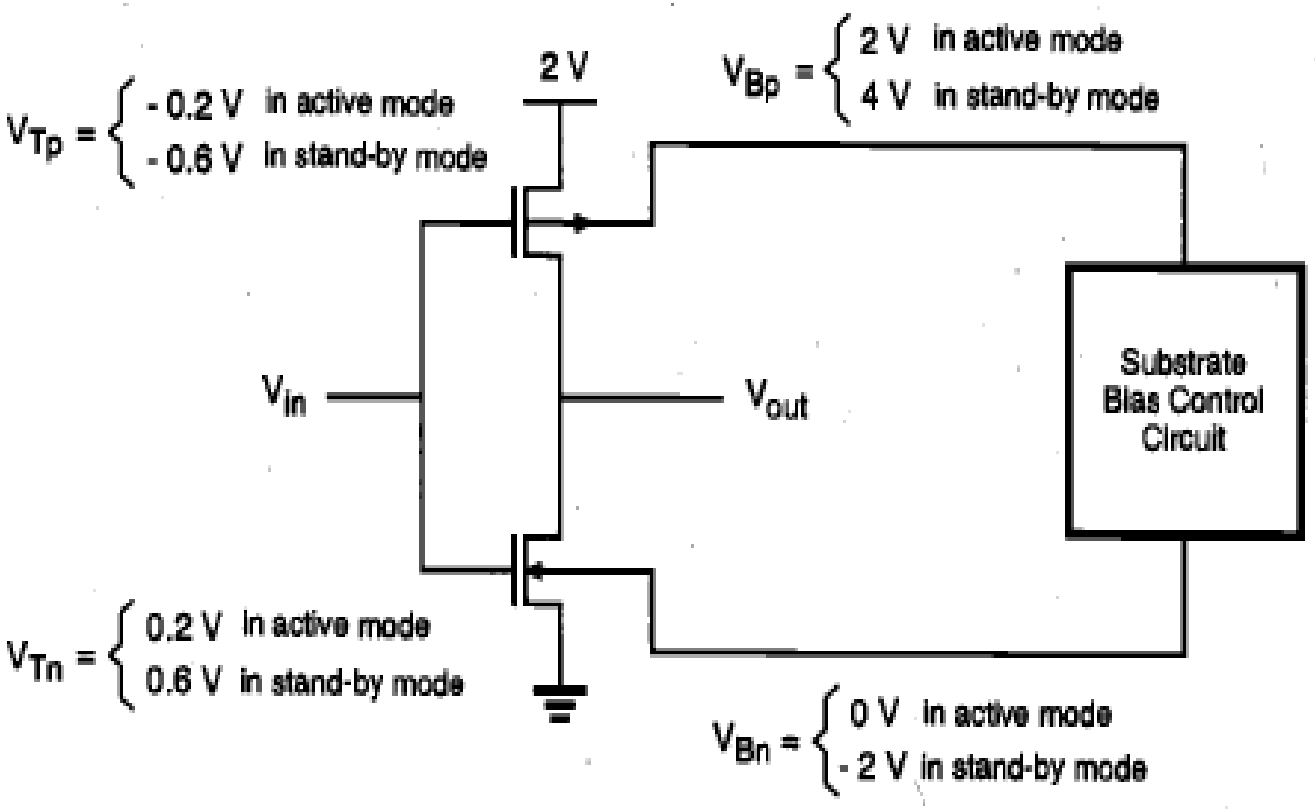
Variable-Threshold CMOS (VTCMOS) Circuits

- We have seen that using a low supply voltage *(VDD) and a low threshold voltage (VT) in* CMOS logic circuits is an efficient method for reducing the overall power dissipation, while maintaining high speed performance.

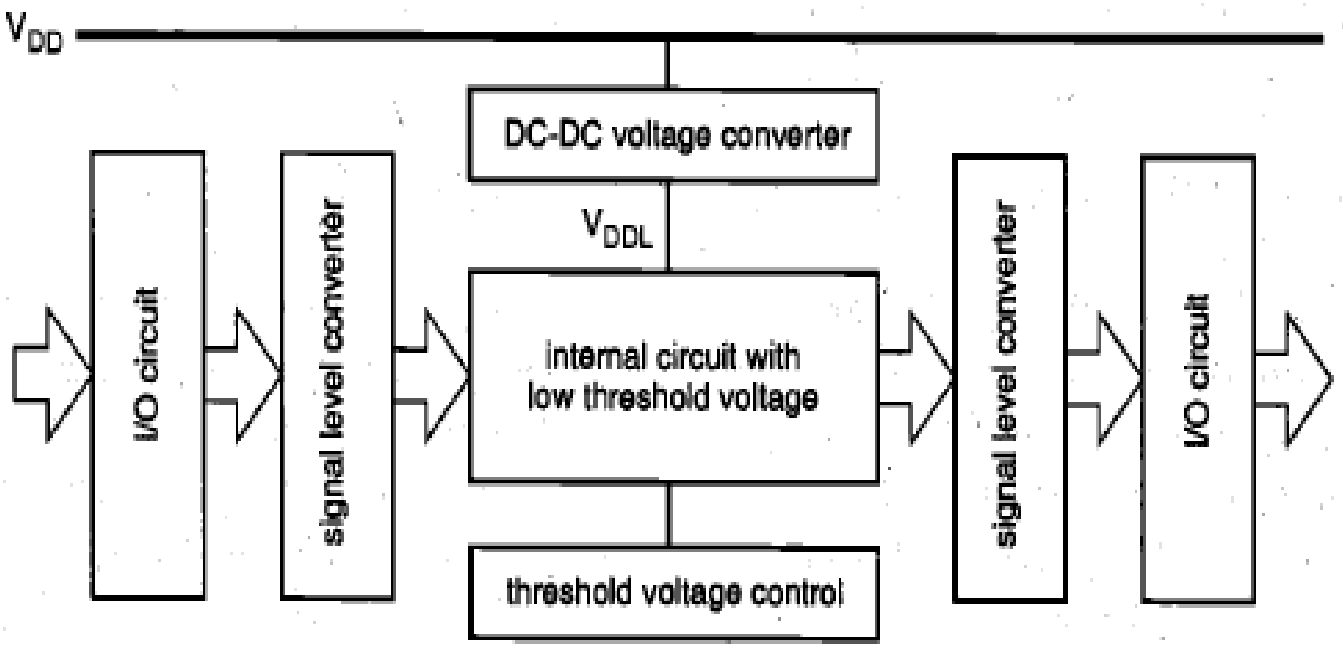
- Yet designing a CMOS logic gate entirely with low-VT transistors will inevitably lead to increased subthreshold leakage, and consequently, to higher stand-by power dissipation when the output is not switching.

- One possible way to overcome this problem is to *adjust the threshold voltages of the* transistors in order to avoid leakage in the stand-by mode, by changing the substrate bias.

A variable-threshold CMOS (VTCMOS) inverter circuit. The threshold voltages of nMOS and pMOS transistors are increased by adjusting the substrate bias voltage, in order to reduce subthreshold leakage currents in the stand-by mode.



Block diagram of a typical low-power chip. The internal supply voltage is generated on-chip, by a DC-DC converter circuit



Multiple-Threshold CMOS (MTCMOS) Circuits