UNIT 5:
Low – Power CMOS Logic Circuits

Estimation and Optimization of Switching Activity

- An approach to low power design is to reduce the switching activity and the amount of the switched capacitance to the minimum level required to perform a given task.
- The measures to accomplish this goal can range from optimization of algorithms to logic design, and finally to physical mask design.

The Concept of Switching Activity

- Dynamic power consumption of a CMOS logic gate depends, among other parameters, on the node transition factor αT, which is the effective number of power-consuming voltage transitions experienced by the output capacitance per clock cycle.

- This parameter, also called the switching activity factor, depends on the Boolean function performed by the gate, the logic family, and the input signal statistics.

- We can easily investigate the output transition probabilities for different types of logic gates

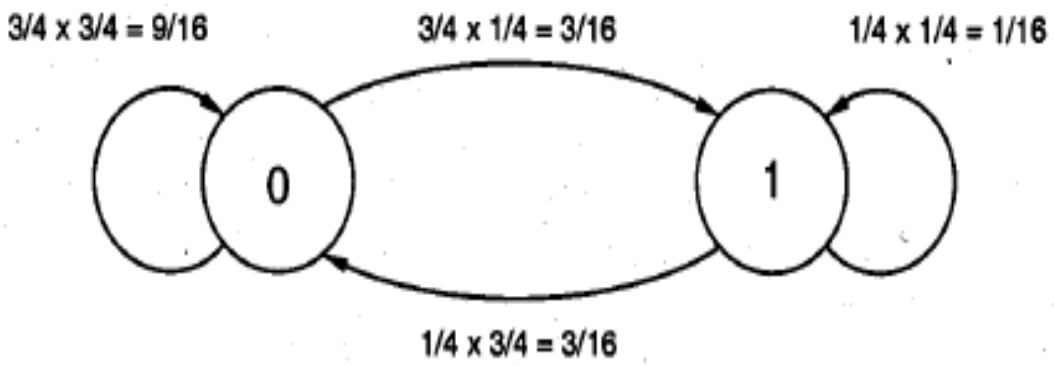
- Consider, two signal probabilities, *P0 and P1.*
- *P0 corresponds to the* probability of having a logic "0" at the output, and ***P1 = (1 - PO) corresponds to the*** probability of having a logic "1" at the output.
- Therefore, the probability that a power consuming (0-to- 1) transition occurs at the output node is the product of these two output signal probabilities.

Example: Static CMOS NOR2 gate

- If the two inputs are independent and uniformly distributed, the four possible input combinations (00, 01,10, 11) are equally likely to occur.
- Thus, we can find from the truth table of the NOR2 gate that PO = 3/4*, and* P1= 1/4.
- The probability that a power-consuming transition occurs at the output node is

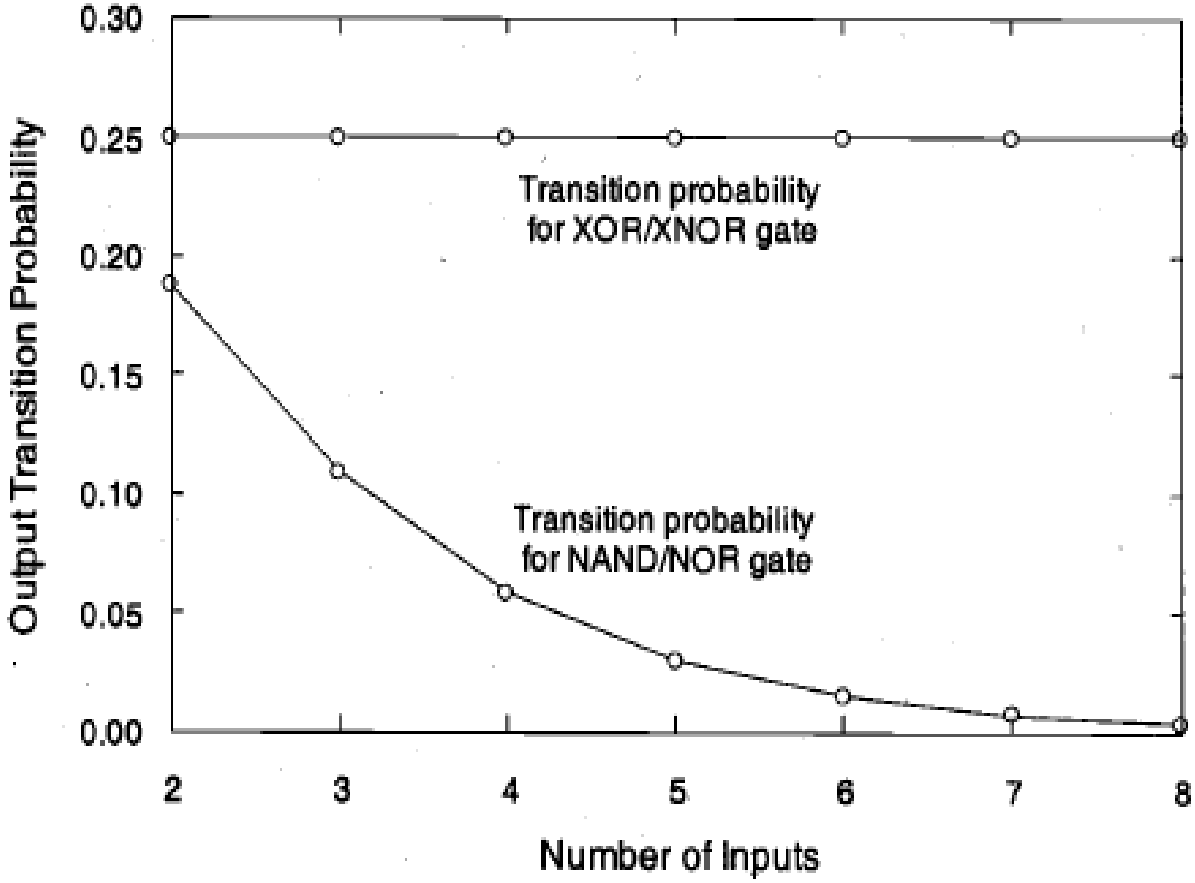
$$P_{0\to1} = P_0 \cdot P_1 = \frac{3}{4} \cdot \frac{1}{4} = \frac{3}{16}$$

State transition diagram and state transition probabilities of a NOR2 gate



- It shows two possible output states and the possible transitions.
- In the general case of a CMOS logic gate with n input variables, the probability of a power consuming output transition can be expressed as a function of *n0, which is the number of* zeros in the output column of the truth table.

$$P_{0\to1} = P_0 \cdot P_1 = \left(\frac{n_0}{2^n}\right) \cdot \left(\frac{2^n - n_0}{2^n}\right)$$



Output transition probabilities of different logic gates, as a function of the number of inputs. Note that the transition probability of the XOR gate is independent of the number or inputs.

- Consider the NOR2 gate examined above.
- Let $P_{1,A}$ represent the probability of having a logic " 1 " at the input A, and $P_{1,B}$ represent the probability of having a logic " 1 " at the input B.
- The probability of obtaining a logic " 1 "at the output node is

$$P_1 = \left(1 - P_{1,A}\right) \cdot \left(1 - P_{1,B}\right)$$

- Using this expression, the probability of a power-consuming output transition is found
- as a function of $P_{1,A}$ and $P_{1,B}$

$$P_{0\to 1} = P_0 \cdot P_1 = \left(1 - P_1\right) \cdot P_1$$

$$= \left(1 - \left(1 - P_{1,A}\right) \cdot \left(1 - P_{1,B}\right)\right) \cdot \left(\left(1 - P_{1,A}\right) \cdot \left(1 - P_{1,B}\right)\right)$$

Reduction of Switching Activity

- Switching activity in CMOS digital integrated circuits can be reduced by algorithmic optimization, by architecture optimization, by proper choice of logic topology or by circuit-level optimization.

- **<u>Techniques to reduce switching activity:</u>**

- ***Glitch Reduction***
- ***Gated Clock Signals***

Glitch Reduction

- It is based on **delay balancing** and the reduction of glitches.
- In multi-level logic circuits, the propagation delay from one logic block to the next can cause spurious signal transitions, or glitches as a result of *critical races or dynamic hazards.*
- If all input signals of a gate change simultaneously, no glitching occurs. But a dynamic hazard or glitch can occur if

  input signals change at different times.
- A node can exhibit multiple transitions in a single clock cycle before settling to the correct logic level

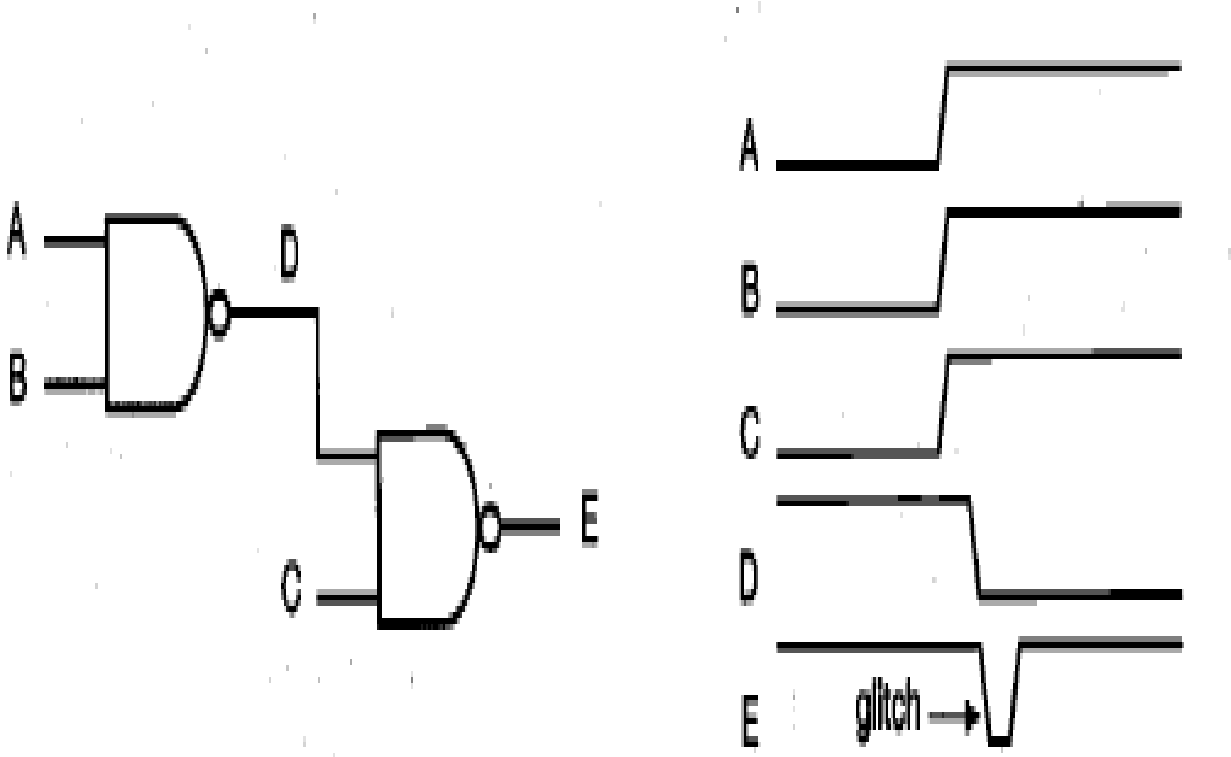
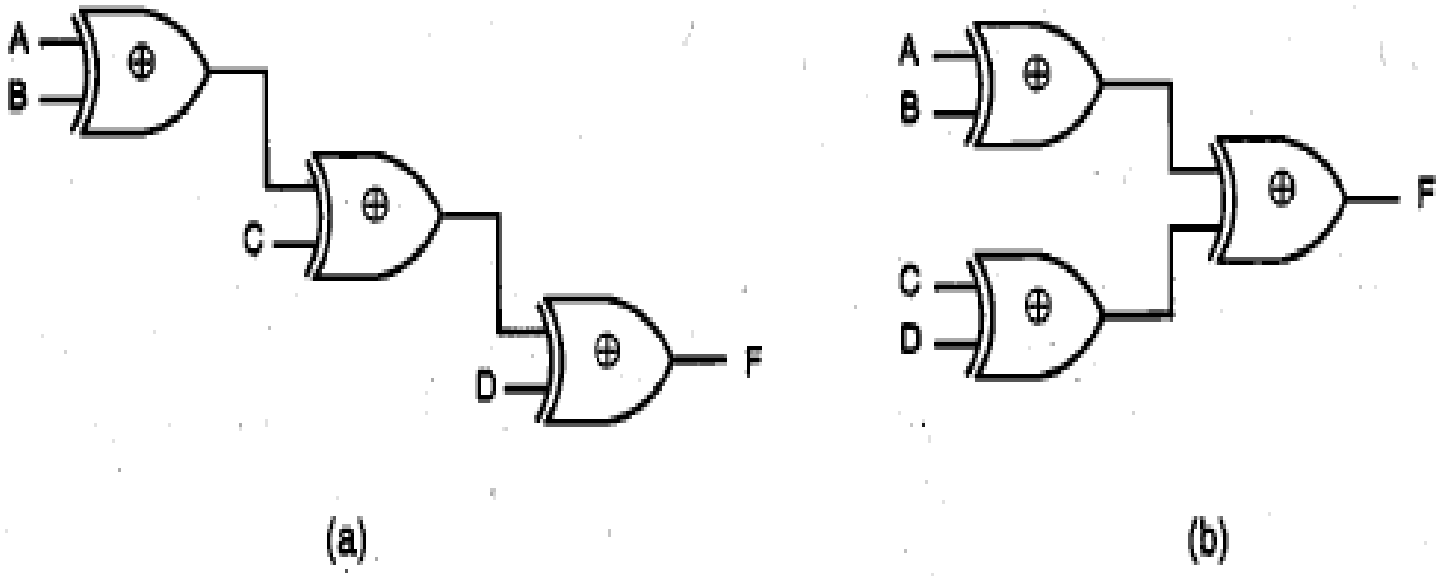


Fig: Signal glitching in multi-level static CMOS circuits

Eg: Simple parity network



- If all XOR gates have the same delay and four input signals arrive at the same time, the network in Fig(a) will suffer from glitching due to the wide disparity between the arrival times of the input signals.

- In the network shown in Fig. (b), all input arrival times are uniformly identical because the delay paths are balanced.

- Such redesign can significantly reduce the glitches, and consequently, the dynamic power dissipation in complex multi-level networks.

- The tree structure in Fig.(b) results in smaller overall propagation delay.

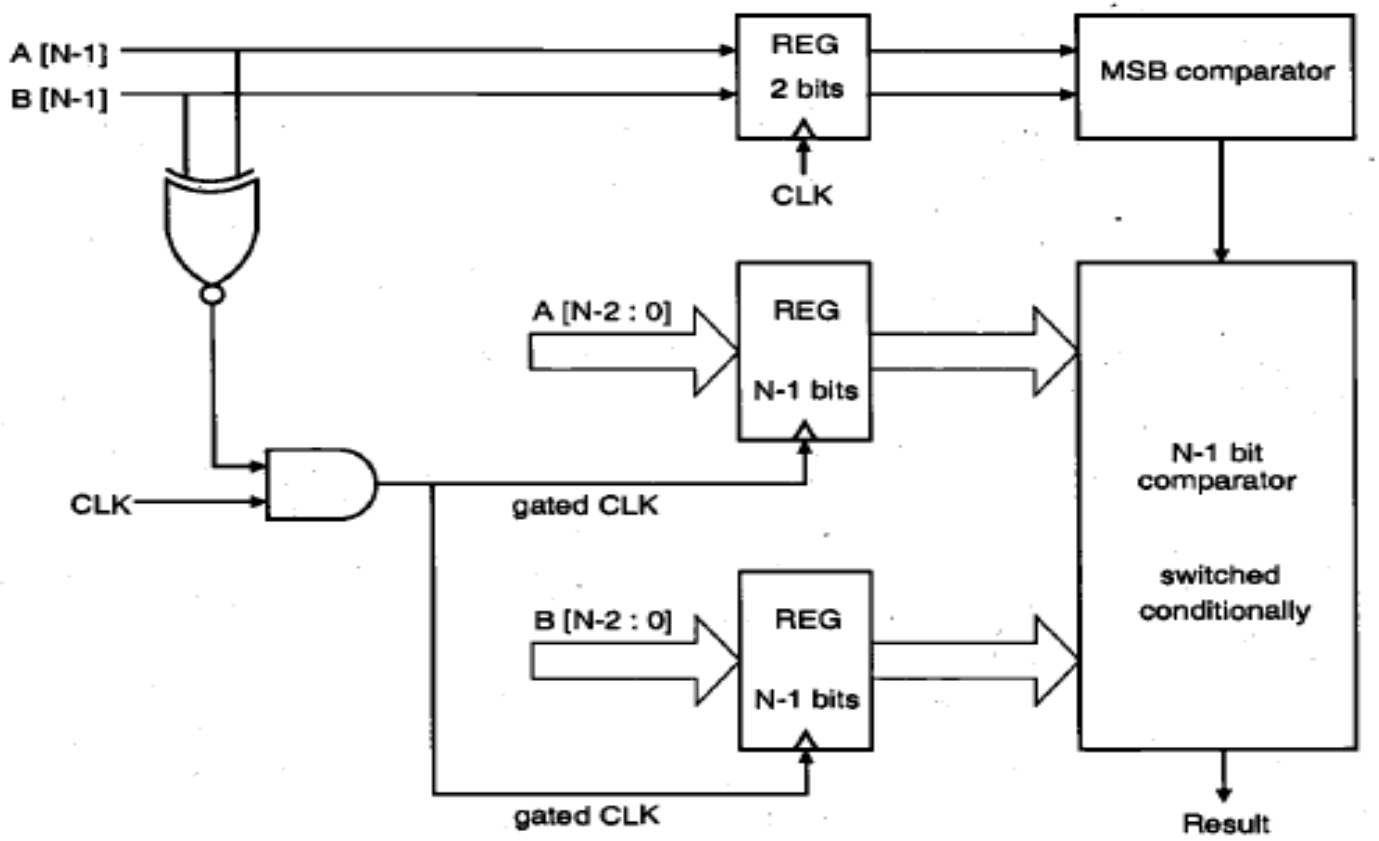
Gated Clock Signals

- The circuit compares the magnitudes of two unsigned N-bit binary numbers (A and B) and produces an output to indicate which one is larger. In the conventional approach, all input bits are first latched into two N-bit registers, and subsequently applied to the comparator circuit.

- In this case, two N-bit register arrays dissipate power in every clock cycle.

- Yet if the most significant bits, A[N-1 I and B[N-1], of the two binary numbers are different from each other, then the decision can be made by comparing the most significant bits (MSBs) only.

Eg. Block diagram of an N-bit number comparator with gated clock scheme



- The two MSBs are latched in a two-bit register which is driven by the original system clock. At the same time, these two bits are applied to an XNOR gate and the output of the XNOR is used to generate the gated clock signal with an AND gate.

- If the two MSBs are different (i.e., "01" or "10"), the XNOR produces a logic "0" at the output, disabling the clock signal of the lower-order registers. In this case, a separate MSB comparator circuit is used to decide which one of the two numbers is larger.

- If the two MSBs are identical (i.e., "00" or " 11"), the gated clock signal is applied to the lower order

  registers and the decision is made by the (N- 1)-bit comparator circuit.

- The amount of power dissipated in the lower-order registers and the (N-1)-bit comparator circuit can be quite significant, especially if the bit-length (N) is large.

- Assuming that the incoming binary numbers are randomly distributed, we can see that the gated clock strategy effectively reduces the overall switching power dissipation of the system by approximately 50%, since a large portion of the system is disabled for half of all input combinations.