UNIT 5:
Low – Power CMOS Logic Circuits

Reduction of Switched Capacitance

- Reduction of this parasitic capacitance is a major goal for low-power design of digital integrated circuits.

- There are various techniques at the system level, circuit level and physical design (mask) level which can be used to reduce the amount of switched capacitance.

1) System-Level Measures

- At the system level, one approach to reduce the switched capacitance is to limit the use of shared resources.
- A simple example is the use of a global bus structure for data transmission between a large number of operational modules.
- If a single shared bus is connected to all modules as in Fig. (a), this structure results in a large bus capacitance due to

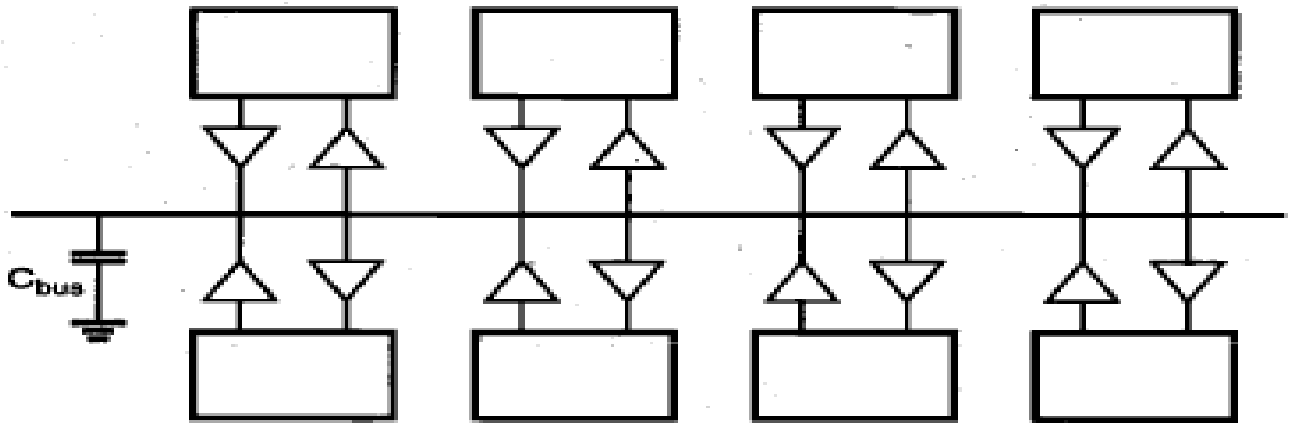
(i) the large number of drivers and receivers sharing the same transmission medium

(ii) the parasitic capacitance of the long bus line.

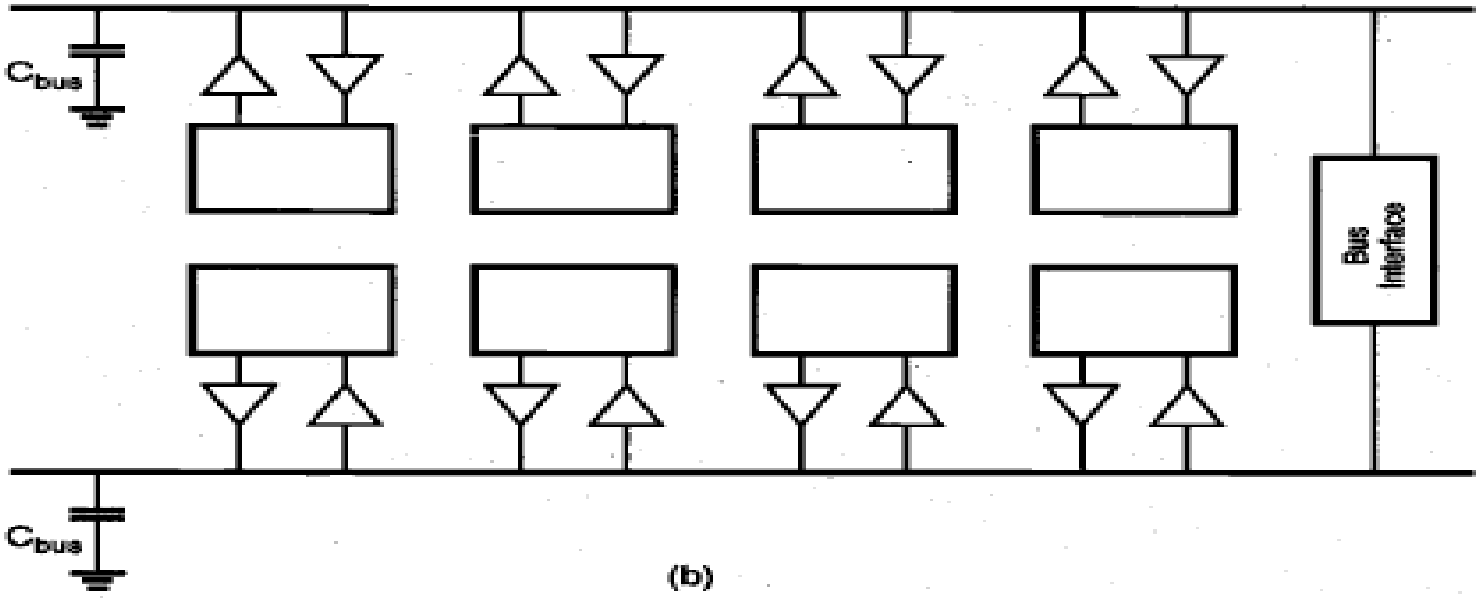
- Driving the large bus capacitance will require a significant amount of power consumption during each bus access.

- Alternatively, the global bus structure can be partitioned into a number of smaller dedicated local buses to handle the data transmission between neighboring modules, as shown in Fig(b).

- In this case, the switched capacitance during each bus access is significantly reduced, although multiple buses may increase the overall routing area on the chip.



(a)



(b)

2)Circuit-Level Measures

- The type of logic style used to implement a digital circuit also affects the output load capacitance of the circuit.
- The capacitance is a function of the number of transistors that are required to implement a given function.
- For example, one approach to reduce the load capacitance is to use transfer gates (pass-transistor logic) instead of conventional CMOS logic gates to implement logic functions.
- Pass-gate logic design is attractive since fewer transistors are required for certain functions such as XOR and XNOR.
- Therefore, this design style has emerged as a promising alternative to conventional CMOS, for low power design.
- Still, a number of important issues must be considered for pass-gate logic.

- The threshold-voltage drop through nMOS transistors while transmitting a logic " 1 “ makes swing restoration necessary in order to avoid static currents in subsequent inverter stages or logic gates (cf. Chapter 9). In order to provide acceptable output driving capabilities, inverters are usually attached to pass-gate outputs, which increases the overall area, time delay and the switching power dissipation of the logic gate.

- Because pass-transistor structures typically require complementary control signals, dual-rail logic is used to provide all signals in complementary form.

- As a consequence, two complementary nMOS pass-transistor networks are necessary in addition to swing restoration and output buffering circuitry, effectively diminishing the inherent advantages of pass transistor logic over conventional CMOS logic.

- Thus, the use of pass-transistor logic gates to achieve low power dissipation must be carefully considered, and the choice of logic design style must ultimately be based on a detailed comparison of all design aspects such as silicon area, overall delay as well as switching power dissipation.

3)Mask-Level Measures

- The amount of parasitic capacitance that is switched (i.e. charged up or charged down) during operation can be also reduced at the physical design level, or mask level.

- The parasitic gate and diffusion capacitances of MOS transistors in the circuit typically constitute a significant amount of the total capacitance in a combinational logic circuit.

- Hence, a simple mask-level measure to reduce power dissipation is keeping the transistors (especially the drain and source regions) at minimum dimensions whenever possible and feasible, thereby minimizing the parasitic capacitances.

- Designing a logic gate with minimum-size transistors certainly affects the dynamic performance of the circuit, and this trade-off between dynamic performance and power dissipation should be carefully considered in critical circuits.

- Especially in circuits driving a large *extrinsic capacitive* loads, e.g., large fan-out or routing capacitances, the transistors must be designed with larger dimensions.

- Yet in many other cases where the load capacitance of a gate. is mainly *intrinsic, the transistor sizes can be kept at a minimum.*

- *Note that most standard cell* libraries are designed with larger transistors in order to accommodate a wide range of capacitive loads and performance requirements.

- Consequently, a standard-cell based design may have considerable overhead in terms of switched capacitance in each cell.

Adiabatic Logic Circuits

- In conventional level-restoring CMOS logic circuits with rail-to-rail output voltage swing, each switching event causes an energy transfer from the power supply to the output node, or from the output node to the ground.

- During a O-to-VDD transition of the output, the total output charge Q *= Cd VDD is drawn from the power supply at a constant voltage.*

- Thus, an energy of *EsuppI = C load VDD2 is drawn from the power supply during this* transition.

- Charging the output node capacitance to the voltage level *VDD means that at* the end of the transition, the amount of stored energy in the output node is *Estored = Cad VDD 2/2.*

- *Thus, half of the injected energy from the power supply is dissipated in the pMOS* network while only one half is delivered to the output node.

- During a subsequent *VDDto* O transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the nMOS network.

- To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods.

- Yet in all these cases, the energy drawn from the power supply is usedonly once before being dissipated.

- To increase the energy efficiency of logic circuits, other measures can be introduced for *recycling the energy drawn from the power supply.*

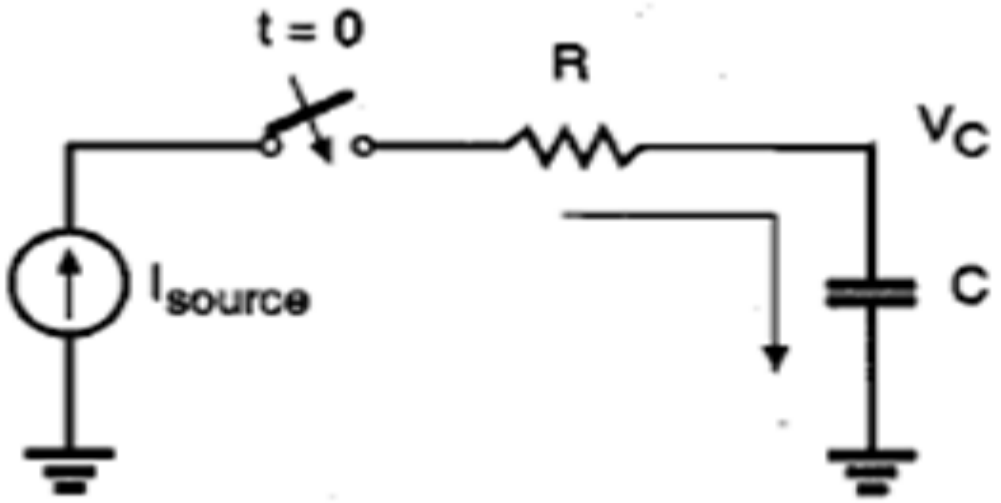
- *A* novel class of logic circuits called *adiabatic logic offers the possibility of further* reducing the energy dissipated during switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply.

- To accomplish this goal, the circuit topology and the operation principles have to be modified, sometimes drastically.

- The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed and voltage swing.

- The term "adiabatic" is typically used to describe thermodynamic processes that have no energy exchange with the environment, and therefore, no energy loss in the form of dissipated heat.

Adiabatic Switching

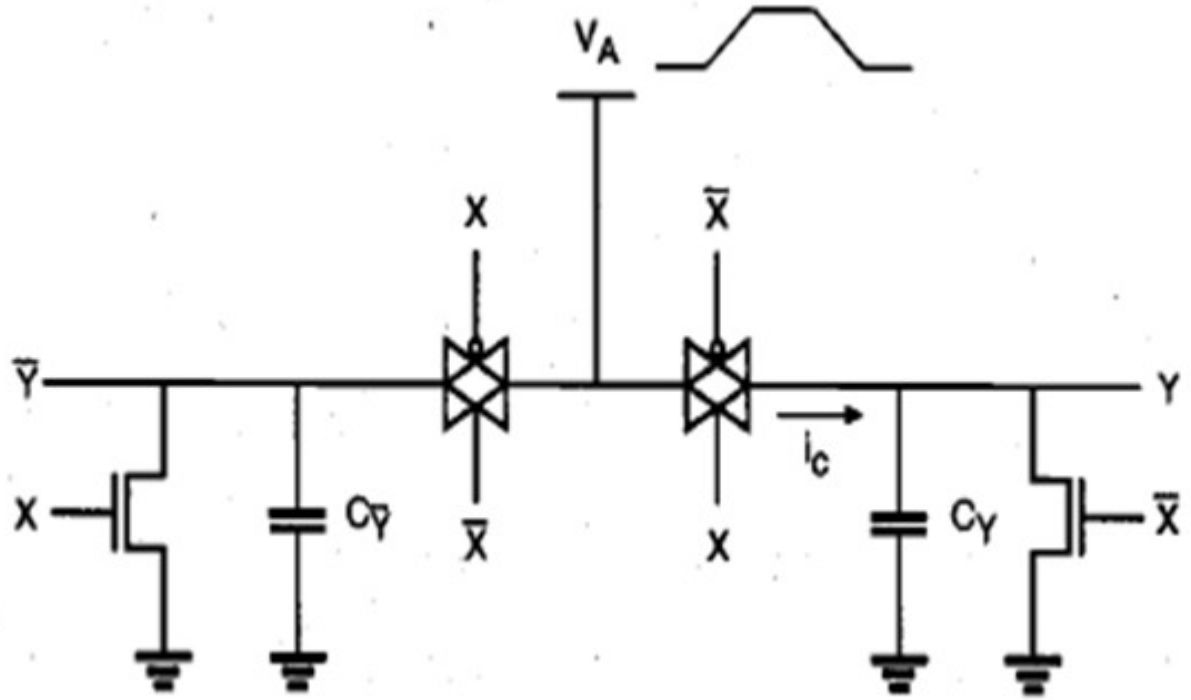


Constant-current source charging a load capacitance *C*, through a resistance *R*

- The dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = \frac{RC}{T} C V_C^2(T)$$

Adiabatic Logic Gates



Circuit diagram of an adiabatic CMOS AND/NAND gate.