UNIT 5:
Low – Power CMOS Logic Circuits

Design for Testability: Introduction

- The task of determining whether fabricated chips are fully functional is highly complex and can be very time-consuming.
- However, when faulty chips pass an improperly designed test, they can cause system failures and enormous difficulty in system debugging.
- It is known that the debugging cost increases by about tenfold from chip level to board level, and also from board level to system level.
- Thus, it is of great importance to detect faults as early as possible. As the number of transistors integrated into a single chip increases, the task of chip testing to ensure correct functionality becomes increasingly more difficult.

Introduction (Contd.)

- In a production environment, many chips must be tested within a short time for timely delivery to customers.
- To overcome such difficult issues, *design for testability has become ever more critical.*
- *In this chapter, we discuss types of faults,* the corresponding fault models, design of testable circuits, and self-testing circuits.
- The testability will be defined in terms of observability and controllability, which are also commonly used in control and system theory.

Fault Types and Models

Examples of ***physical defects*** *include:*

* Defects in silicon substrate
* Photolithographic defects
* Mask contamination and scratches
* Process variations and abnormalities
* Oxide defects

The physical defects can cause electrical faults and logical faults.

The ***electrical faults*** *include:*

- Shorts (bridging faults)
- Opens Transistor stuck-on, stuck-open
- Resistive shorts and opens
- Excessive change in threshold voltage
- Excessive steady-state currents

The electrical faults in turn can be translated into logical faults.

The ***logical faults*** include:

- Logical stuck-at-0 or stuck-at-I
- Slower transition (delay fault)
- AND-bridging, OR-bridging

- The relationships between physical defects, electrical faults, and logical faults can be explained using a simple NOR2 gate as shown in Fig.

- A metallic blob (physical defect) between the common drain terminal in the n-diffusion region and the ground bus line shown in Fig.(a) can be modeled as a *resistive short between the output node* Z and the ground as shown in Fig.(b),

- And also by a *stuck-at-0 (s-a-0) fault of output* Z when the resistance is low or a *pull-up delay fault when the resistance is high, as shown* in Fig.(c).

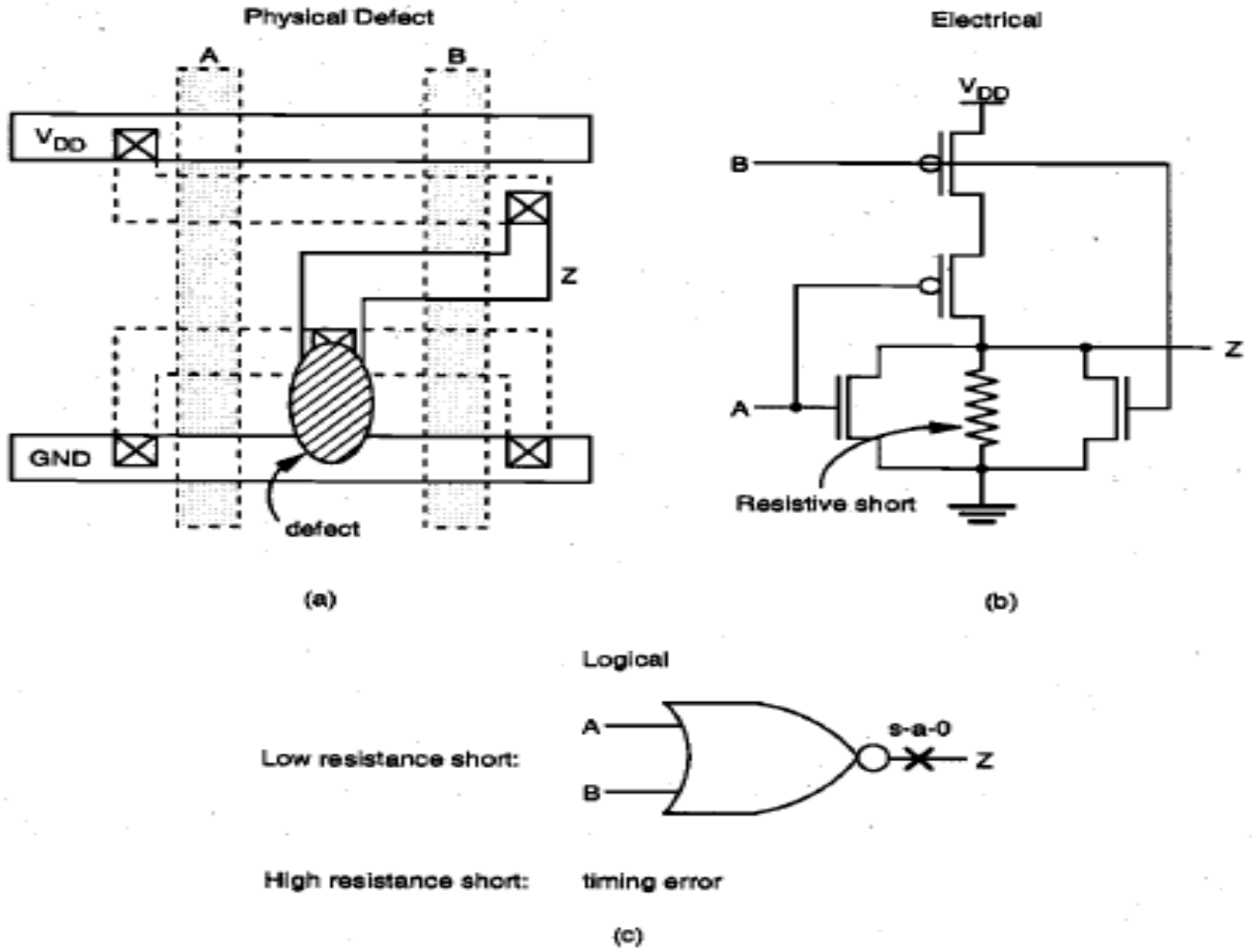


Fig. (a) Physical defect in NOR2 fabrication, (b) its electrical fault model; and (c) its logical fault models.

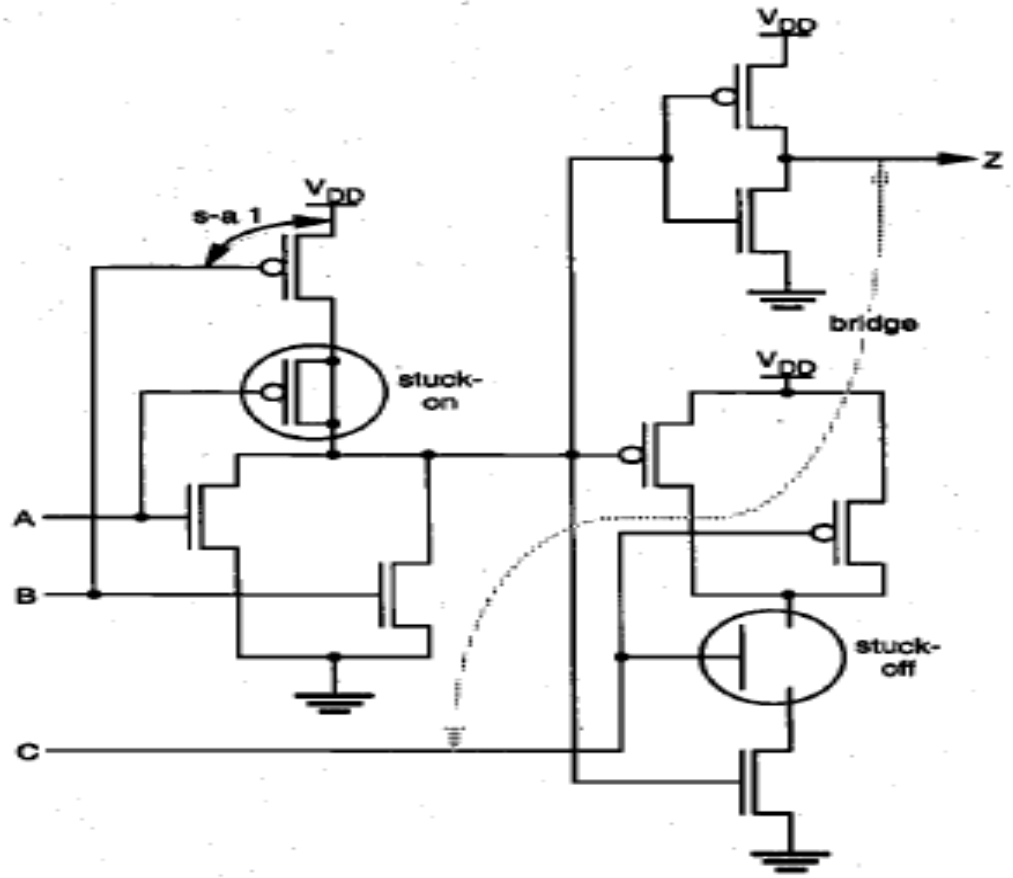
- The single stuck-at fault models are used frequently, although the DUT can have defects that do not map to a single stuck-at fault. Some of the reasons are:

- Complexity of test generation is greatly reduced.

- Single stuck-at fault is independent of technology, design style.

- Single stuck-at tests cover a large percentage of multiple stuck-at faults.

- Single stuck-at tests cover a large percentage of *unmodeled physical defects.*



Some process-related defects in a CMOS circuit consisting of NOR2, NAND2, and inverter gates.