UNIT 5:
Low – Power CMOS Logic Circuits

Controllability and Observability

- The ***controllability*** *of a circuit is a measure of the ease (or difficulty) with which the* controller (test engineer) can establish a specific signal value at each node by setting values at the circuit input terminals.

- The ***observability*** *is a measure of the ease (or* difficulty) with which one can determine the signal value at any logic node in the circuit by controlling its primary input and observing the primary output.

- The term *primary* refers to the I/O boundary of the circuit under test.

- The degree of controllability and observability and, thus, the degree of testability of a circuit, can be measured with respect to whether test vectors are generated deterministically or randomly.

- For example, if a logic node can be set to either logic 1 or 0 only through a very long sequence of random test vectors, the node is said to have a very *low random controllability since the* probability of generating such a vector in random test generation is very low.

- There exist time constraints in practice, and in such cases the circuit may not be considered testable.

- There are deterministic procedures for test generation for combinational circuits, such as the D-algorithm which uses a recursive search procedure advancing one gate at a time and backtracking, if necessary, until all the faults are detected.

- The D-algorithm requires a large amount of computer time. To overcome such shortcomings, many improved algorithms such as Path-Oriented DEcision Making (PODEM) and FAN-out-oriented test generation (FAN) have been introduced, Sequential circuit test generation is several orders of magnitude more difficult than these algorithms.

- To ease the task of ATG, design-for-test (DFT) techniques are routinely employed.

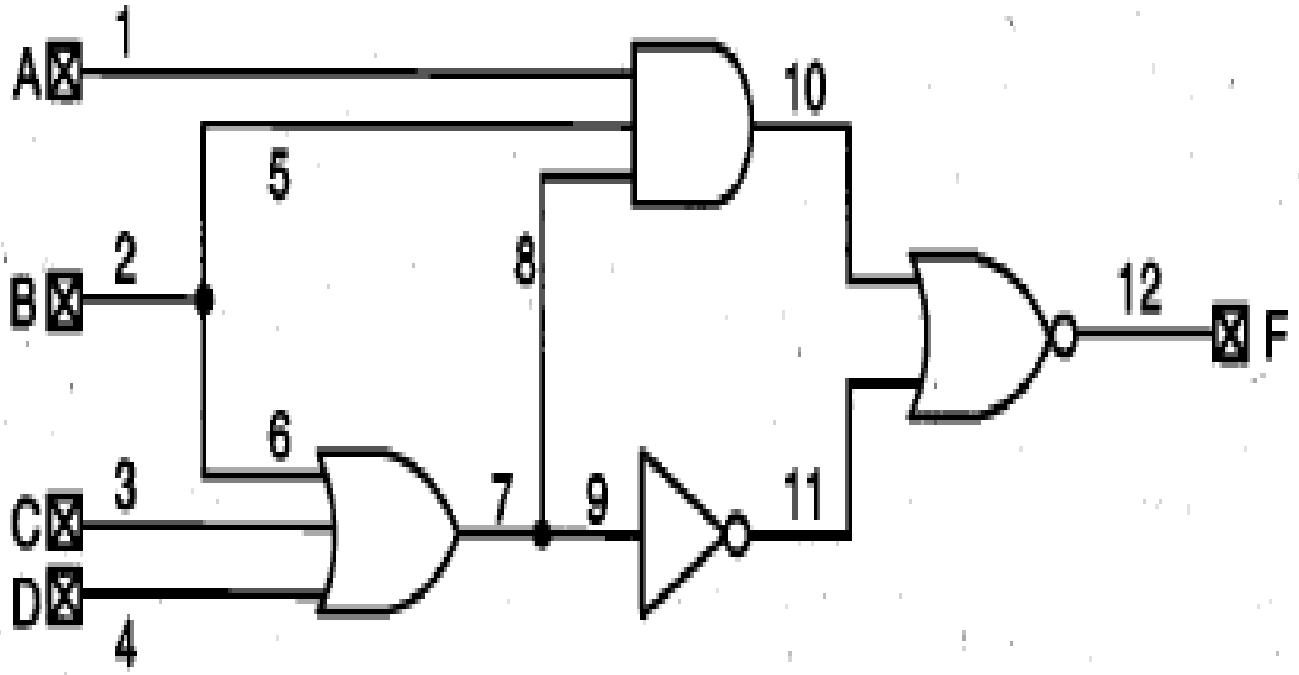

Fig. A simple circuit consisting of four gates with four primary inputs and one primary output.

- To detect any defect on line 8, the primary inputs A and B must be set to logic 1.
- However, such a setting forces line 7 to logic 1. Thus, any stuck-at- (s-a- 1) fault on line 7 *cannot be tested at the primary output, although in the absence of such a fault, the logic* value on line 7 can be fully controllable through primary inputs B, C, and D.

- Therefore, this circuit is *not fully testable. The main cause of this difficulty in this circuit is the fact* that input B fans out to lines 5 and 6, and then after the OR3 gate, both line signals are combined in the AND3 gate.

- Such a fanout is called ***reconvergent*** *fanout.*

- *Reconvergent* fanouts make the testing of the circuit much more difficult.

- If a large number of input vectors are required to set a particular node value to 1 or 0 (fault excitation) and to propagate an error at the node to an output (fault effect propagation), then the testability is low.

- The circuits with poor controllability include those with feedbacks, decoders, and clock generators.

- The circuits with poor observability include sequential circuits with long feedback loops and circuits with reconvergent fanouts, redundant nodes, and embedded memories such as RAM, ROM, and PLA.