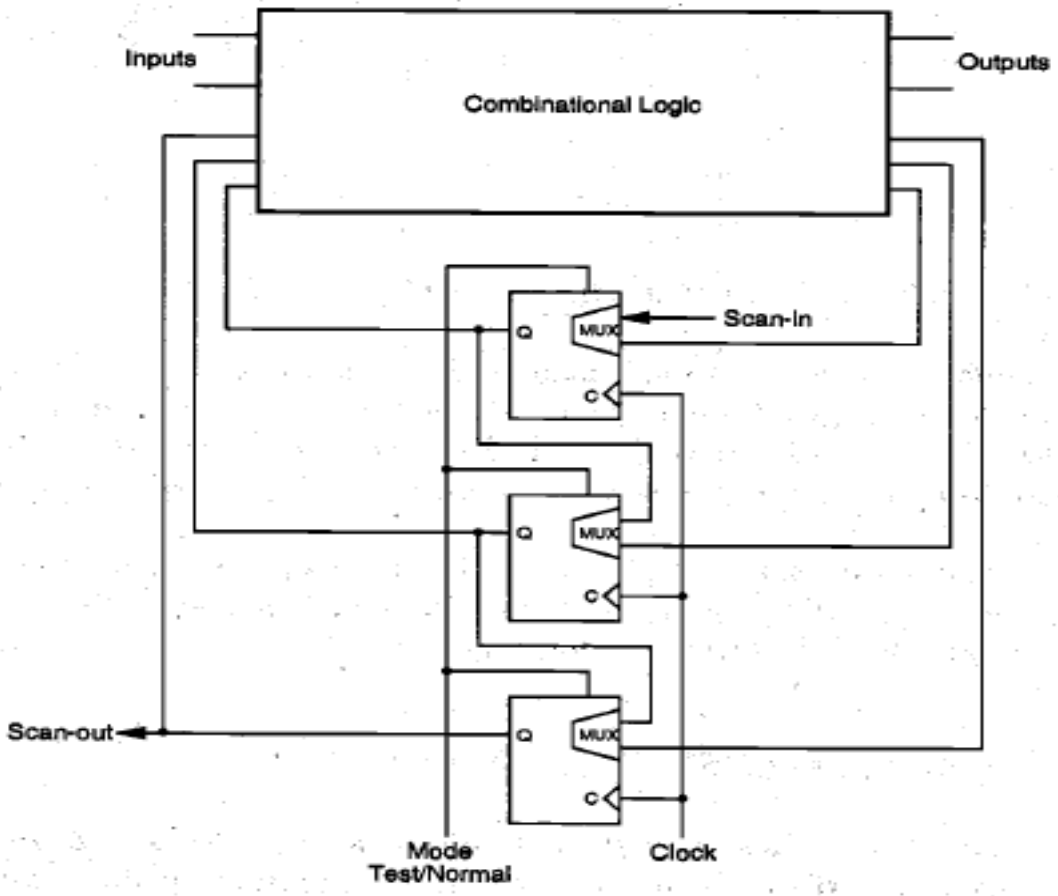
UNIT 5:
Low – Power CMOS Logic Circuits

Scan-Based Techniques



- **Step 1:** Set the mode to *test and, let latches accept data from scan-in input,*
- **Step 2:** Verify the scan path by shifting in and out the test data.
- **Step 3:** Scan in (shift in) the desired state vector into the shift register.
- **Step 4:** Apply the test pattern to the prim ary input pins. I : ;
- **Step 5:** Set the mode to *normal and observe the primary outputs of the circuit after* sufficient time for propagation.
- **Step 6:** Assert the circuit clock, for one machine cycle to capture the outputs of the combinational logic into the registers.
- **Step 7:** Return to *test mode; scan out the contents of the registers, and at the same time* scan in the next pattern.
- **Step 8:** Repeat steps 3-7 until all test patterns are applied.

- The storage cells in scan design can be implemented using edge-triggered D flipflops, master-slave flip-flops, or level-sensitive latches controlled by complementary clock signals to ensure race-free operation.

- Figure shows a scan-based design of an edge-triggered D flip-flop.

- In large high-speed circuits, optimizing a single clock signal for skews, etc., both for normal operation and for shift operation, is difficult.

- To overcome this difficulty, two separate clocks, one for normal operation and one for shift operation, are used.

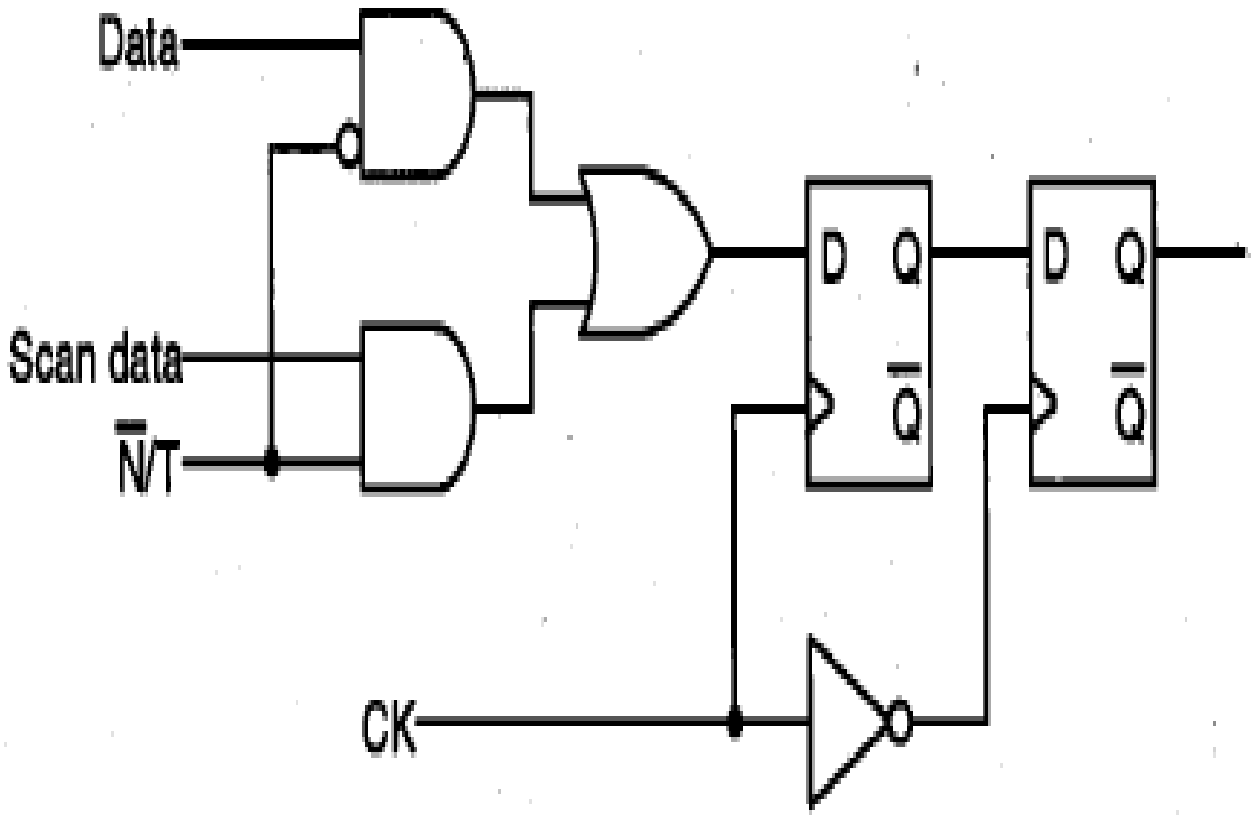


Figure 16.10. Scan-based design of an edge-triggered D flip-flop.

Built-In Self Test (BIST) Techniques

- In built-in self test (BIST) design, parts of the circuit are used to test the circuit itself.
- Online BIST is used to perform the test under normal operation, whereas off-line BIST is used to perform the test off-line.

The essential circuit modules required for BIST include:

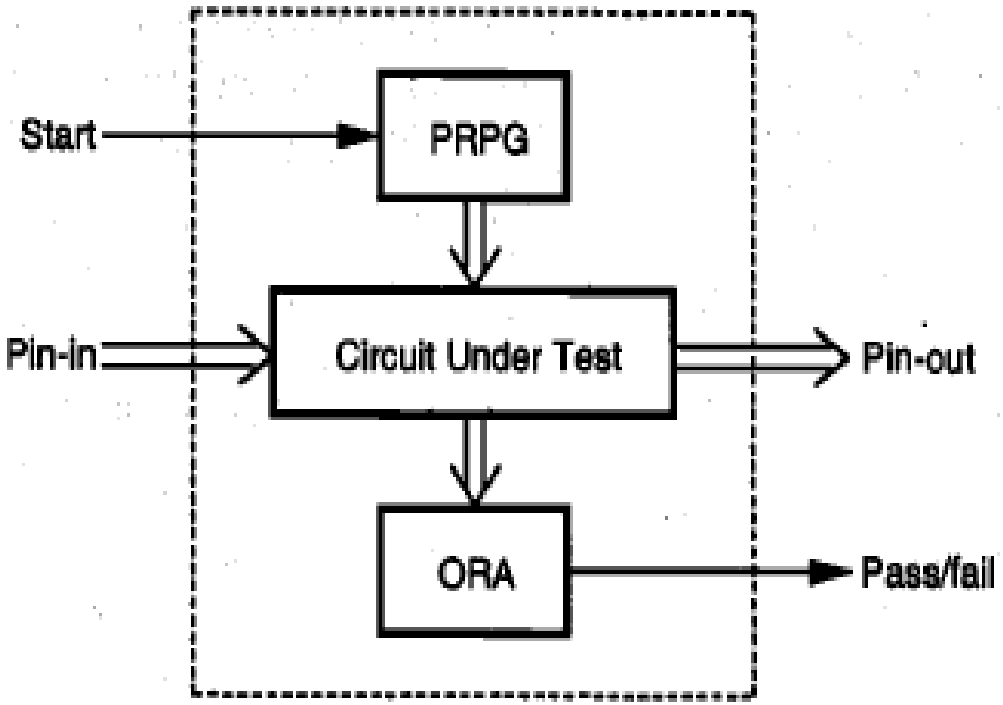
- Pseudo random pattern generator (PRPG)
- Output response analyzer (ORA)

Pseudo Random Pattern Generator

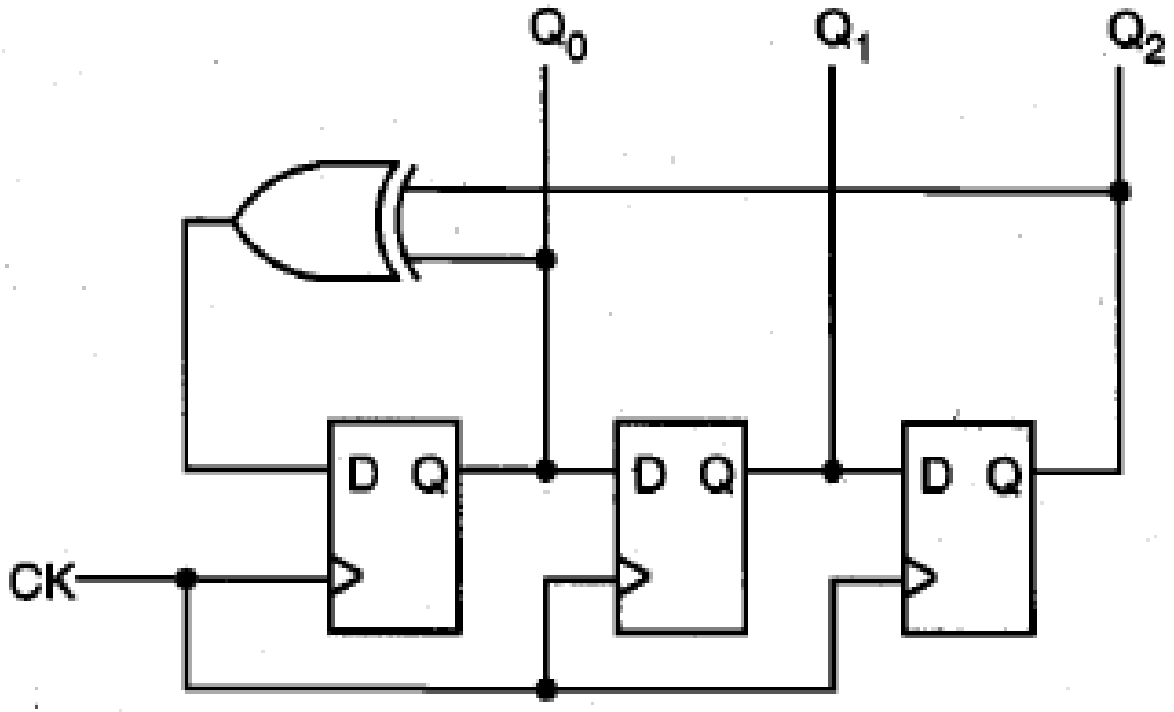
- To test the circuit, test patterns first have to be generated either by using a pseudo random pattern generator, a weighted test generator, an adaptive test generator, or other means.

- A pseudo random test generator circuit can use an LFSR

A procedure for BIST



A pseudo-random sequence generator using LFSRA pseudo-random sequence generator using LFSR



Linear Feedback Shift Register as an ORA

- To reduce the chip area penalty, data compression schemes are used to compare the compacted test responses instead of the entire raw test data.

- One of the popular data compression schemes is the *signature analysis, which is based on the concept of cyclic* redundancy checking.

- It uses polynomial division, which divides the polynomial representation of the test output data by a characteristic polynomial and then finds the remainder as the signature.

- The signature is then compared with the expected signature to determine whether the device under test is faulty.

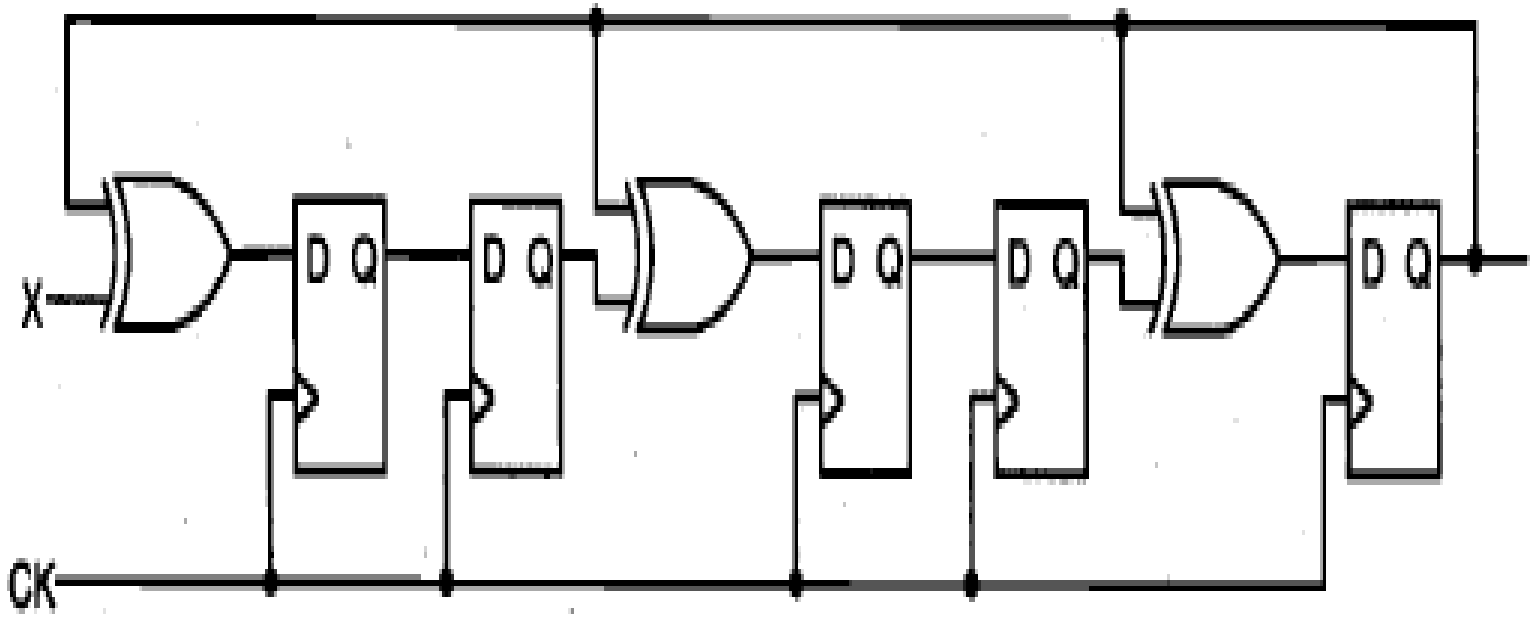


Figure 16.13. Polynomial division using LFSR for signature analysis.

Output Response Analyzer

- A simple alternative method is to compare the outputs of two identical circuits for the same input, with one of them regarded as reference.

- In addition to the above circuits for built-in self test, self-checking design techniques can be used to detect faults autonomously during on-line operation.

- Usually a checker circuit is inserted such that the checker generates and sends out a signal when on-line faults occur.

Built-In Logic Block Observer

- The built-in logic block observer (BILBO) register is a form of ORA which can be used in each cluster of partitioned registers.
- A basic BILBO circuit is which allows four different modes controlled by C0 and Cl signals.

3-bit built-in logic observer (BILBO) example