Dronacharya Group of Institutions, Greater Noida
Electronics & Communication Engineering Department
Question Bank

Subject: VLSI DESIGN (EEC-703) **Course: B. Tech 7th Sem (ECE)**

1. What are four generations of Integration Circuits?
   Hint Ans: SSI (Small Scale Integration)
   MSI (Medium Scale Integration)
   LSI (Large Scale Integration)
   VLSI (Very Large Scale Integration)

2. Give the advantages of IC?
   Hint Ans: Size is less
   High Speed
   Less Power Dissipation

3. Give the variety of Integrated Circuits?
   Hint Ans: More Specialized Circuits
   Application Specific Integrated Circuits(ASICs)
   Systems-On-Chip

4. Give the basic process for IC fabrication.
   Hint Ans: Silicon wafer Preparation
   Epitaxial Growth
   Oxidation
   Photolithography
   Diffusion
   Ion Implantation
   Isolation technique
   Metallization
   Assembly processing & Packaging

5. What are the various Silicon wafer Preparation?
   Hint Ans: Crystal growth & doping
   Ingot trimming & grinding
   Ingot slicing
   Wafer polishing & etching
   Wafer cleaning.

6. Different types of oxidation?
   Hint Ans: Dry & Wet Oxidation

7. What are the different layers in MOS transistors?
   Hint Ans: n-type transistors & p-type transistors.

8. What is Enhancement mode transistor?
   Hint Ans: The device that is normally cut-off with zero gate bias.

9. What is Depletion mode Device?
   Hint Ans: The Device that conduct with zero gate bias.

10. When the channel is said to be pinched –off?
    Hint Ans: If a large Vds is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the drain.

11. Give the different types of CMOS process?
    Hint Ans: p-well process
    n-well process Silicon-On-Insulator Process
    Twin- tub Process

12. What are the steps involved in twin-tub process?
    Hint Ans: Tub Formation
    Thin-oxide Construction
    Source & Drain Implantation
    Contact cut definition
    Metallization.

13. What are the advantages of Silicon-on-Insulator process?
    Hint Ans: No Latch-up
    Due to absence of bulks transistor structures are denser than bulk silicon.

14. What is BiCMOS Technology?
    Hint Ans: It is the combination of bipolar technology & CMOS technology.

15. What are the advantages of CMOS process?
    Hint Ans: Low Input Impedance
    Low delay Sensitivity to load.

16. What is the fundamental goal in Device modeling?
    Hint Ans: To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled.

17. Define Short Channel devices?
    Hint Ans: Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.

18. What is pull down device?
    Hint Ans: A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

19. What is pull up device?
Hint Ans: A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

20. Why NMOS technology is preferred more than PMOS technology?
Hint Ans: N- channel transistors has greater switching speed when compared tp PMOS transistors.

21. What are the different operating regions for an MOS transistor?
Hint Ans: Cutoff region
Non- Saturated Region
Saturated Region

22. What are the different MOS layers?
Hint Ans: n-diffusion
p-diffusion
Polysilicon
Metal

23. What is Stick Diagram?
Hint Ans: It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

24. What are the basic processing steps involved in BiCMOS process?
Hint Ans: Additional masks defining P base region
N Collector area
Buried Sub collector (SCCD)
Processing steps in CMOS process

25. What are the advantages of CMOS process?
Hint Ans: Low power Dissipation
High Packing density
Bi directional capability

26. Describe about the different design methodologies used in VLSI Design.

27. Discuss about the design flow of VLSI circuits in detail.

28. With the help of different examples explain about the concepts of Regularity, Modularity and Locality.

29. Draw the stick diagram of CMOS inverter.

30. Derive the current voltage relationship of NMOS for different bias conditions.

31. Describe about the different scaling techniques in detail.

32. Explain about the small geometry effects.

33. List and explain about the capacitances related to MOS under different bias conditions.

34. Explain about Y-diagram and design hierarchy.

35. With the help of diagrams explain about the Resistive load inverters.

36. What is the advantage of active load inverter? Discuss the advantages and disadvantages of different active load inverters with suitable diagram.

37. What is the cause of delay in CMOS inverter? Define the time delay parameters in CMOS.

38. Explain with suitable diagram the working of a CMOS inverter and also give different voltage levels in all five regions.

39. With the help of NMOS and PMOS characteristic curves explain the different regions of CMOS inverter, also explain why it exhibits a large gain in region3.

40. Find the expression for time delay in CMOS inverter by approximate or average method and exact method.

41. Explain about the leakage currents in DRAM cells and refresh operations.

42. Draw the circuit of CMOS falling edge triggered master slave D flip flop.

43. Realize the CMOS full adder circuit with minimum number of transistors. What will happen if pull-up network is implemented by NMOS and pull down network is implemented by PMOS?

44. Explain in detail about the transmission gate and also prove that the effective impedance is independent of the output voltage.

45. Draw the circuit of CMOS falling edge triggered master slave D flip flop and also explain about it.

46. Derive the relationship between Current & Voltage for an NMOS enhancement transistor for cutoff, Linear and saturation.

47. What are the different parasitic capacitances associated with NMOS Transistor in cutoff, linear and saturation region.

48. With neat diagram explain the working of resistive load inverter. Also discuss the merit and demerit of this inverter.

49. What is the advantage of active load inverter? Discuss the advantages and disadvantages of different active load inverters with suitable diagram.

50. What is the cause of delay in CMOS inverter? Define the time delay parameters in CMOS.

51. Explain with suitable diagram the working of a CMOS inverter and also give different voltage levels in all five regions.

52. With the help of NMOS and PMOS characteristic curves explain the different regions of CMOS inverter, also explain why it exhibits a large gain in region3.

53. Explain in detail about the power consumption in CMOS inverter and also find the expression for it.

54. Why threshold logic voltage of a CMOS inverter kept as 50% off supply voltage. Under what condition it can be maintained? Find the expression for it.

55. Discuss in detail about the small geometry effects of an NMOS inverter.

56. What will happen if the current ratio of an NMOS and PMOS kept less than 1 and greater than 1?

57. Give two different configurations of the BiCMOS inverter. How these configurations can provide a larger fan out?

58. How the width of the uncertainty region can be kept small? Why a small uncertainty region results in a larger noise margin?

59. Realize the CMOS full adder circuit with minimum number of transistors. What will happen if pull-up network is implemented by NMOS and pull down network is implemented by PMOS?

60. Explain in detail about the transmission gate and also prove that the effective impedance is independent of the output voltage.

61. Explain in detail with suitable diagrams about the various configurations of DRAM cell.

62. Draw the circuit of CMOS falling edge triggered master slave D flip flop and also explain about it.

63. Derive the relationship between Current & Voltage for an NMOS enhancement transistor for cutoff, Linear and saturation.

64. With neat diagram explain the working of resistive load inverter. Also discuss the merit and demerit of this inverter.

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