Unit 1
Lecture 6

Logic Devices for Interfacing

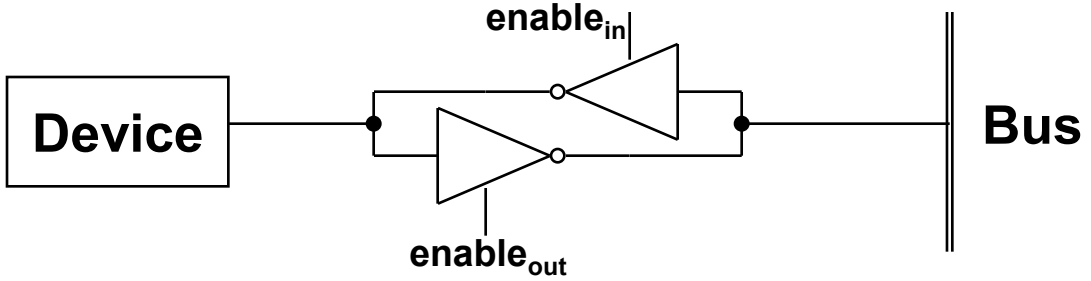
- Tri-State devices
- Buffer
- Bidirectional Buffer
- Decoder
- Encoder
- D Flip Flop :Latch and Clocked

Tri-state Logic Outputs

- Since we can have multiple masters on a bus, we need Tri-state logic for attachment to a bus so that each device can choose to drive or not drive the bus depending on whether it is the bus master for a given bus cycle
- Tri-state logic prevents a bus conflict where one device is driving a signal to 1 and another device is driving it to 0 at the same time – generates high current through wires (and smoke?)

Tri-State Logic and Buses

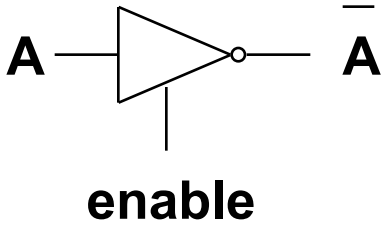
- The logical element has output enable pin to go from a floating output to drive the output from the circuit
- Inverters and buffers are used as bus drivers or buffers
  - Two such drivers or buffers in opposite directions are used to make the connection bi-directional
  - The gates also provide more “drive” onto the bus so that the bus signals are stronger and the bus can be longer .



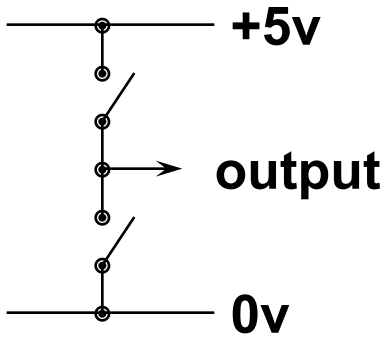
Tri-State Logic

- The problem with connecting multiple "normal" outputs together on a bus is that each has to be in one logic state (0) or the other (1) – driving voltage on each bus signal high or low.
- This represents a conflict over the state of the signal.
- We resolve this conflict with *tri-state logic.*

Logically



Electrically

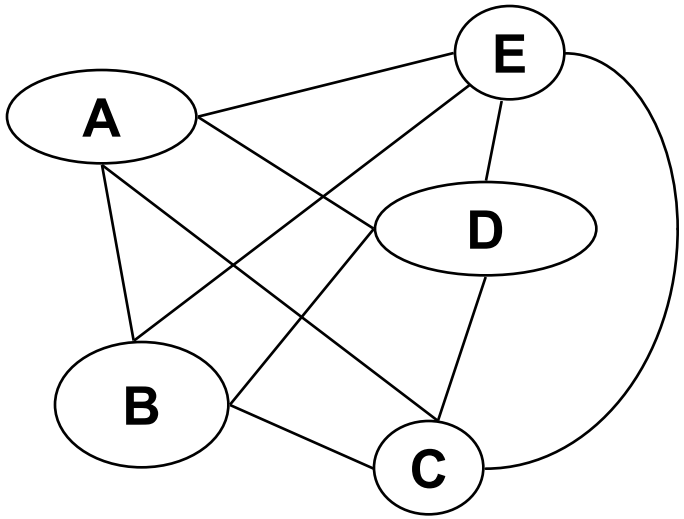


Truth Table

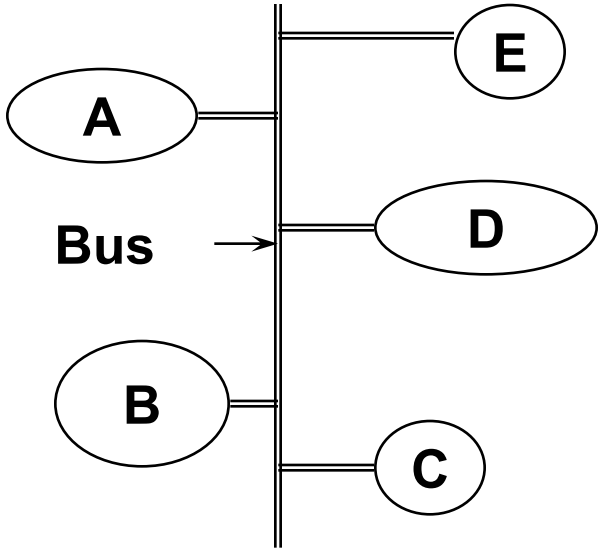
enable	A	Output
0	0	(Z)
0	1	(Z)
1	0	1
1	1	0

Buses

- Concept is to link together multiple functional units over a common data highway at a lower cost than using multiple point to point links.

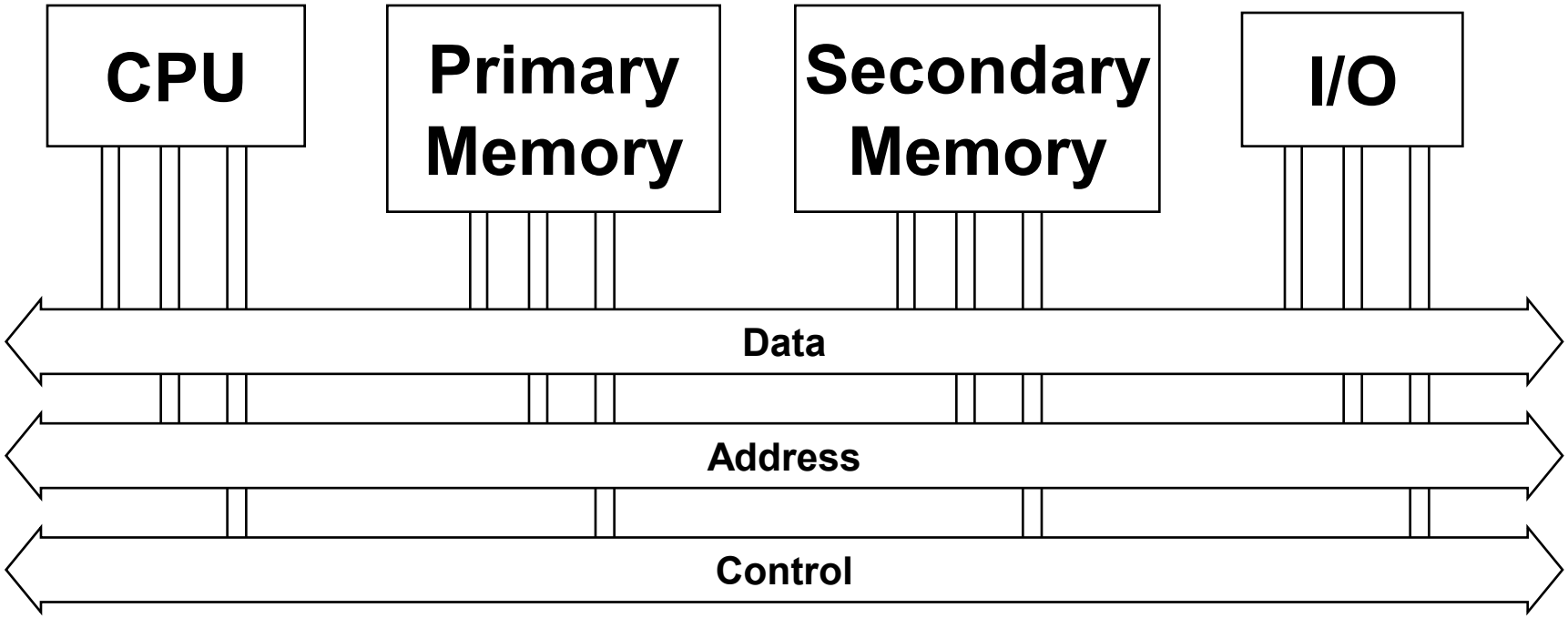


OR

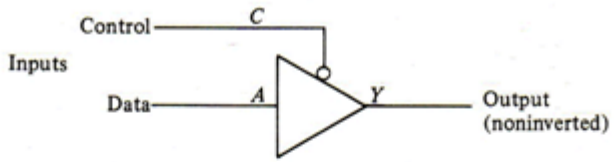


Number of Links = n * (n – 1) / 2

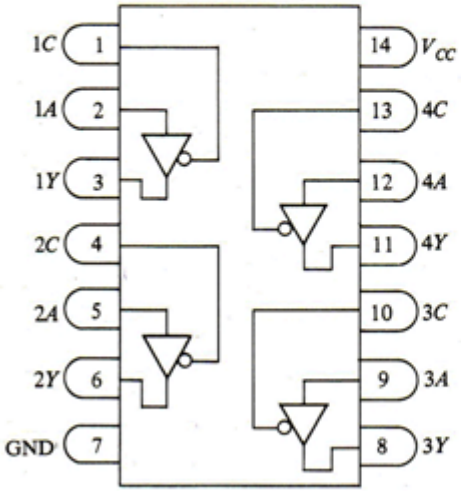
Bus – Essential Part of Any Computer



Tri-State Logic and Buses



(a) Logic symbol of a three-state buffer



(b) Pin diagram

Inputs		Output
C	*A*	*Y*
L	L	L
L	H	H
H	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = don't care
(Z) = high impedance (off)

(c) Truth table

74125 quad three-state buffer IC

Bus Master – Slave Relationships

- Up till now, I have said that the address bus and the control bus are always driven by the processor, however that is NOT really true!
- That was only a “lie of simplification”!
- The processor is NOT the only device that may be driving the address and control busses .
- Hopefully you are now well-prepared for me to un-simplify a bit.

Bus Arbitration

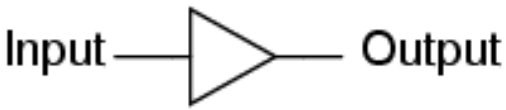
- Bus arbitration is used to hand off a bus between one of several potential bus masters using signals that are a part of the bus itself.
- A bus arbitration protocol implements some form of bus request and bus grant handshake to determine which device will be the master on the bus for the next bus cycle.

Tri-State Bus Summary

- All devices have tri-state logic connections to the data bus – may be driving or receiving.
- Memory and I/O devices don't need tri-state logic on address/control bus (never drive them).
- Because the processor may need to yield the control/address busses, it must have tri-state logic for driving those bus signals.
- DMAC controller must have tri-state logic for driving the control and address bus signals.

BUFFER

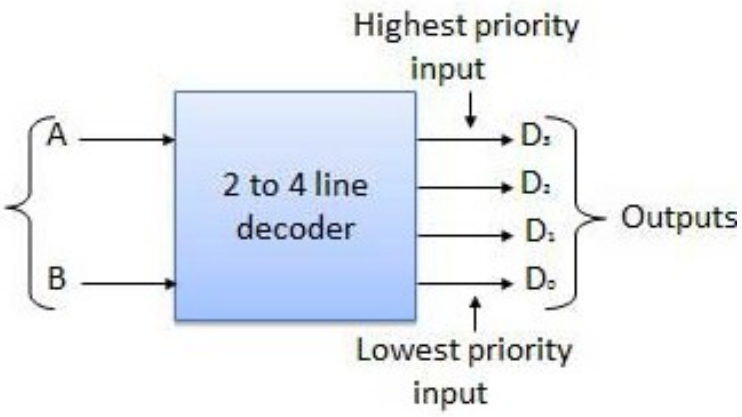
- A buffer has only a single input and a single output with behavior that is the opposite of an NOT gate. It simply passes its input, unchanged, to its output. In a Boolean logic simulator, a buffer is mainly used to increase propagation delay. In a real-world circuit, a buffer can be used to amplify a signal if its current is too



Input	Output
0	0
1	1

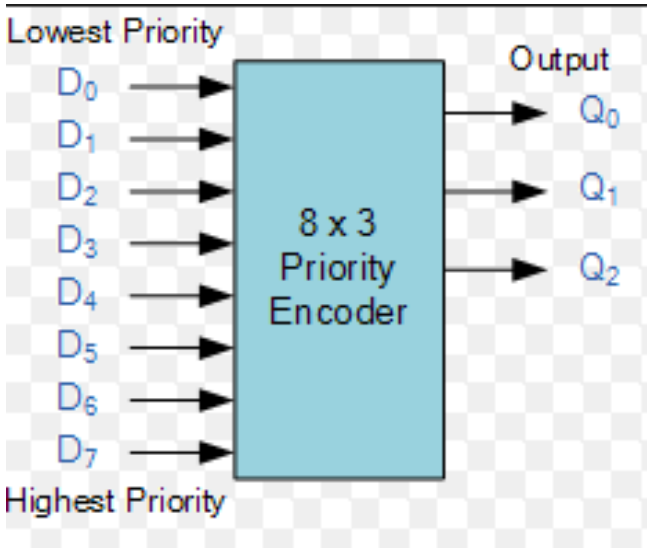
DECODER

A **decoder** is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a m output lines.



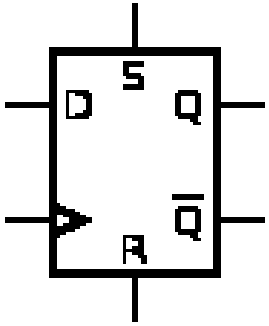
ENCODER

- An **encoder** is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security or compressions.



D FLIP FLOP: Latched and Clocked

- A **flip-flop** or latch is a circuit that has two stable states and can be used to store state information. A **flip-flop** is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
- The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop.
- The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.



Truth table:

Clock	D	Q_{next}
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	Q