Unit 3
Lecture 1
16-bit Microprocessors

16 Bit DATA TRANSFER TO REGISTER PAIR (LXI)

Load register pair immediate

- LXI Reg. pair, 16-bit data.
- The instruction loads 16-bit data in the register pair designated in the operand.
- Example: LXI H, 2034H or LXI H, XYZ

16 Bit DATA TRANSFER TO REGISTER PAIR (LXI)

Load H and L registers direct

- LHLD 16-bit address
- The instruction copies the contents of the memory location pointed out by the 16-bit address into register L and copies
  the contents of the next memory location into register H.
- The contents of source memory locations are not altered.
- Example: LHLD 2040H

DATA TRANSFER FROM MEMORY TO MICROPROCESSOR

MOV R,M

- R, M copies data byte from Memory to Register. Memory location, its location is specified by the contents of the HL registers.

- Example: MOV B, M

- Load accumulator indirect

DATA TRANSFER FROM MEMORY TO MICROPROCESSOR

LDAX B/D Reg. pair

- The contents of the designated register pair point to a memory location. This instruction copies the contents of that memory location into the accumulator. The contents of either the register pair or the memory location are not altered.
- Example: LDAX B

Load accumulator

- LDA 16-bit address The contents of a memory location, specified by a 16-bit address in the operand, are copied to the accumulator.
- The contents of the source are not altered.
- Example: LDA 2034H

DATA TRANSFER FROM MICROPROCESSOR TO MEMORY OR DIRECTLY INTO MEMORY

MOV M,R

- This instruction copies the contents of the source.
- The source register are not altered. As one of the operands is a memory location, its location is specified by the contents of the HL registers.
- Example: MOV M, B

- **STA 16-bit address**
- The contents of the accumulator are copied into the memory location specified by the operand.
- This is a 3-byte instruction, the second byte specifies the low-order address and the third byte specifies the high-order address.
- Example: STA 4350H

(cont.)

Store accumulator indirect

- STAX Reg. pair The contents of the accumulator are copied into the memory location specified by the contents of the operand (register pair). The contents of the accumulator are not altered.
- Example: STAX B

(cont.)

Store H and L registers indirect

- SHLD 16-bit address The contents of register L are stored into the memory location specified by the 16-bit address in the operand and the contents of H register are stored into the next memory location by incrementing the operand. The contents of registers HL are not altered. This is a 3-byte instruction, the second byte specifies the low-order address and the third byte specifies the high-order address.

- Example: SHLD 2470H

Arithmetic Operations Related to 16 Bits or Register Pairs

Increment register pair by 1

- INX R The contents of the designated register pair are incremented by 1 and the result is stored in the same place.
- Example: INX H

Decrement register pair by 1

- DCX R The contents of the designated register pair are decremented by 1 and the result is stored in the same place.
- Example: DCX H

Arithmetic Operations Related to Memory

Add memory

- ADD M : The contents of the operand (memory) are added to the contents of the accumulator and the result is stored in the accumulator.
- The operand is a memory location, its location is specified by the contents of the HL registers.
- All flags are modified to reflect the result of the addition.

Arithmetic Operations Related to Memory

Subtract memory

- SUB M : The contents of the operand (memory) are subtracted to the contents of the accumulator and the result is stored in the accumulator. The operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the Subtraction.

Increment memory by 1/Decrement memory by 1

- INR M/DCR M : The contents of the memory are incremented by 1 using INR and decremented by 1 using DCR and the result is stored in the same place. The operand is a memory location, its location is specified by the contents of the HL registers.