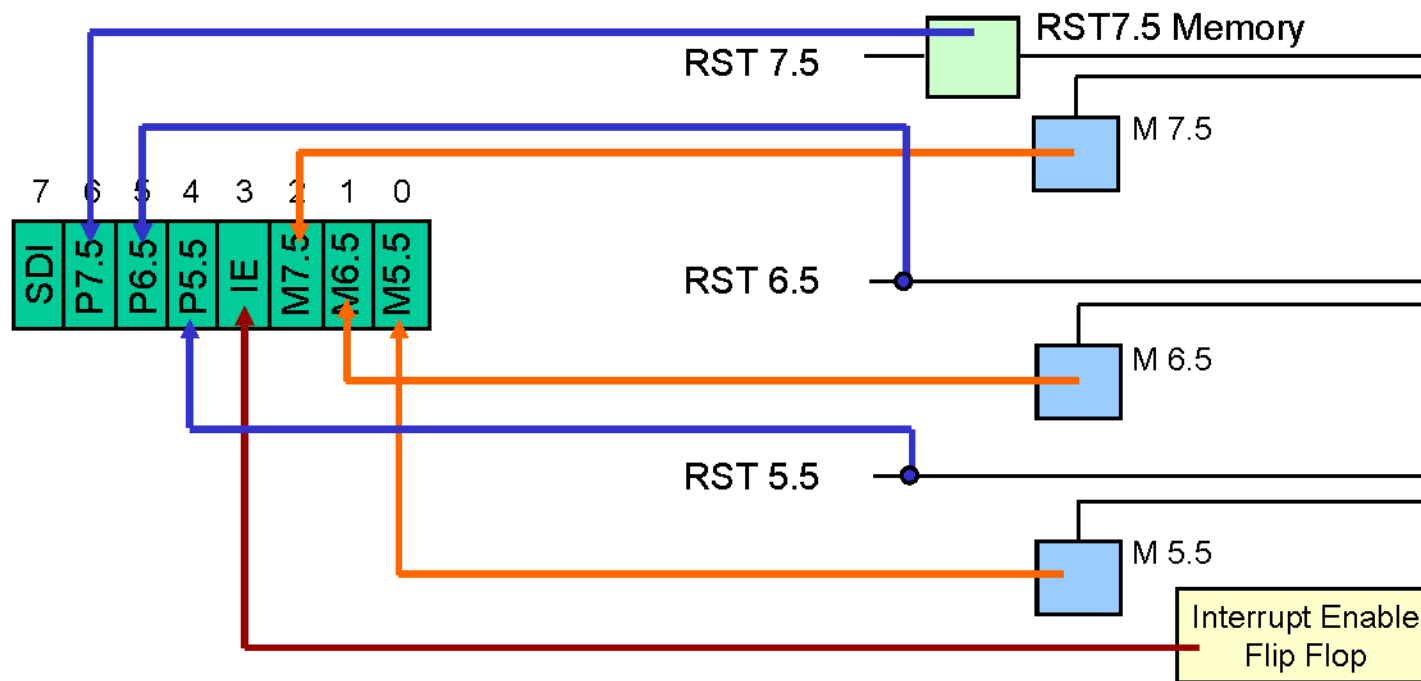


Unit 3

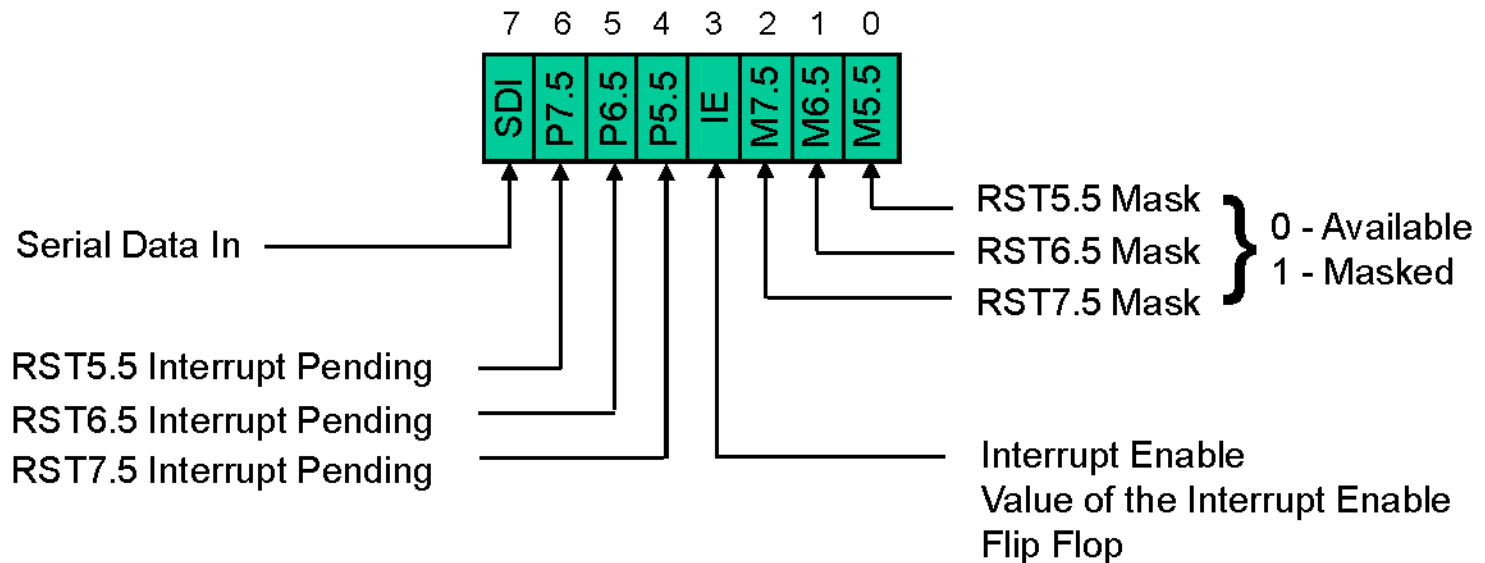
LECTURE 7

Determining the Current Mask Settings

- RIM instruction: Read Interrupt Mask
 - Load the **accumulator** with an 8-bit pattern showing the status of each interrupt pin and mask.



How RIM sets the Accumulator's different bits



The RIM Instruction and the Masks

- Bits 0-2 show the current **setting of the mask** for each of RST 7.5, RST 6.5 and RST 5.5
 - They return the contents of the three mask flip flops.
 - They can be used by a program to read the mask settings in order to modify only the right mask.
- Bit 3 shows whether the maskable interrupt process is **enabled or not**.
 - It returns the contents of the Interrupt Enable Flip Flop.
 - It can be used by a program to determine whether or not interrupts are enabled.

The RIM Instruction and the Masks

- Bits 4-6 show whether or not there are **pending interrupts** on RST 7.5, RST 6.5, and RST 5.5
 - Bits 4 and 5 return the current value of the RST5.5 and RST6.5 **pins**.
 - Bit 6 returns the current value of the RST7.5 memory **flip flop**.
- Bit 7 is used for **Serial Data Input**.
 - The RIM instruction reads the value of the **SID pin** on the microprocessor and returns it in this bit.

Pending Interrupts

- Since the 8085 has five interrupt lines, interrupts may occur during an ISR and remain pending.
 - Using the **RIM** instruction, the programmer can read the status of the interrupt lines and find if there are any pending interrupts.
 - The advantage is being able to find about interrupts on RST 7.5, RST 6.5, and RST 5.5 without having to enable low level interrupts like INTR.

Using RIM and SIM to set Individual Masks

- Example: Set the mask to enable RST6.5 without modifying the masks for RST5.5 and RST7.5.
 - In order to do this correctly, we need to use the RIM instruction to find the current settings of the RST5.5 and RST7.5 masks.
 - Then we can use the SIM instruction to set the masks using this information.
 - Given that both RIM and SIM use the Accumulator, we can use some logical operations to mask the un-needed values returned by RIM and turn them into the values needed by SIM.

Using RIM and SIM to set Individual Masks

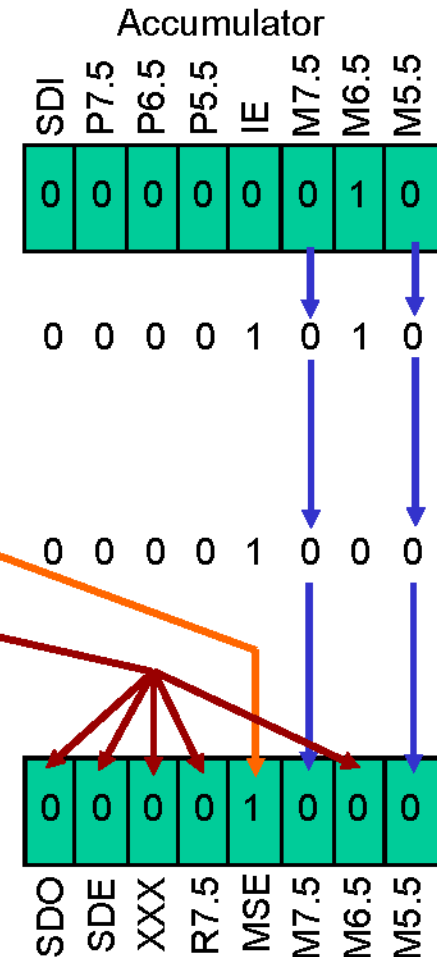
- Assume the RST5.5 and RST7.5 are enabled and the interrupt process is disabled.

RIM ; Read the current settings.

ORI 08H ; 0 0 0 0 1 0 0 0
; Set bit 4 for MSE.

ANI 0DH ; 0 0 0 0 1 1 0 1
; Turn off Serial Data, Don't reset
; RST7.5 flip flop, and set the mask
; for RST6.5 off. Don't cares are
; assumed to be 0.

SIM ; Apply the settings.



TRAP

- TRAP is the only **non-maskable** interrupt.
 - It does not need to be enabled because it **cannot be disabled**.
- It **has the highest priority** amongst interrupts.
- It is **edge and level sensitive**.
 - It needs to be high and stay high to be recognized.
 - Once it is recognized, it won't be recognized again until it goes low, then high again.
- TRAP is usually used for power failure and emergency shutoff.

Internal Interrupt Priority

- Internally, the 8085 implements an **interrupt priority scheme**.
 - The interrupts are ordered as follows:
 - TRAP
 - RST 7.5
 - RST 6.5
 - RST 5.5
 - INTR
 - However, TRAP has lower priority than the HLD signal used for DMA.

The 8085 Interrupts

Interrupt Name	Maskable	Masking Method	Vectored	Memory	Triggering Method
INTR	Yes	DI / EI	No	No	Level Sensitive
RST 5.5 / RST 6.5	Yes	DI / EI SIM	Yes	No	Level Sensitive
RST 7.5	Yes	DI / EI SIM	Yes	Yes	Edge Sensitive
TRAP	No	None	Yes	No	Level & Edge Sensitive