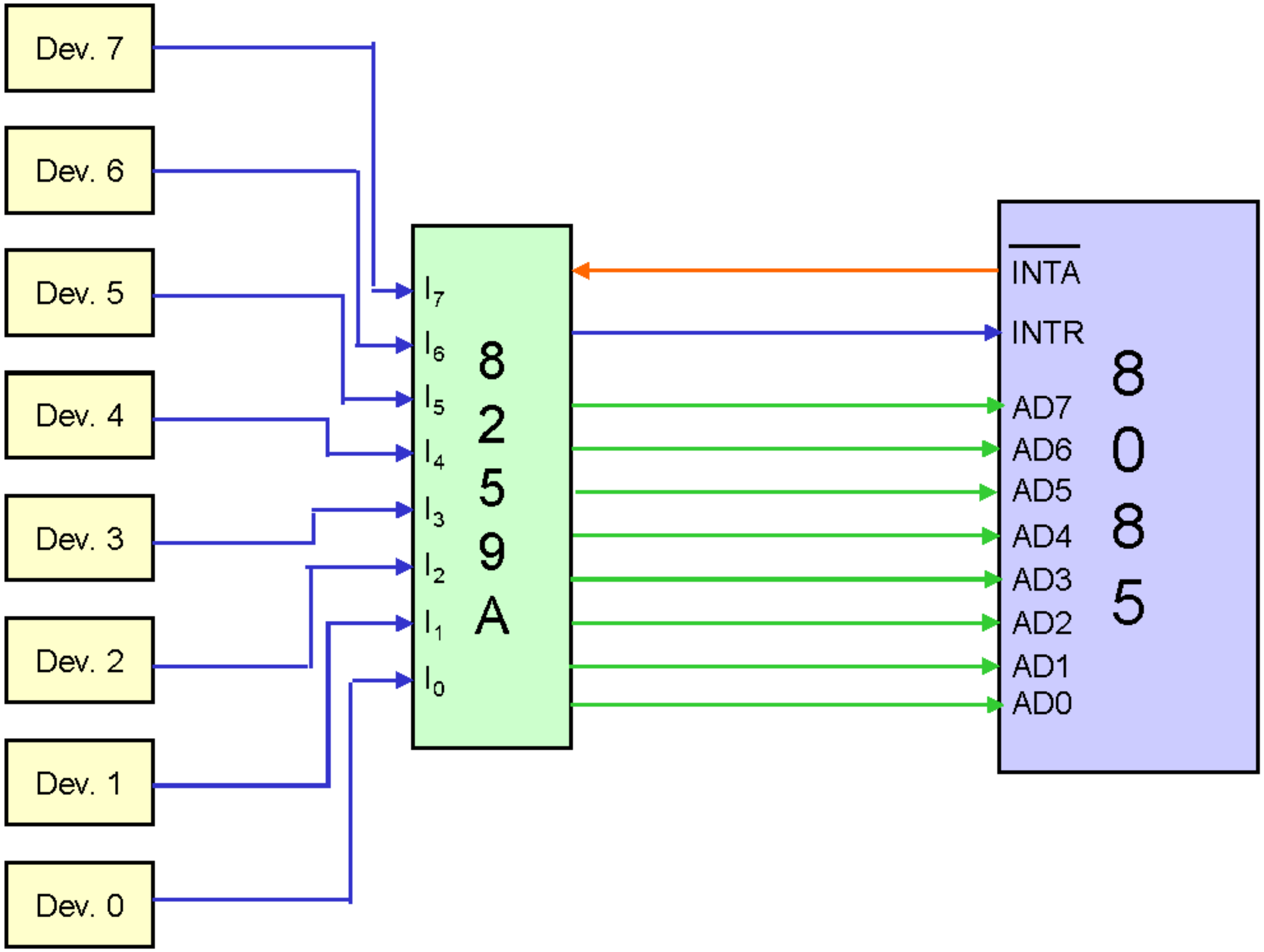
Unit 5
LECTURE 4

The Need for the 8259A

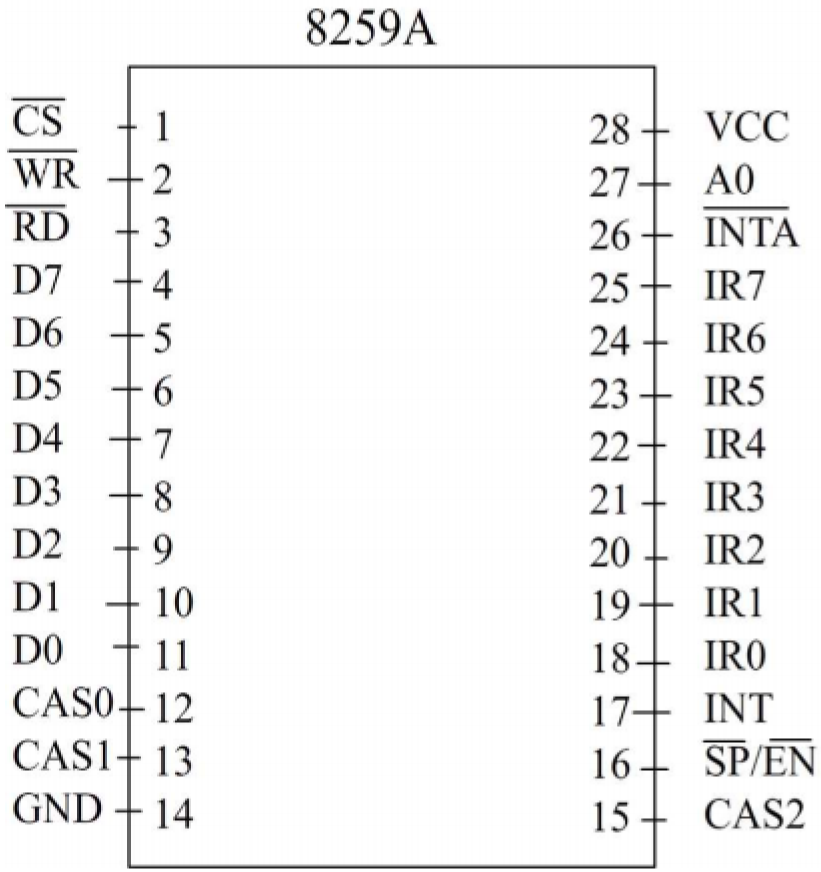
- The 8085 INTR interrupt scheme presented earlier has a few limitations:
  - The RST instructions are all vectored to memory page 00H, which is usually used for ROM.
  - It requires additional hardware to produce the RST instruction opcodes.
  - Priorities are set by hardware.

- Therefore, we need a device like the 8259A to expand the priority scheme and allow mapping to pages other than 00H.

Interfacing the 8259A to the 8085



PIN DIAGRAM



The pins are defined as follows:

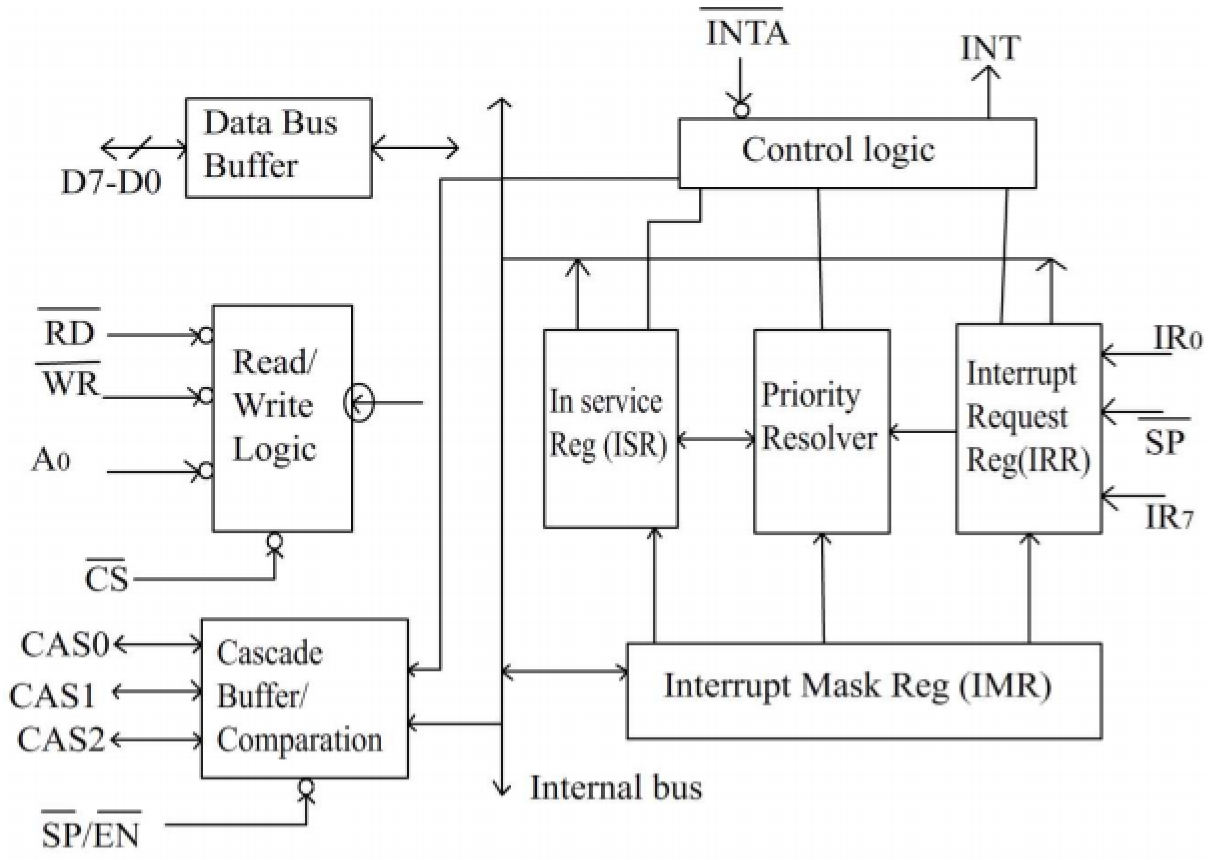
FUNCTIONAL DESCRIPTION

❖The 8259 A has eight interrupt request inputs, TR2 IR0. The 8259 A uses its INT output to interrupt the 8085A via INTR pin. The 8259A receives interrupt acknowledge pulses from the at its input.

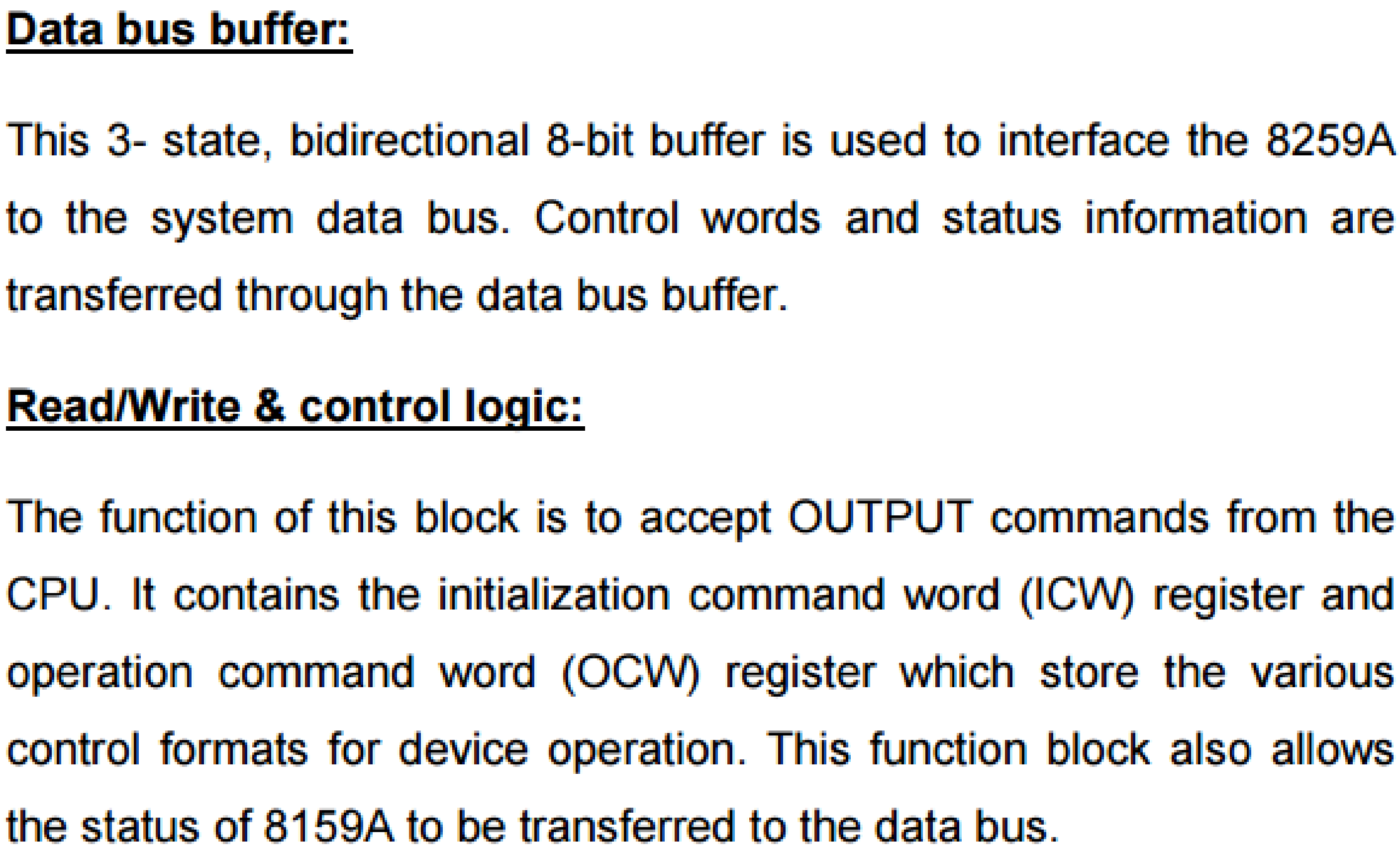
❖Vector address used by the 8085 A to transfer control to the service subroutine of the interrupting device, is provided by the 8259 A on the data bus.

❖The 8259A is a programmable device that must be initialized by command words sent by the. After initialization the 8259 A mode of operation can be changed by operation command words from the.

8259A ARCHITECTURE



8259A Description



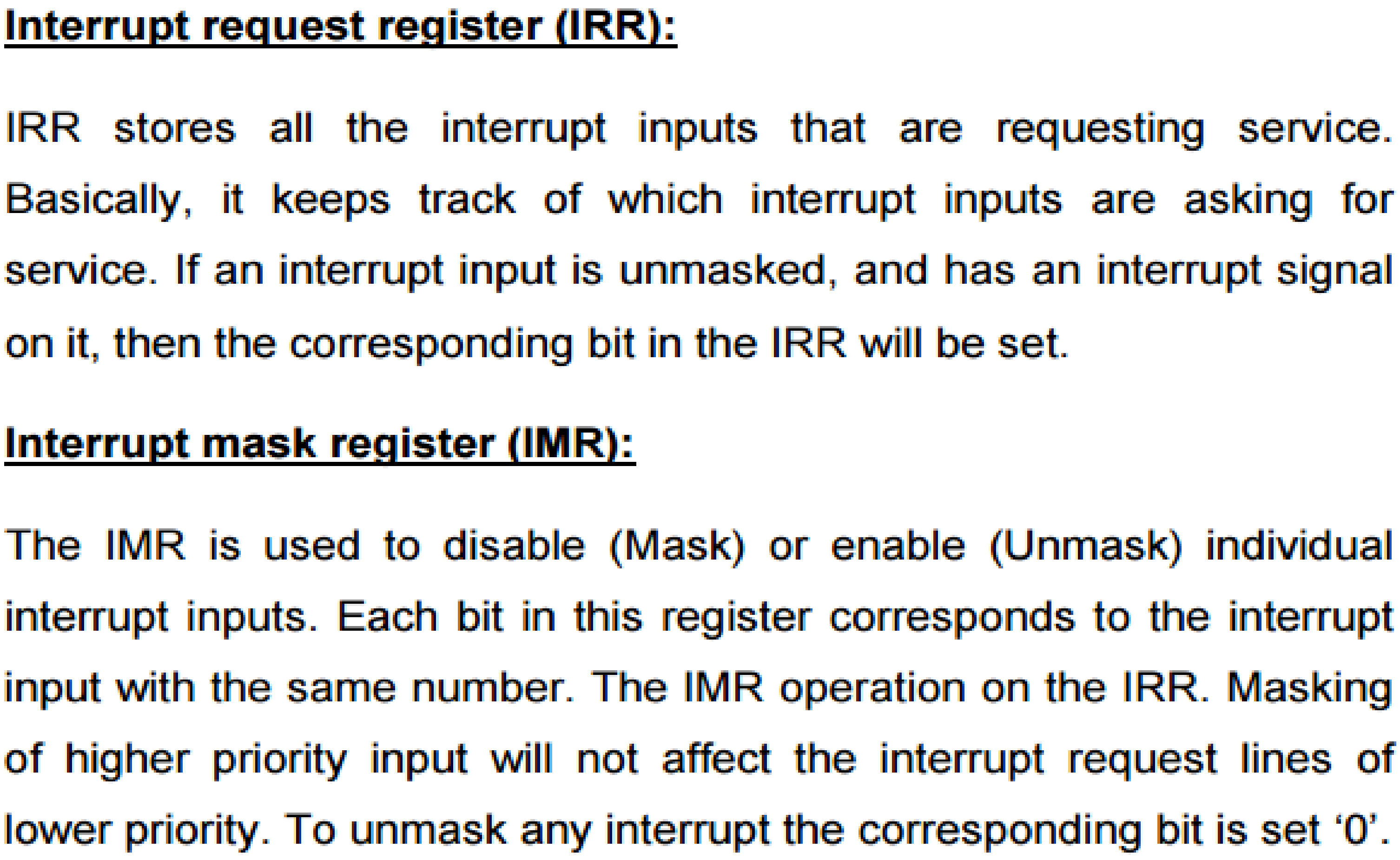
Data bus buffer:

This 3- state, bidirectional 8-bit buffer is used to interface the 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write & control logic:

The function of this block is to accept OUTPUT commands from the CPU. It contains the initialization command word (ICW) register and operation command word (OCW) register which store the various control formats for device operation. This function block also allows the status of 8159A to be transferred to the data bus.

8259A Description (CONT.)



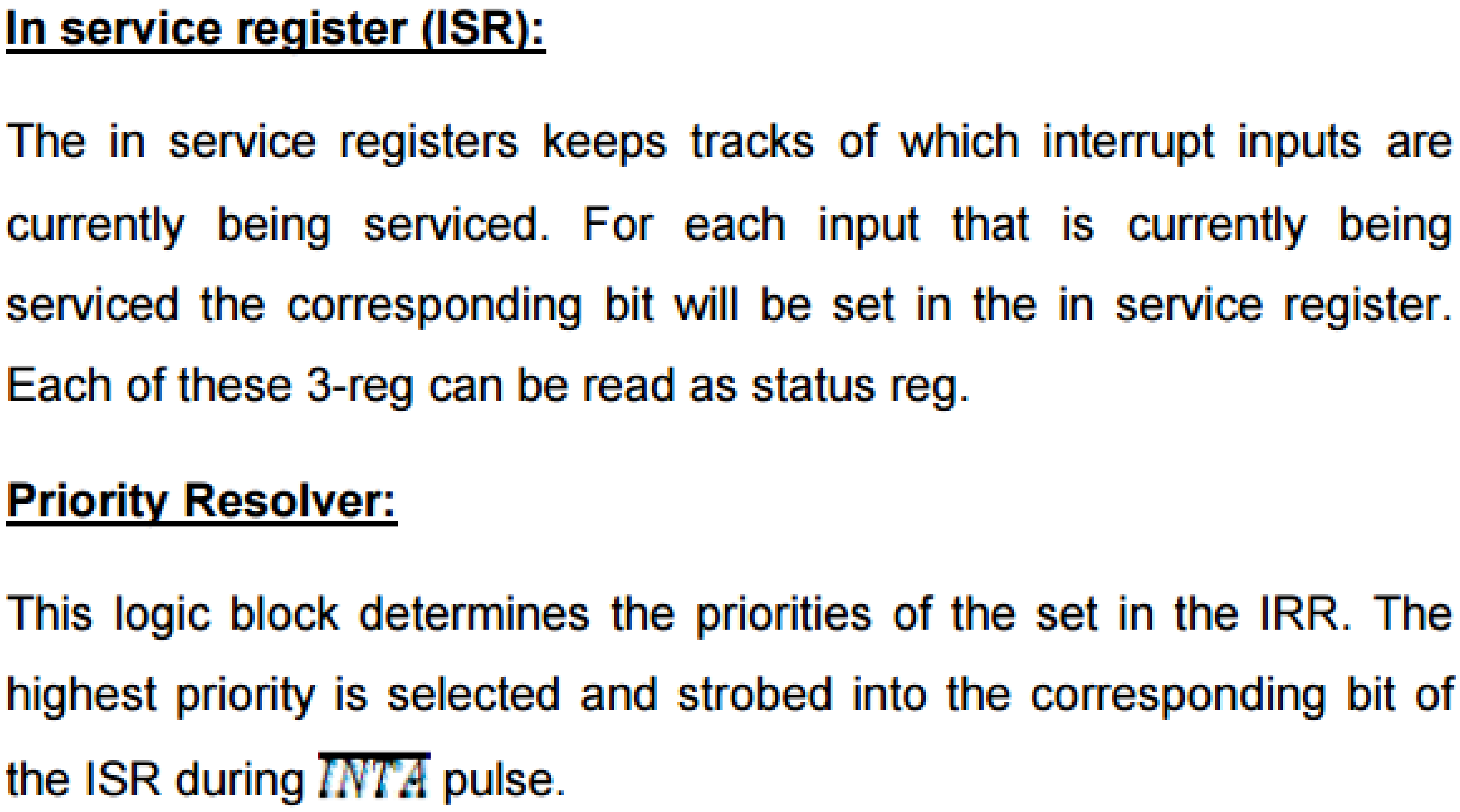
Interrupt request register (IRR):

IRR stores all the interrupt inputs that are requesting service. Basically, it keeps track of which interrupt inputs are asking for service. If an interrupt input is unmasked, and has an interrupt signal on it, then the corresponding bit in the IRR will be set.

Interrupt mask register (IMR):

The IMR is used to disable (Mask) or enable (Unmask) individual interrupt inputs. Each bit in this register corresponds to the interrupt input with the same number. The IMR operation on the IRR. Masking of higher priority input will not affect the interrupt request lines of lower priority. To unmask any interrupt the corresponding bit is set ‘0’.

8259A Description (CONT.)



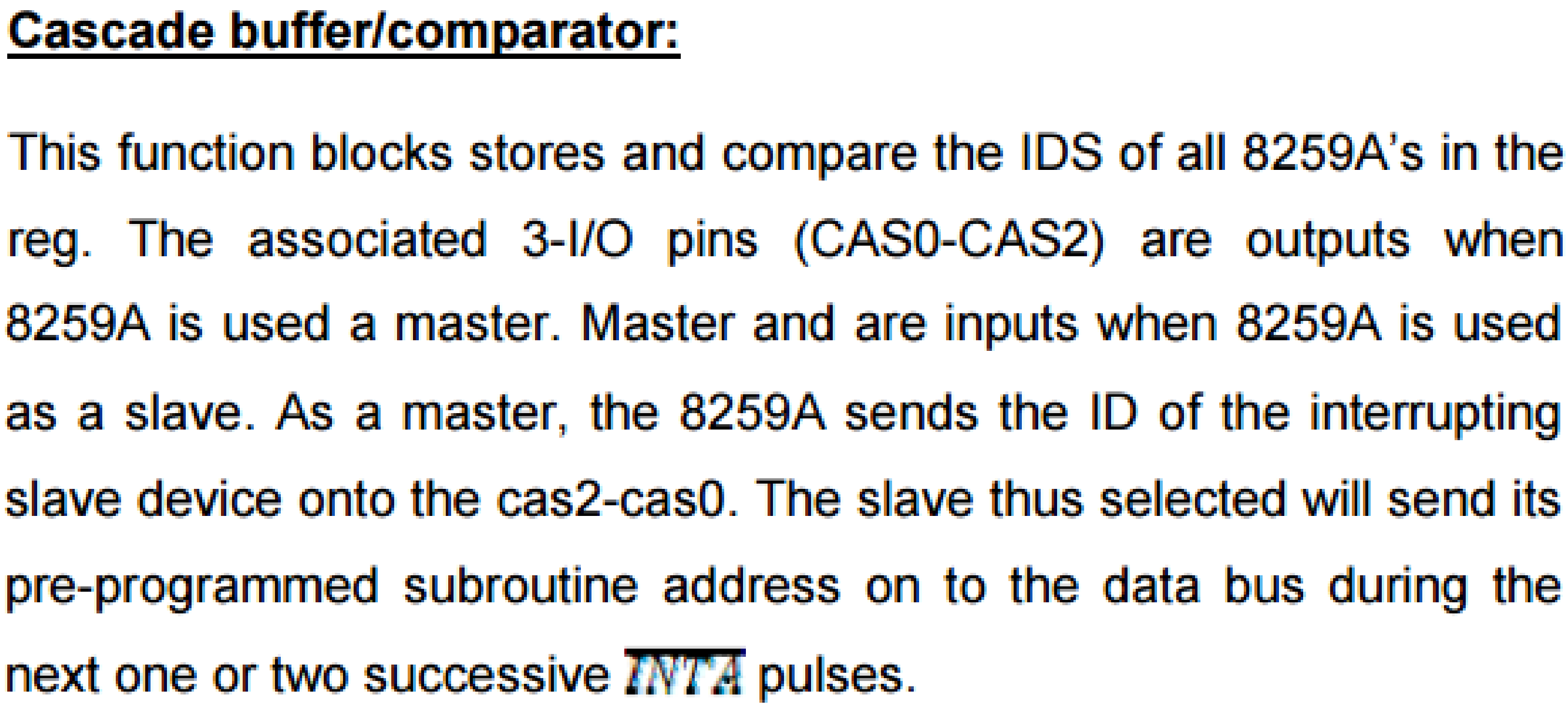
In service register (ISR):

The in service registers keeps tracks of which interrupt inputs are currently being serviced. For each input that is currently being serviced the corresponding bit will be set in the in service register. Each of these 3-reg can be read as status reg.

Priority Resolver:

This logic block determines the priorities of the set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

8259A Description (CONT.)



Cascade buffer/comparator:

This function blocks stores and compare the IDS of all 8259A's in the reg. The associated 3-I/O pins (CAS0-CAS2) are outputs when 8259A is used a master. Master and are inputs when 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the cas2-cas0. The slave thus selected will send its pre-programmed subroutine address on to the data bus during the next one or two successive $\overline{INTA}$ pulses.

Operating of the 8259A

- The 8259A requires the microprocessor to provide 2 control words to set up its operation. After that, the following sequence occurs:

1. One or more interrupts come in.
2. The 8259A resolves the interrupt priorities based on its internal settings
3. The 8259A sends an INTR signal to the microprocessor.
4. The microprocessor responds with an INTA signal and turns off the interrupt enable flip flop.
5. The 8259A responds by placing the op-code for the CALL instruction (CDH) on the data bus.

Operating of the 8259A

6. When the microprocessor receives the op-code for CALL instead of RST, it recognizes that the device will be sending 16 more bits for the address.
7. The microprocessor sends a second INTA signal.
8. The 8259A sends the high order byte of the ISR's address.
9. The microprocessor sends a third INTA signal.
10. The 8259A sends the low order byte of the ISR's address.
11. The microprocessor executes the CALL instruction and jumps to the ISR.